54F/74F384

8-Bit Serial/Parallel Twos Complement Multiplier

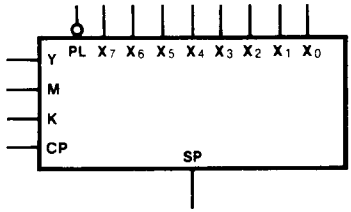
Description

The 'F384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand (X_0-X_7). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

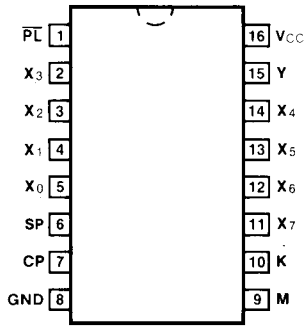
The K input is used for expansion to longer X words, using two or more 'F384 devices. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load ($\overline{PL}$) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

Ordering Code: See Section 5

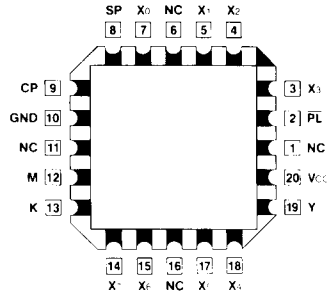
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
K	Serial Expansion Input	0.5/0.375
M	Mode Control Input	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.75
X_0-X_7	Multiplicand Data Inputs	0.5/0.375
Y	Serial Multiplier Input	0.5/0.375
SP	Serial X•Y Product Output	25/12.5

Functional Description

Referring to the Logic Diagram, the multiplicand (X_0-X_7) latches are enabled to receive new data when $\overline{PL}$ is LOW. Data that meet the setup time requirements are latched and stored when $\overline{PL}$ goes HIGH. The LOW signal on $\overline{PL}$ also clears the Y_{a-1} flip-flop as well as the carry-save flip-flops and the partial product register in the arithmetic section. Figure a is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the carry logic. The cells use the carry-save technique to avoid the complexity and delays inherent in lookahead carry schemes for longer words.

Figure b is a timing diagram for an 8x8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that $\overline{PL}$ goes LOW shortly after the CP rising edge that marks the beginning of T_0 and goes HIGH again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input (X_0 Y_0) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the SP output of the package. The next-least bit (Y_1) of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the SP output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the SP output contains information formed one stage further upstream. For example, the SP output during T_9 contains X_7Y_0, which was actually formed during T_1.

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the 'F322 Shift Register. Figure c shows the method of using two 'F384s to perform a 12xn bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to X_4-X_7 of the most significant package. Whereas the 8x8 multiplication required 18 clock periods (m + n to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of Figure c requires 12 + n bits to form the product terms plus the bit times to clear the multiplier and to recognize and store SP_{n+11}.

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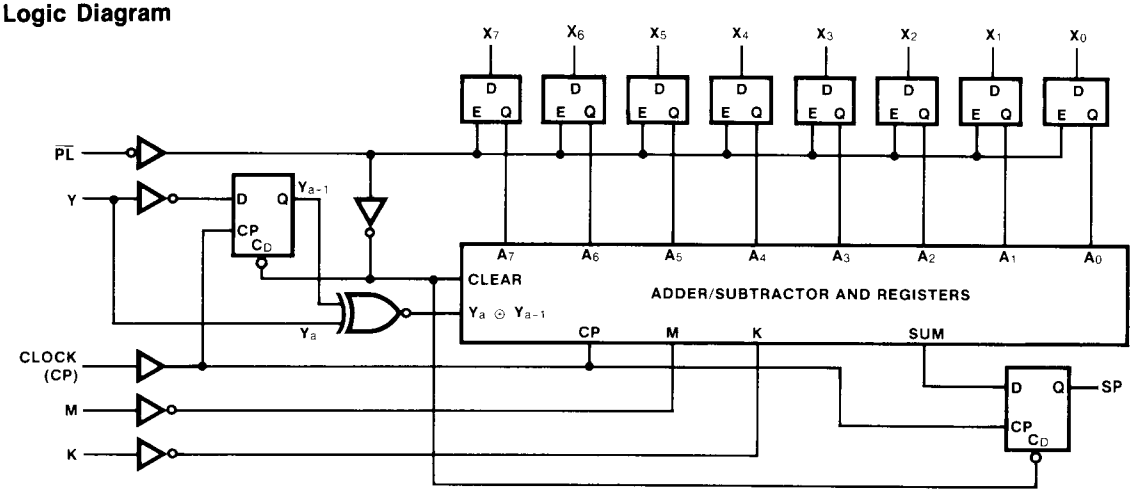
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs						Internal	Output	Function
$\overline{PL}$	CP	K	M	X_i	Y	Y_{a-1}	SP	
X	X	L	L	X	X	X	X	Most Significant Multiplier Device
X	X	CS	H	X	X	X	X	Devices Cascaded in Multiplier String
L	X	X	X	OP	X	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	X	X	X	X	X	X	X	Device Enabled
H	↑	X	X	X	L	L	AR	Shift Sum Register
H	↑	X	X	X	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	X	X	X	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	X	X	X	H	H	AR	Shift Sum Register

H = HIGH Voltage Level
L = LOW Voltage Level
↑ = LOW-to-HIGH Transition
CS = Connected to SP output of high order device
OP = X_i latches open for new data (i = 0-7)
AR = Output as required per Booth's algorithm
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		60	90	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	100					70	MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to SP	3.5 3.5	6.5 6.5	9.0 9.0			3.5 3.5	10.0 10.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{PL}$ to SP	6.0	10.0	13.0			6.0	14.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW K to CP	13.5 13.5		15.0 15.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW K to CP	2.0 2.0		2.0 2.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Y to CP	15.0 15.0		15.0 15.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Y to CP	2.0 2.0		2.0 2.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW X_n to $\overline{PL}$	5.5 5.5		6.5 6.5	ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW X_n to $\overline{PL}$	2.0 2.0		2.0 2.0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 5.5		7.5 6.0	ns	3-7
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	6.5		7.0	ns	3-11
t_{rec}	Recovery Time $\overline{PL}$ to CP	5.5		6.0	ns	3-11

Fig. a Conceptual Carry Save Adder Cell

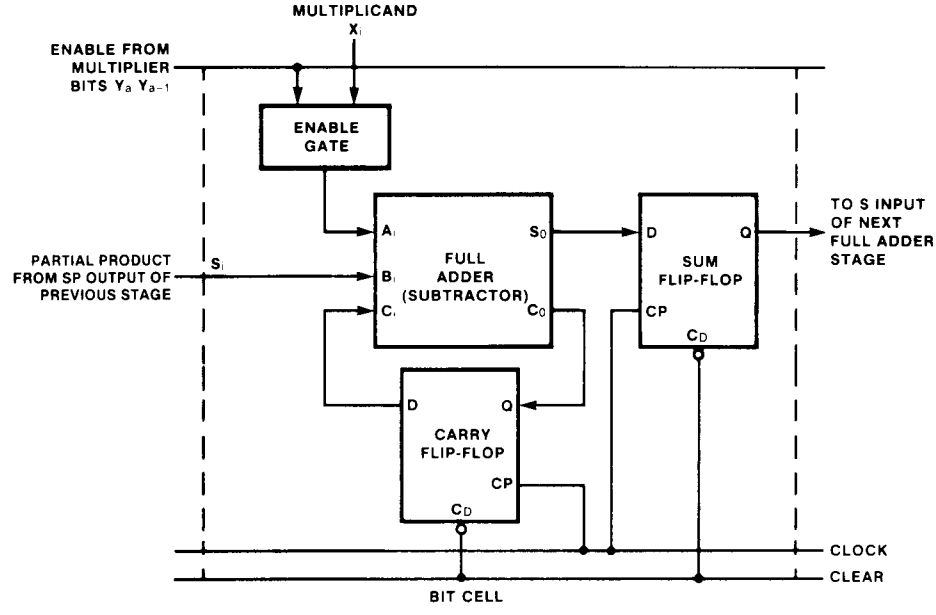


Fig. b Timing Diagram Showing 18 Clock Cycle Operation of 8x8 Multiplication

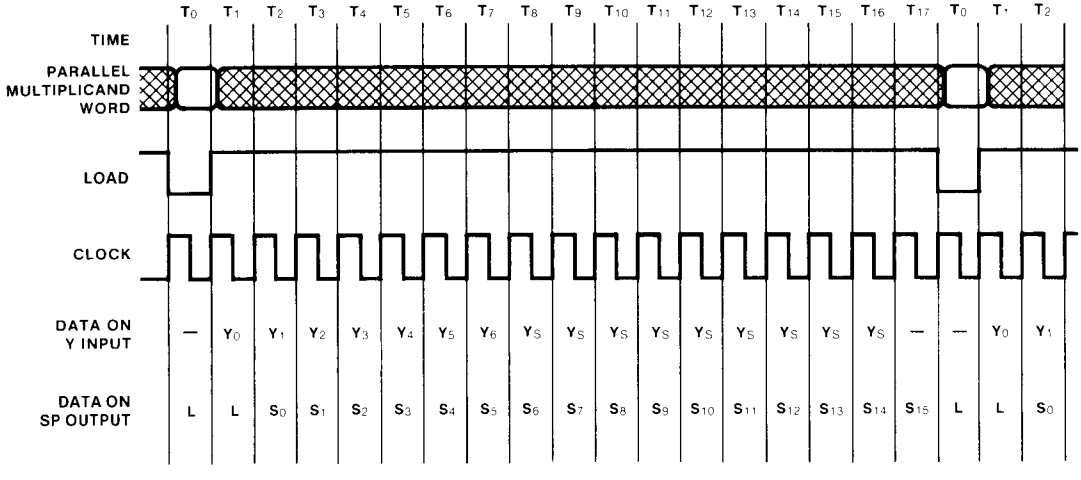


Fig. c 12-Bit by n-Bit Twos Complement Multiplier