T-75-37-07

PRELIMINARY SPECIFICATION MHS SEPTEMBER 1988

DATA SHEET 29C42

MNP, V42 PROTOCOL CONTROLLER

MAIN FEATURES

- FULLY CONFORMS TO NEW CCITT V42 SPEC
- SUPPORTS LAP M AND MNP PROTOCOLS
- PERFORMS ASYNCHRONOUS TO SYNCHRONOUS CONVERSION
- SUPPORTS DATA FLOW UP TO 64KB/S
- FULL DUPLEX SERIAL (V24/RS232C) TO PARALLEL INTERFACE
- DIRECTLY COMPATIBLE WITH 80C51 MICROCONTROLLER
- PROVIDES AN EXTRA 8 BIT INPUT PORT
- FULL CMOS DEVICE

CONTENTS

1 REFERENCES

CCITT V42 DRAFT SPECIFICATIONS TEMPORARY DOCUMENT 80-E

2 GENERAL DESCRIPTION

The 29C42 is a powerful interface circuit which allows to build several types of data transmission equipment requiring ERROR CORRECTION capability for modems using asynchronous to synchronous conversion.

Applications include regular or baseband modems, ISDN terminal adaptors, and industrial networks. See *figure 1* for regular error correction DCE.

All three modes of the CCITT V42 recommendation are implemented:

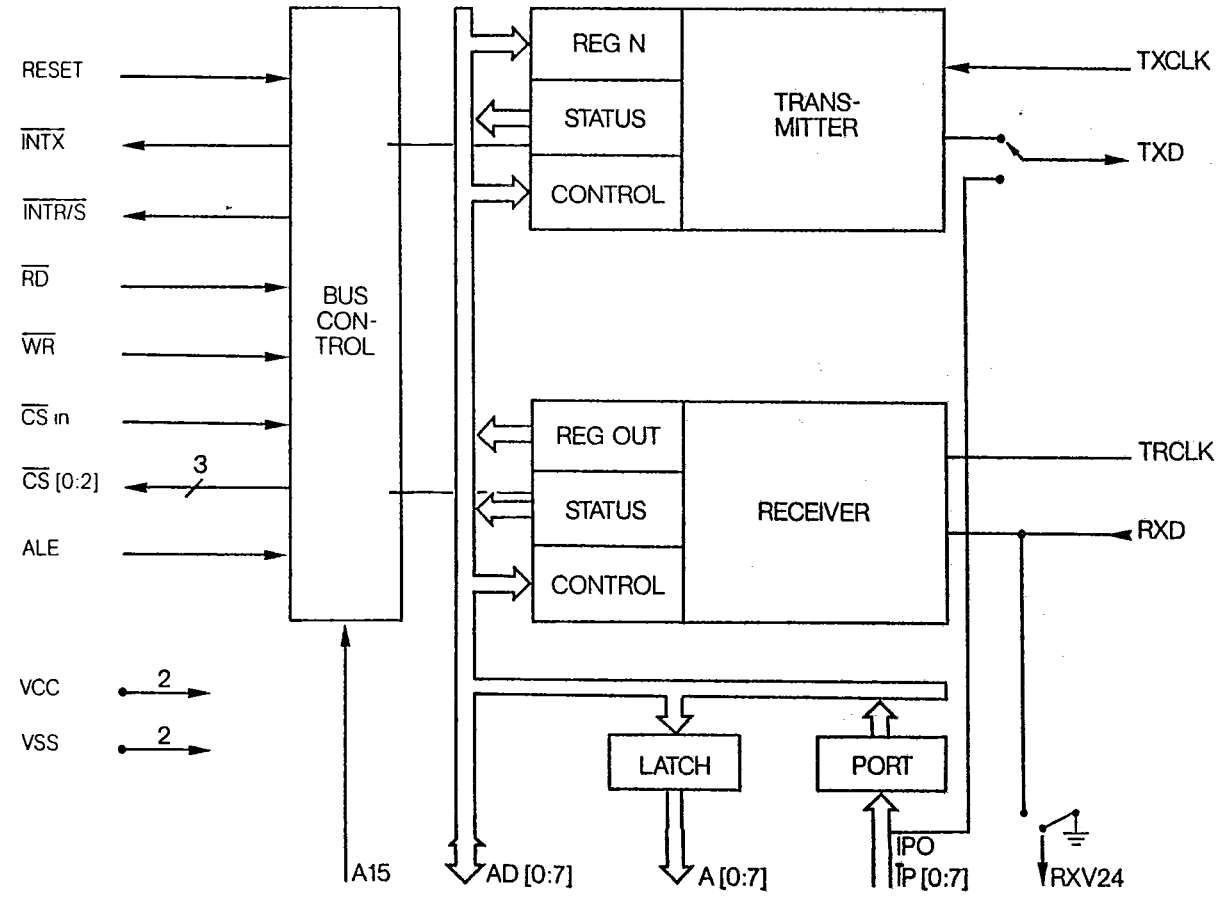
- 10 moments (start/7 bit with parity/stop) or (start/8 bit without parity/stop) ASYNCHRONOUS mode used during the detection phase and communication with a distant modem which does not support error correction.
- Byte oriented framing used during handshake and communication when V42 error correction scheme applies. This mode is available with and without start/stop encapsulation.
- Bit oriented framing mode (HDLC) used during communication when V42 error correction scheme applies.

The 29C42 is a microprocessor or microcontroller peripheral device. The transmit and receive sections have separate transmit and receive clocks supplied by the modem. The micro processor interface is fully asynchronous, consequently no special chip clock (no crystal) is required.

The device integrates bus demultiplexing for 80C51 family microcontrollers, and provides three chip select controls.

Error correcting DCE

29C42 Block Diagram



3 MAIN CONTROL BLOCK

The main control block includes the internal MODE, CONTROL, STATUS registers and the INTERRUPT logic.

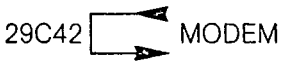
3.1 Mode Register

MODE R/W @ 08H RESET=00H

IT2	IT1	IT0	TRV	T1	MR2	MR1	MR0

MR [2, 1, 0] : Serial channel mode selection
- 0 0 0 : ASYNC 7 bit + parity
- 0 1 0 : ASYNC 8 bit
- 0 0 1 : Octet oriented SYNC mode with start stop encapsulation
- 1 0 0 : Octet oriented SYNC mode without start stop encapsulation
- 0 1 1 : Bit oriented SYNC mode (HDLC)
- 1 0 1 : not used
- 1 1 0 : not used
- 1 1 1 : not used

T1 : Enable Loop back towards modem



TRV : Enable transparent mode
IT0 : Transmit interrupt mask
IT1 : Receive interrupt mask
IT2 : Status interrupt mask

In transparent V24 mode (TRV=1) the bit IP0 from the input port is routed to output TXD. The specific RXV24 output reflects the RXD input.

3.2 Control Register

The control register is used to enable the transmit and receive channels and to control break transmission.

CTRL R/W @ 09H RESET=00H

*	*	*	*	LBR	SBR	TEN	REN

REN : Receive channel enable
TEN : Transmit channel enable
SBR : Send short BREAK (24 bit at 0 in ASYNC mode)
LBR : Send long BREAK (continuous 0 in ASYNC mode)

TEN bit allows to abort control in HDLC mode. Clearing TEN during a transmission will force the transmit block to send continuous "ones". If TEN bit is returned to one immediately, the 29C42 will insure that 8 ones are transmitted anyway, resulting in a true abort.

REN bit must be used to disable the receive path.

3.3 Transmit Status Register

TSR R @ 0AH RESET=00H

*	*	*	*	END	FLG	SBC	TXE

TXE : Transmit buffer empty
SBC : Short BREAK completed
FLG : start of closing flag transmission in HDLC or Byte SYNC modes
END : end of closing flag transmission in HDLC or Byte SYNC modes

TXE bit is set once the transmit buffer is empty. If the transmit interrupt is not masked, ITXb output is activated. Writing in the transmit buffer TXBUF clears bit TXE and interrupt output ITXb.

SBC status reports that a short break (24 bit=0) has been sent. SBR bit in the control register is automatically cleared once SBC rised. SBC bit does not produce interrupt. SBC is cleared by a write in the transmit buffer TXBUF.

In SYNC modes (BYTE and BIT oriented modes), the frames are automatically closed with the closing sequence once the circuit attempts to read an empty TXBUF.

FLG and END are status that do not produce interrupts. FLG is set when a closing flag transmission start in HDLC. END is set once the closing flag transmission is completed. Both are cleared once a new byte is written in the transmit buffer TXBUF. In byte SYNC mode, FLG status is set when transmission of the closing sequence DLE byte starts, END status rised when the CRC word transmission is completed.

The easiest way to proceed in HDLC mode, is to mask the transmit interrupt once the last byte of a frame has been written in TXBUF, then wait for FLG to be rised it one wants to implement a "shared opening flag/closing flag" encapsulation method, or wait until END is rised if one wants to implement a "closing flag/ opening flag" type of frame separation. Additionnally, waiting END to be rised before disabling the transmit channel is a good way to insure that the last frame has been completely transmitted.

In Byte SYNC mode, one can wait until FLG is rised to write the first byte of a new frame in TXBUF, the opening sequence will be automatically inserted. Interframe are filled with idle code FFH.

3.4 Receive Status Register

The receive status is described below. Interrupts are transmitted over $\overline{ITR/S}$ output.

RSR R @0BH RESET=00H

*	G-E	B-E	ABO	OVR	BRE	PAR	RBF

RBF : Receive buffer full
PAR : Parity error in ASYNC
BRE : Break detected in ASYNC (10 successive "O")
OVR : Overrun detected
ABO : Abort detected in BIT SYNC
B-E : CRC error in Bit SYNC mode
CRC error or Bad End of Frame in Byte SYNC mode
Absence of stop bit in ASYNC mode
G-E : Good end of frame in SYNC mode (BYTE or BIT modes)

RBF is set when a new byte is present in the receive buffer RXBUF. Output $\overline{ITR/S}$ is activated if the receive interrupt is not masked. Reading the RXBUF register clears RBF bit and $\overline{ITR/S}$ output.

If the status interrupt is not masked, each time PAR or BRE or OVR or ABO or B-E or G-E, are set, the $\overline{ITR/S}$ output is activated. Reading RSR register will clear both the 7 status bit and the $\overline{ITR/S}$ output.

If a status interrupt appears whille RBF is high, $\overline{ITR/S}$ will not come back to 0 after RXBUF reading, indicating that a status interrupt is also present.

3.5 Transmit and Receive Buffers

TXBUF W @0CH RESET=00H

D7	D6	D5	D4	D3	D2	D1	D0

RXBUF R @0CH RESET=00H

D7	D6	D5	D4	D3	D2	D1	D0

3.6 Input PORT

IP R @0DH RESET=00H

D7	D6	D5	D4	D3	D2	D1	D0

The D0 bit is connected to the TXD output when transparent mode is selected (TRV=1).

3.7 CS PORT

CS R/W @07H RESET=01H

*	*	*	*	*	*	*	$\overline{CS2}$

$\overline{CS2}$ bit is connected to the $\overline{CS2}$ output. It can be used for chip select generation,. Upon reset, it is in the deactivated state.

4 TRANSMIT BLOCK

The transmit block implement the parallel to serial conversion in the ASYNC, BYTE or BIT SYNC modes of the V42 standard.

This block work synchronously with the TXCLK. Bit are sampled on the rising edge of TXCLK input.

In ASYNC modes, the absence of a new character in the transmit buffer cause transmission of repetitive stop bit (bit=1). In SYNC modes, the circuit close the frame accordingly to the selected mode: BYTE or BIT Oriented mode.

In BYTE SYNC mode, when start/stop option is selected, only one start bit and one stop bit are transmitted with each byte. Once the transmit buffer is empty, the circuit close the frame.

When no modes are selected or if the transmit channel is disabled, the TXD output gives a continuous one.

4.1 BIT SYNC Mode

In this mode, the circuit encapsulates frames according to HDLC standard (flag, bit stuffing, CRC). The CCITT polynomial is used. Finally, the circuit conforms to the LAPB standard for interframe filling (filled with flags). Separating frames with one flag is supported by the circuit. If at the end of a closing flag transmission, a new byte is ready in TXBUF, it will be sent directly, the closing flag being also the opening one. If at the end of a closing flag transmission the TXBUF is still empty, the circuit will automatically fill the interframe with flags as recommended in V42 protocol. If one wants to send an abort, it should be done by deselecting the transmit channel. As the circuit maintains a byte alignment internally, the abort sequence will be 8 bit at "one" minimum.

4.2 BYTE SYNC Mode

In this mode, the circuit begins each frame with the opening sequence (SYN/DLE/STX) the special byte values are: SYN=16H, DLE=10H, STX=02H. During transmission, if a DLE byte is detected in TXBUF, it will be transmitted with automatic insertion of an additionnal DLE byte (transparent byte). When no more byte are present in the TXBUF, the circuit will automatically close the frame with the closing sequence (DLE/ETX then the 16 bit CRC word). The ETX byte value is 03 H. The polynomial used for CRC is the one recommended in V42 standard for this mode. The CRC is calculated with all transmitted bytes after SYN/DLE/STX sequence (not included) excepted the transparent DLE. The DLE byte of the closing sequence will not be incorporated in the CRC calculation while the ETX byte will. This fully conforms to the V42 standard for OCTET oriented SYNC mode.

Depending on the selected mode, each byte will or will not be encapsulated with one start bit and one stop bit.

4.3 ASYNC Mode

In this mode, the circuit supports 10 moments ASYNC transmission scheme. Depending on which mode is selected, the circuit will accept 8 bit data or will ignore the MSB of each byte in TXBUF, calculate a parity bit for all 7 other bits and transmit the 7 bits plus the parity bit. Each character will begin with a start bit (0) and be followed by at least one stop bit (1). If no other byte is ready in the TXBUF, the circuit will insert additionnal stop bit, otherwise, it will start a new character immediately.

It is possible to force a short break. In this case the circuit will insert 24 bits at 0. This conforms the 2M + 3 bit at 0 requirement for Break. The transmitter will report the short break completion in the SBC bit of TSR, then return to idle state. If a new byte is ready in TXBUF when the short break transmission is completed, the circuit will transmit a one bit idle (bit = 1) prior to start bit of the new character.

It is also possible to force a permanent break condition (LBR = 1).

5 RECEIVE BLOCK

The receive block achieves the serial to parallel conversion in the ASYNC or SYNC modes. It fully conforms to the V42 standard. This block works synchronously with RXCLK clock input. Bits are sampled on RXCLK falling edges.

5.1 BIT SYNC Mode

In this mode the circuit processes an incoming frame with flag delineation, bit stuffing CRC check (CCITT polynomial).

The circuit supports incoming frames with interframes filled with flags, or a shared closing/opening flag. Moreoever, interframes can also be filled with bit = 1 (idle). In that case it is mandatory to have a separate closing flag before the interframe.

The circuit is capable to support minimum frame with 1 byte + CRC + flag.

If an "abort" (7 bits = 1) is detected after an opening flag, the frame (empty) will be ignored (no EOF report).

Each time a closing flag is detected, a status is generated GOODEOP (G-E) or BADEOP (B-E):

If an abort is detected (7 bits = 1) the circuit starts waiting for a new opening flag and an EOPABORT (ABO) status is reported.

If a new character is to be writen in a full receive buffer RXBUF, an overrun status (OVR) is generated and the circuit will automatically search for the next opening flag.

The following status are generated:

GOODEOP	: G-E	: CRC correct and byte aligned frame
BADEOP	: B-E	: CRC error or non byte aligned frame
ABORT	: ABO	: Abort condition detection
OVERRUN	: OVR	: Overun condition detected

5.2 BYTE SYNC Mode

In this mode the circuit looks for a starting sequence STX/DLE/SYN. Once recognized, following byte are sent over RXBUF except transparent DLE. If a closing sequence is recognized (DLE/ETX), a CRC (V42 polynomial) is calculated and compared with the next 2 bytes. A status is reported with good or bad CRC. The CRC computation fully conforms to the V42 standard.

If the circuit detects a sequence of DLE followed by a byte which is not ETX or STX or DLE, an error is assumed and BADEOP status is reported (B-E). In that case the receiver automatically returns to the search for opening flag state.

If a new character is to be written in a full receive buffer RXBUF, an overrun status (OVR) is generated and the circuit will automatically search for the next opening flag.

Depending of the selected mode, the circuit automatically removes from the flow the start and stop bits. If start/stop encapsulation mode is selected, the receiver will assume that each character are

encapsulated with one start and one stop bit. If a fail occurs on encapsulation (ex no stop) the receiver will report a BADEOP status and return to the search for opening flag state.

The following status are generated:

GOODEOP	: G-E	: CRC correct
BADEOP	: B-E	: CRC error or bad DLE sequence or bad start stop encapsulation (if this mode is selected)
OVERRUN	: OVR	: Overrun condition detected

5.3 ASYNC Mode

A 10 moments mode is supported. Each character should have one start bit and at least one stop bit. Stop bit suppression is not supported.

2 submodes are supported:
- ASYNC 7 bit + parity
- ASYNC 8 bit

The circuit recognizes a break with one start bit, one byte at 00 H and a stop bit violation (bit = 0). If a break is detected, the circuit will then wait for a new 10 moment character with valid start/stop.

If the circuit recognizes a stop bit suppression, an error message will be generated (B-E) and the circuit will search for a new 10 moment character with valid start/stop.

If a new character is to be written in a full receive buffer RXBUF, an overrun status (OVR) is generated and the circuit will automatically search for the next opening flag.

The circuit generates the following status

BREAK	: BRE	: break detection (10 bit at 0)
BAD-PARITY	: PAR	: parity error if "7 bit + parity" mode is chosen
STOP BIT ERROR	: B-E	: detection of a suppressed stop bit
OVERRUN	: OVR	: detection of overrun condition

6 INTERFACE BLOCK

This block supports the bus demultiplexing function using ALE input, reset function, $\overline{ITX}$ and $\overline{ITR/S}$ management and the Chip Select management using:

$\overline{CSin}$	: inverted Chip Select input
ADR15	: Address bit 15
ADR0..7	: Address low significant byte
$\overline{RD}$	: Inverted READ strobe
$\overline{WR}$	: Inverted WRITE strobe

The chip select equation are given below:

Internal registers selection : select = A15*CSin*not A7*(Read + Write)
Selection for $\overline{CS0}$ output : select = not A15*(Read + Write)
Selection for $\overline{CS1}$ output : select = A15*CSin*A7*(Read + Write)

INPUT			OUTPUT		COMMENTS
$\overline{CSin}$	A15	A7	$\overline{CS0}$	$\overline{CS1}$	
0	1	0	1	1	29C42 int. Reg select
0	1	1	1	0	peripheral CS ex modem
X	0	X	0	1	CS for 32 Kbyte RAM

Application example with 80C51 + 29C42 + 32 Kbyte RAM + MODEM:

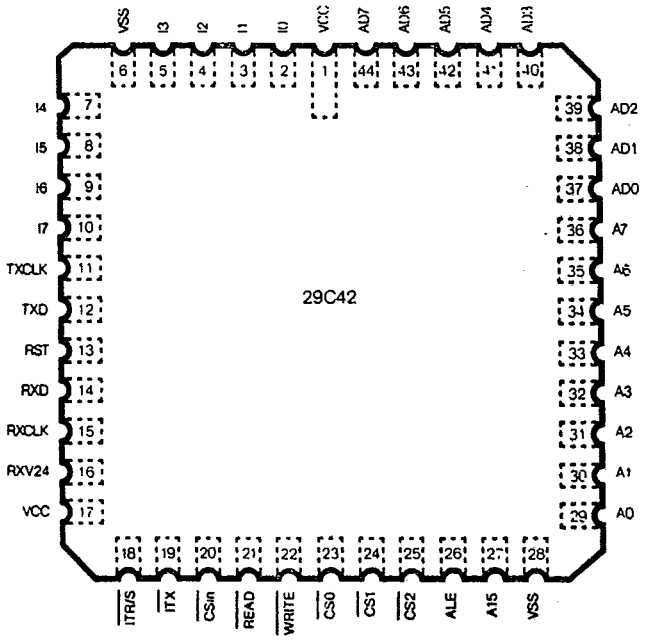
External Address decoder on A8 to A14 should be used to define in the upper 32 Kbyte of the memory map an area reserved for 29C42 and MODEM registers.

7 PIN DESCRIPTION

The 29C42 is housed in a 44 pin PLCC package. The PINOUT and a short description is given below:

NAME	PIN	TYPE	DESCRIPTION
ALE	26	in	Address latch enable
$\overline{RD}$	21	in	Not READ
$\overline{WR}$	22	in	Not WRITE
$\overline{CSin}$	20	in	Chip Select input
$\overline{ITX}$	19	out	Transmit Interrupt active low
$\overline{ITR/S}$	18	out	Receive and status Interrupt active low
Reset	13	in	General Reset
RXV24	16	out	RXDout in transparent mode
IP0:3	2 to 5	in	Input port low nibble
IP4:7	7 to 10	in	Input port high nibble
RXCLK	15	in	Receive clock
TXCLK	11	in	Transmit clock
RXD	14	in	Receive data
TXD	12	out	Transmit data
$\overline{CS2}$	25	out	Not chip select2
$\overline{CS1}$	24	out	Not chip select1
$\overline{CS0}$	23	out	Not chip select0
AD0:7	37/44	I/O	Multiplexed address low and data
A0:7	29/36	out	Demultiplexed address low
A15	27	in	MSB of 16 bit address
VCC	1 & 17	supply	+5 volts
VSS	6 & 28	supply	Ground

PLCC 28 pin out top view



8 ABSOLUTE MAXIMUM RATING

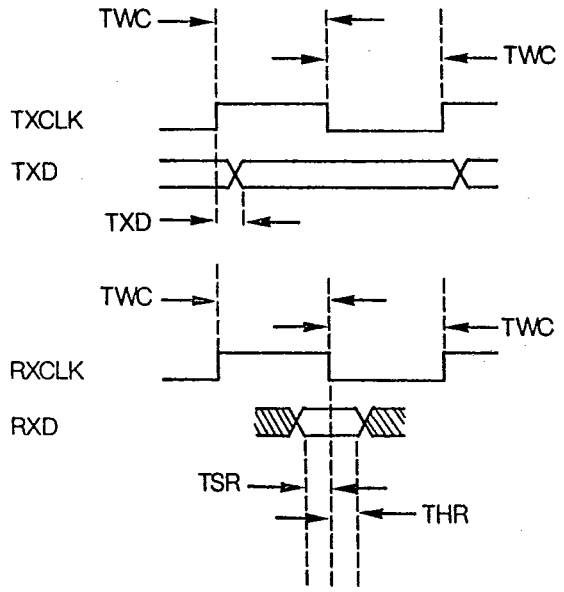
Ambiant temperature : 0 to 70 degree celsius
Storage temperature : −65 to 125 degree celsius
Voltage at any pin with respect to ground : −0.4 volt to VCC + 0.4 volt

9 DC CHARACTERISTICS

VIL : input low voltage : 0.8 volt max
VIH : input high voltage : 2.0 volt min
VOL : output low voltage : 0.45 volt max (IOL=2.4 mA)
VOH : output high voltage : 2.4 volt min (IOH=60µA)
ICC : power supply current : mA
ILI : input leakage current : µA
ILO : output leakage current : µA

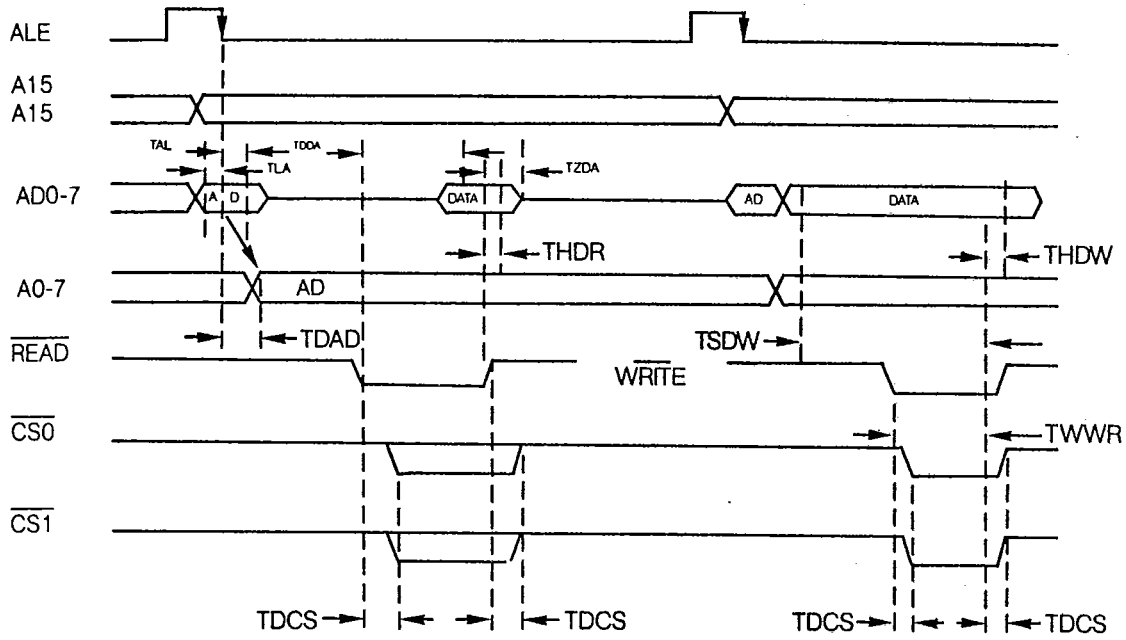
10 AC CHARACTERISTICS

Modem Interface



TWC	TXCLK, RXCLK high or low min width	TSR	Setup data to RXCLK
TXD	Delay time TXCLK to valid data	THR	Hold data from RXCLK

Micro Controller Bus Timing

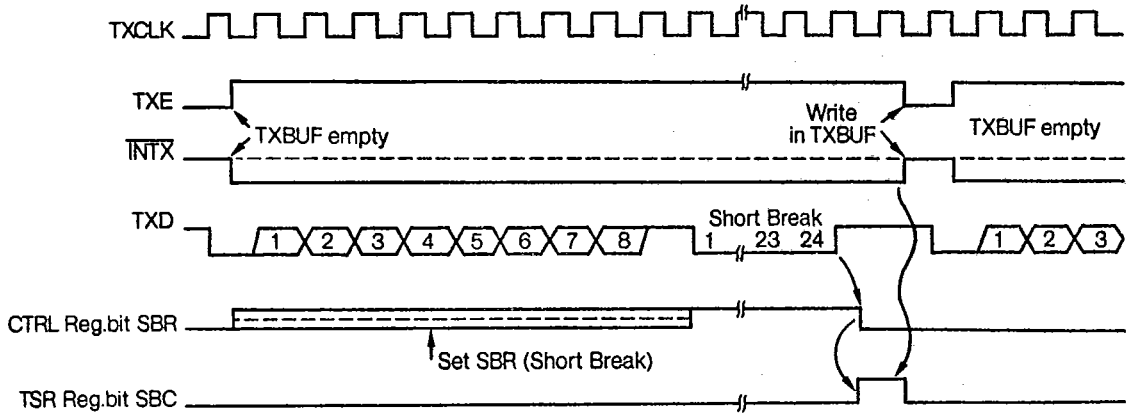


TDAD	Delay	ALE to address valid	TWWR	Minimum	Write pulse
TDDA	Delay	Read strobe to valid data	TSDW	Setup	Data to write strobe
THDR	Hold	Valid data from read strobe	THDW	Hold	Valid data from write strobe
TZDA	Delay	Read strobe to data tri-state	TAL	Setup	Address to ALE
TDCS	Delay	Read/Write to $\overline{CS}$	TLA	Hold	Address from ALE

11 TIMINGS

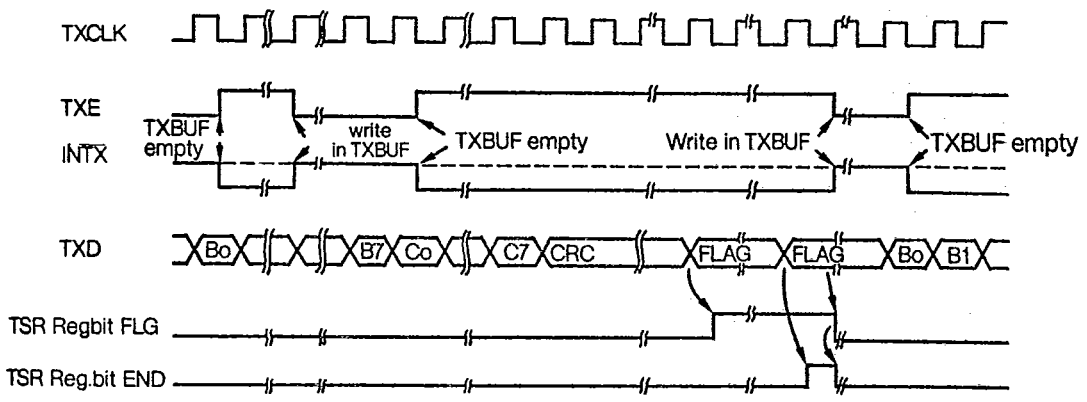
Following figures give the transmitter and receiver timings in the different modes of programmation and under different exception conditions.

TRANSMIT ASYNC MODE



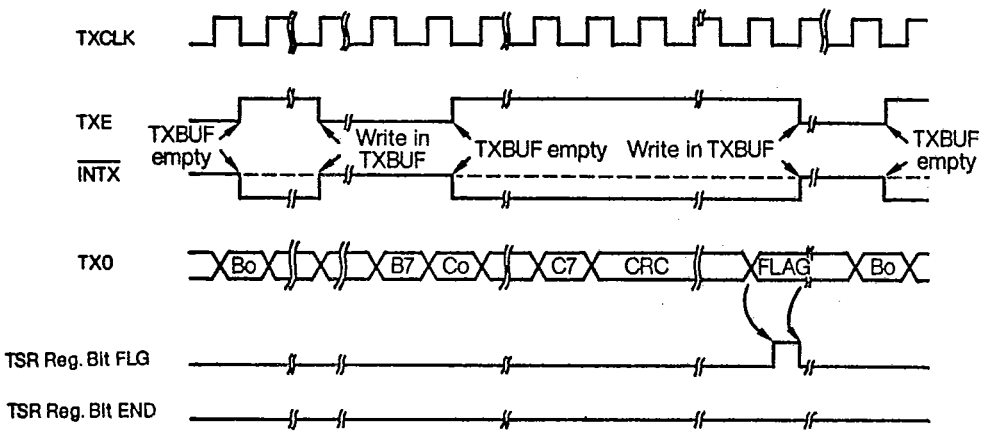
- TXE = 1 and $\overline{INTX}$ is active to ask For Byte n during start Bit of Byte n−1 transmission.
- Not represented is long Break (continuous 0) and idle.
- Doted line on $\overline{INTX}$ if masked.

TRANSMIT HDLC MODE



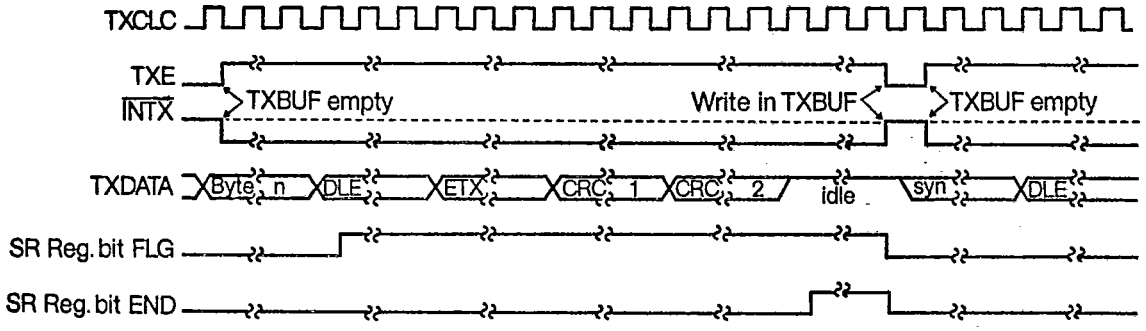
- TXE = 1 and $\overline{INTX}$ is active to ask for Byte n during First of bit of Byte n−1 transmission.
- TXBUF is still empty when Byte C MSB transmission ends. A closing sequence is inserted after.
- Not represented is Abort and return to idle.
- Doted line on $\overline{INTX}$ if masked.

TRANSMIT HDLC MODE



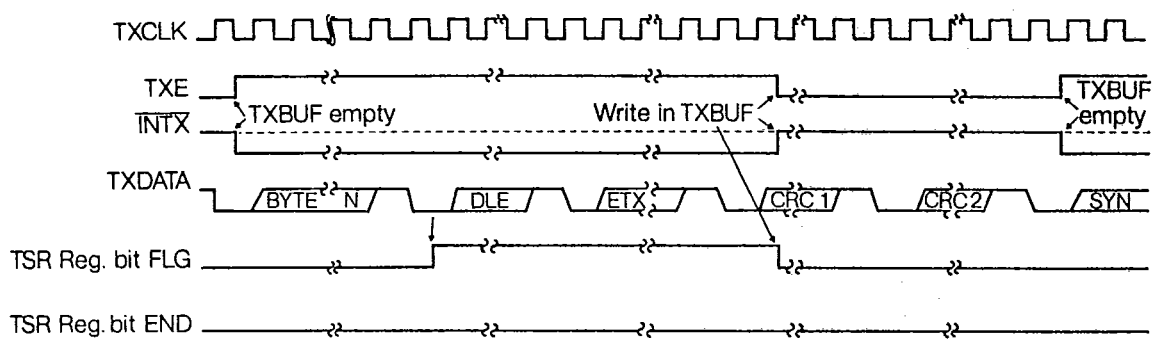
- TXE = 1 and $\overline{INTX}$ is active to ask for Byte n during first bit of Byte n−1 transmission.
- TXBUF is still empty when Byte C MSB transmission ends. A closing sequence is inserted after.
- TXBUF is filled during closing Flag transmission, closing Flag/opening Flag sharing occurs.
- Doted line on $\overline{INTX}$ if masked.

Transmit Byte Sync Mode No Start/Stop



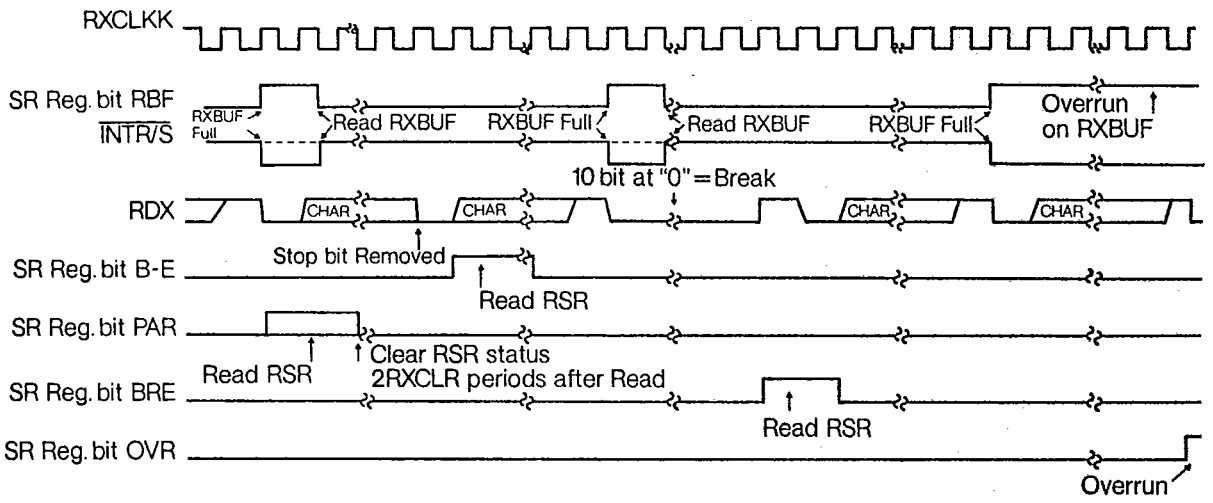
- TXE = 1 and $\overline{INTX}$ active to ask for Byte N during First bit of Byte N−1 transmission.
- Doted line on $\overline{INTX}$ if masked.
- TXBUF is still empty when Byte N transmission ends. A closing sequence is inserted after.
- Filling of TXBUF with First Byte of a new Frame delayed, an idle period occurs.

Transmit Byte Sync Mode With Start/Stop



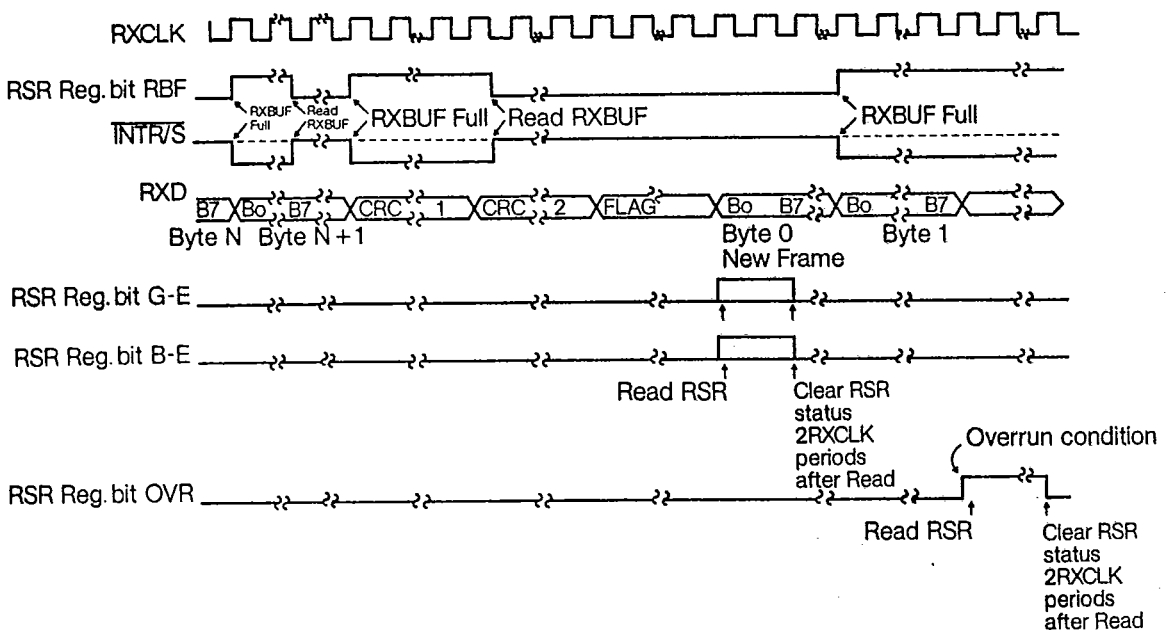
- TXE = 1 and $\overline{INTX}$ active to ask for Byte n during start bit of Byte n–1 transmission.
- Doted line on $\overline{INTX}$ if masked.
- TXBUF is still empty when Byte N transmission ends. A closing sequence is inserted after.

Receiver Async Mode



- Doted line on $\overline{INTR/S}$ if masked.

Receiver HDLC Mode



- Not represented is Abort detection (Same behaviour as B-E/G-E)
- Doted line on $\overline{INTR/S}$ if masked.

12 REGISTER AND CHIP SELECT MAPPING

The following table gives the register mapping and the memory map selected by CS0b and CS1b strobes.

8XFFH 8X80H	selected by $\overline{CS1}$
8X7FH 8X10H	reserved
8X0FH	reserved
8X0EH	reserved
8X0DH	IP
8X0CH	TXBUF/RXBUF
8X0BH	RSR
8X0AH	TSR
8X09H	CTRL
8X08H	MODE
8X07H	CS register
8X06H 8X00H	reserved
7FFFH 0000H	selected by $\overline{CS0}$

$\overline{CSin}$ input must be used to define an exact mapping for registers and $\overline{CS1}$ memory map (define X value).

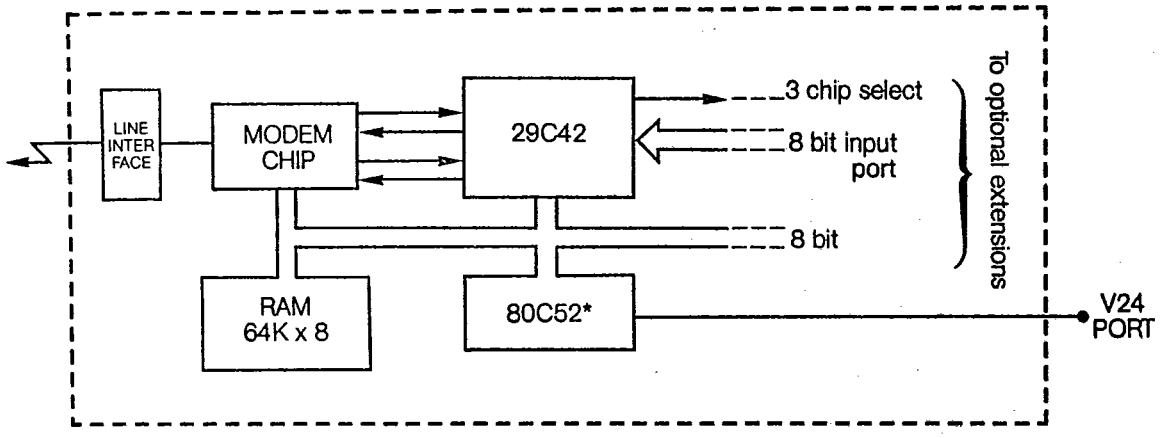
13 APPLICATION

Typical MODEM application including error correction procedure with asynchronous to synchronous conversion is implemented with a limited number of circuits.

The MODEM chip performs A/D and D/A conversion.

The 29C42 chip achieves the lower part of V42 protocol layer 2, while the 80C52 and its associated firmware manages the upper part of V42 protocol layer 2 plus layer 3 and upper.

Modem Application



*80C52 = 8 Kbyte ROM, 256 byte RAM, 3 timers. 83C154 (16 Kbyte ROM) or 80C58 (32 Kb) can also be used.