ISD ChipCorder®
ISD2100 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The ISD2100 is a digital ChipCorder® providing single-chip storage and playback of high quality audio. The device features digital de-compression, comprehensive memory management, flash storage, and integrated audio signal path and Class D speaker driver capable of delivering power of 400mW. This family utilizes flash memory to provide non-volatile audio playback with duration up to 30 seconds (based on 8kHz/4bit ADPCM compression) for a single-chip audio playback solution.

The ISD2100 can be controlled and programmed through an SPI serial interface or operated stand-alone by triggers applied to the device's six GPIO pins.

The ISD2100 requires no external clock sources or components except a speaker to deliver quality audio prompts or sound effects to enhance user interfaces.

In addition, the part can provide non-volatile flash storage in 1Kbyte sectors eliminating the need for additional serial EEPROM/Flash devices.

ISD2100 provides wide range of sampling frequencies, high SNR performance, low power consumption, fast programming time and integrated program verification.

2 FEATURES

- Duration
  - **ISD2130 –** 30 seconds based on 8kHz/4bit ADPCM in 1Mbit of flash storage
  - **ISD2115A** – 15 seconds based on 8kHz/4bit ADPCM in 1Mbit of flash storage
- Audio Management
  - Store pre-recorded audio (**Voice Prompts**) using high quality digital compression
  - Use simple index based command for playback – no address needed.
  - Execute pre-programmed macro scripts (**Voice Macros**) designed to control the configuration of the device and playback Voice Prompts sequences.
- Control
  - Serial SPI interface for microprocessor control and programming.
  - Stand-alone control where customized Voice Macro scripts are assigned to GPIO trigger pins.
- Sample Rate
  - 7 sampling frequencies 4, 5.3, 6.4, 8, 12.8, 16 and 32 kHz are available.
  - Each Voice Prompt can have optimal sample rate.
- Compression Algorithms
  - µ-Law: 6, 7 or 8 bits per sample
  - Differential µ-Law: 6, 7 or 8 bits per sample
  - PCM: 8, 10 or 12 bits per sample
  - Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
  - Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
  - Internal oscillator with internal reference: factory trimmed to ±1% deviation at room temperature.
- Output
  - PWM: Class D speaker driver to direct drive an 8Ω speaker or buzzer.
  - Delivers 400mW at 3V supply.
- I/Os
  - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
  - 6 general purpose I/O pins multiplexed with SPI interface.
- Flash Storage

  - 1Mbit (ISD2130) or 512Kbit (ISD2115A) of storage for combined audio/data.
  - Fast programming time (20µs/byte)
  - Erase sector size 1Kbyte, sector erase time 2ms.
  - Integrated memory checksum calculation for fast verification.
  - Endurance >100K cycles. Retention > 10 years
- Operating Voltage: 2.7-3.6V
- Package:
  - green, 20L-QFN, 14L-SOP
- Temperature Options:
  - Industrial: -40°C to 85°C

3 LOCK DIAGRAM

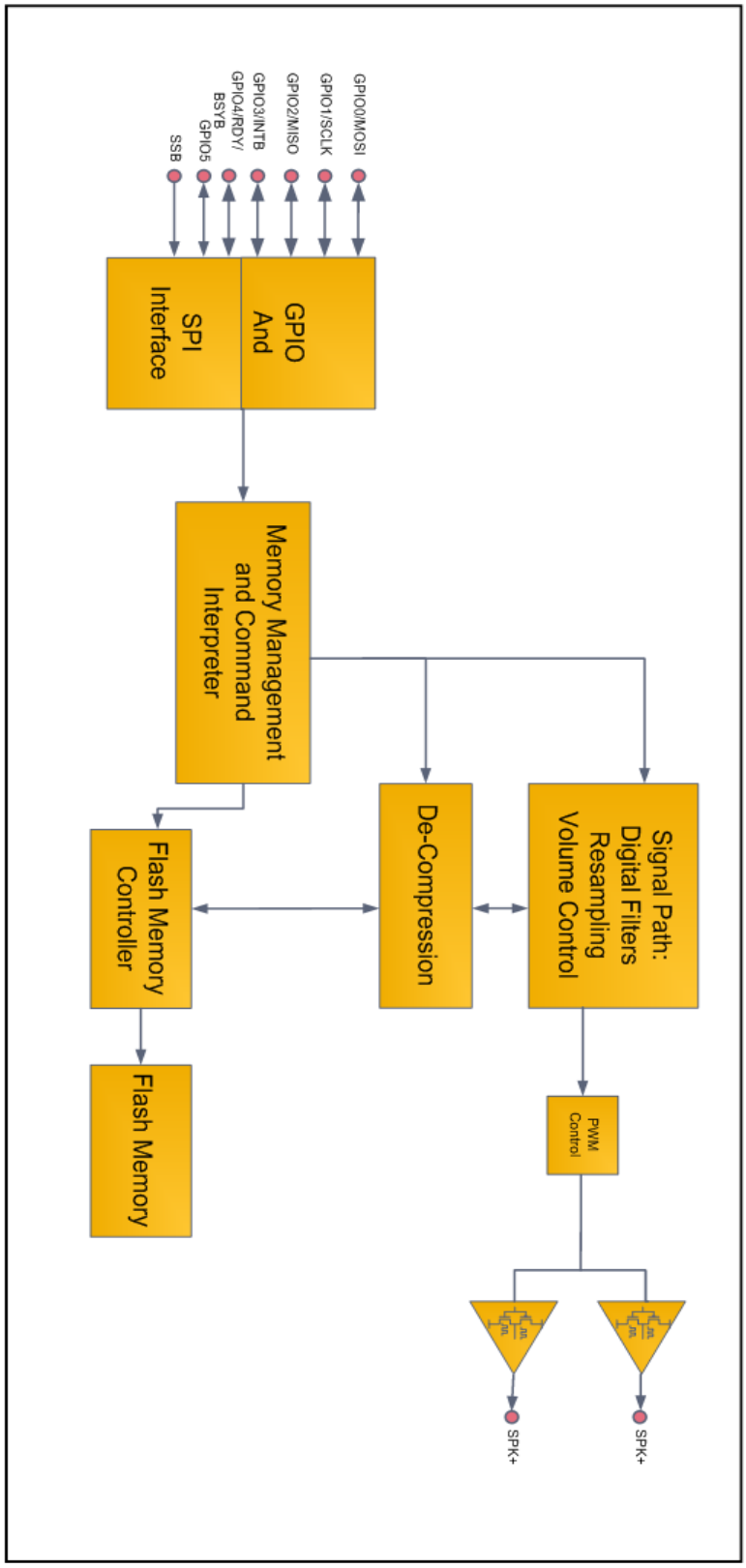


Figure 3-1 ISD2100 Block Diagram

4 PINOUT CONFIGURATION

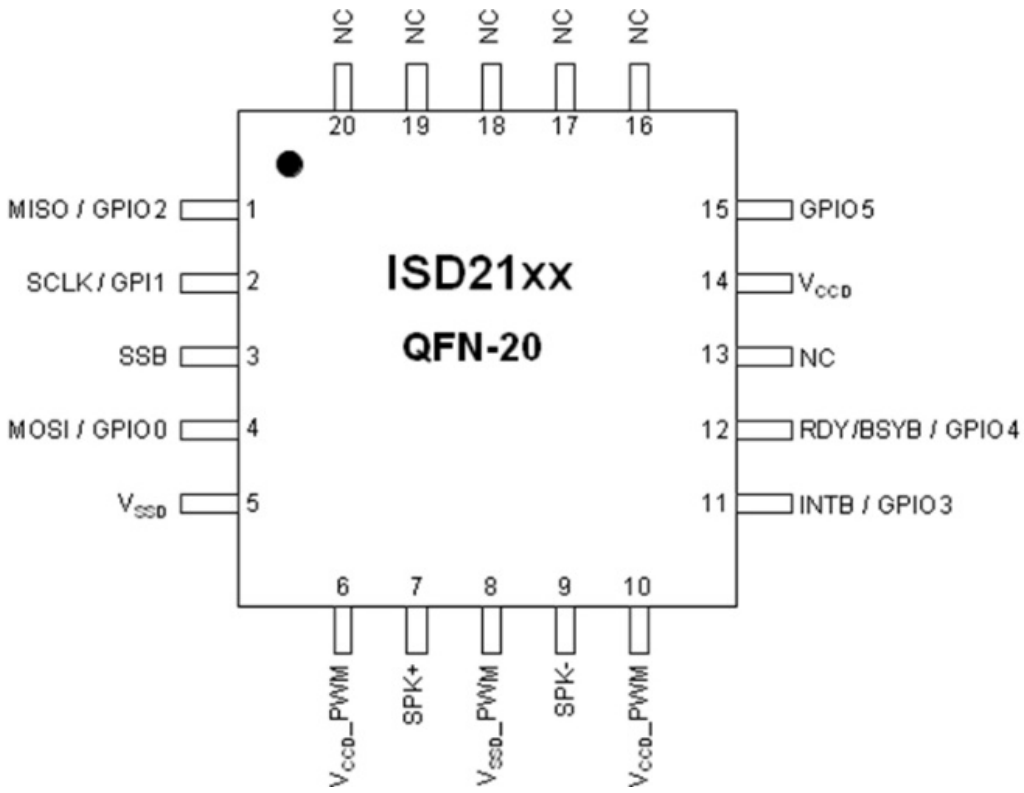


Figure 4-1 ISD2100 20-Lead QFN Pin Configuration

*Note: the center exposed pad underneath of the QFN20 package is electrically connected to back of the die substrate with GROUND potential; it should be connected to VSSD.

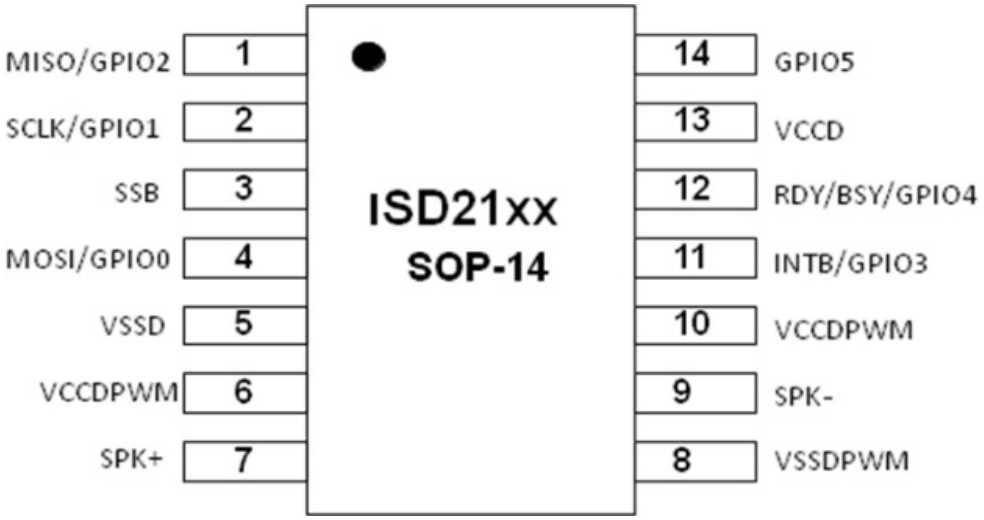


Figure 4-2 ISD2100 SOP14 Pin Configuration

5 PIN DESCRIPTION

ISD2100 QFN20 Pin Configuration

Pin Number	Pin Name	I/O	Function
1	MISO / GPIO2	O	Master-In-Slave-Out. Serial output from the ISD2100 to the host. This pin is in tri-state when SSB=1. Can be configured as a general purpose I/O pin.
2	SCLK / GPI1	I	Serial Clock input to the ISD2100 from the host. Can be configured as a general purpose input pin.
3	SSB	I	Slave Select input to the ISD2100 from the host. When SSB is low device is selected and responds to commands on the SPI interface. When asserted, GPIO0/1/2 automatically configure to MOSI/SCLK and MISO respectively. SSB has an internal pull-up to Vccd.
4	MOSI / GPIO0	I	Master-Out-Slave-In. Serial input to the ISD2100 from the host. Can be configured as a general purpose I/O pin.
5	V_{SSD}	I	Digital Ground.
6	V_{CCD}_PWM	I	Digital Power for the PWM Driver. It can be from a separate different power supply other than V_{CCD}.
7	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tri-state.
8	V_{SSD}_PWM	I	Digital Ground for the PWM Driver.
9	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tri-state.
10	V_{CCD}_PWM	I	Digital Power for the PWM Driver. It can be from a separate different power supply other than V_{CCD}.
11	INTB / GPIO3	O	Active low interrupt request pin. This pin is an open-drain output. Can be configured as a general purpose I/O pin.
12	RDY/BSYB / GPIO4	O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD2100 is ready to accept new SPI commands or data. Can be configured as a general purpose I/O pin.

Pin Number	Pin Name	I/O	Function
13	NC		This pin should be left unconnected.
14	V_{CCD}	I	Digital Power. It can be from a separate different power supply other than V_{CCD}_PWM.
15	GPIO5	I/O	General purpose I/O pin
16	NC		This pin should be left unconnected.
17	NC		This pin should be left unconnected.
18	NC		This pin should be left unconnected.
19	NC		This pin should be left unconnected.
20	NC		This pin should be left unconnected.
21	Center pad	I	The center pad underneath should be connected to Digital Ground V_{SSD}. Please avoid placement of exposed vias under this pad.

ISD2100 SOP14 Pin Configuration

Pin Number	Pin Name	I/O	Function
1	MISO / GPIO2	O	Master-In-Slave-Out. Serial output from the ISD2100 to the host. This pin is in tri-state when SSB=1. Can be configured as a general purpose I/O pin.
2	SCLK / GPI1	I	Serial Clock input to the ISD2100 from the host. Can be configured as a general purpose input pin.
3	SSB	I	Slave Select input to the ISD2100 from the host. When SSB is low device is selected and responds to commands on the SPI interface. When asserted, GPIO0/1/2 automatically configure to MOSI/SCLK and MISO respectively. SSB has an internal pull-up to Vccd.
4	MOSI / GPIO0	I	Master-Out-Slave-In. Serial input to the ISD2100 from the host. Can be configured as a general purpose I/O pin.
5	V_{SSD}	I	Digital Ground.
6	V_{CCD}_PWM	I	Digital Power for the PWM Driver.

Pin Number	Pin Name	I/O	Function
7	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tri-state.
8	V_{SSD}_PWM	I	Digital Ground for the PWM Driver.
9	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tri-state.
10	V_{CCD}_PWM	I	Digital Power for the PWM Driver.
11	INTB / GPIO3	O	Active low interrupt request pin. This pin is an open-drain output. Can be configured as a general purpose I/O pin.
12	RDY/BSYB / GPIO4	O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD2100 is ready to accept new SPI commands or data. Can be configured as a general purpose I/O pin.
13	V_{CCD}	I	Digital Power.
14	GPIO5	I/O	General purpose I/O pin

6 DEVICE OPERATION

Playback of audio stored on the ISD2100 can be accomplished by either sending SPI commands via the serial interface or triggered by signal edges applied to GPIO pins. The device is programmed via the SPI interface either in-system or utilizing commercially available gang programmers.

6.1 AUDIO STORAGE

The audio compression and customization of the ISD2100 is rapidly achieved with the supplied ISD2100VPE or Voice Prompt Editor. This software tool allows the developer to take audio clips in standard wave file format and re-sample and compress them for download to the ISD2100.

Audio is stored in the ISD2100 as series of **Voice Prompts**: these units of audio can be of any length – the compression and sample rate of each Voice Prompt can be individually selected. A powerful feature of the ISD2100 is presence of a scripting ability **Voice Macros**. A Voice Macro can contain commands to play individual Voice Prompts and configure the ISD2100. A Voice Macro can be associated with a GPIO pin such that it is triggered by a transition on that pin. In this way stand-alone systems can be developed without the need for micro-controller interaction. Voice Macros can also be executed via the SPI command interface. Both Voice Prompts and Voice Macros are addressed via a simple sequential index address, no absolute memory address is required, thus audio source material or voice macro function can be updated (or changed for multi-language implementation) without the need to update microcontroller code.

6.2 DEVICE CONFIGURATION

The ISD2100 is configured by writing to a set of configuration registers. This can be accomplished either by sending configuration via the serial SPI interface or executing Voice Macros containing configuration commands. Most configuration registers are reset to their default values when the device is powered down to ensure lowest possible standby current. Exceptions to this are registers that control the configuration of GPIO pins and Jump registers that contain the Voice Macro index to execute for GPIO triggers. Configuration registers may be initialized automatically in customizable Voice Macros that are executed on a power-on reset or power-up condition. Section **Error! Reference source not found.** contains a complete list of all configuration registers in the device.

6.3 GPIO CONFIGURATION

The six GPIO pins of the ISD2100 can be configured for a variety of purposes. Each pin can be configured to trigger a Voice Macro function. Each pin also has an alternate function allowing the pins to be configured as SPI, interrupt or oscillator reference pins.

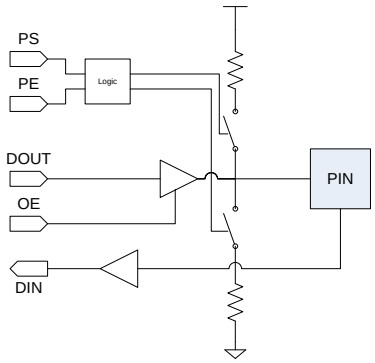


Figure 6-1 GPIO Structure

The structure of the GPIO pads is shown in Figure 6-1. Configuration registers allow the user to control pull-up and pull down resistors, enable the pin as an output or set the output value. See ISD2100 Design Guide for details on the configuration options.

6.4 OSCILLATOR AND SAMPLE RATES

The ISD2100 has an internal oscillator trimmed at manufacturing that requires no external components to operate. This oscillator provides an internal clock source that operates the ISD2100 at a maximum audio sample rate F_{Smax} of 32kHz. The sample rates available for audio storage at this maximum sample rate are shown in Table 6-1. The sample rate is selected during compression using the ISD2100 Voice Prompt Editor software.

Table 6-1 Available Sample Rates.

SR[2:0]	Ratio to F_{Smax}	Sample Rate F_S (kHz)
0	8	4
1	6	5.44
2	5	6.4
3	4	8
4	2.5	12.8
5	2	16
6	1	32

7 MEMORY FORMAT

The memory of the ISD2100 consists of byte addressable flash memory that is erasable in 1Kbyte sectors. Erased memory has a value of 0xFF. Writing to the memory allows host to change bits from erased '1' state to programmed '0' state.

The memory of the ISD2100 is organized into four distinct regions as shown in Figure 7-1. The four regions are:

1. **Configuration and Index Table**: The first region of memory contains configuration data for the device and the index table that points to the Voice Prompt and Voice Macro data. The ISD2100VPE creates this section for download to the device.
2. **Voice Macros**: This section contains the script code of all the projects Voice Macros.
3. **Voice Prompts**: This section contains the compressed audio data for all Voice Prompts.
4. **User Data**: An optional section containing memory sectors allocated by the developer for generic use by the host controller.

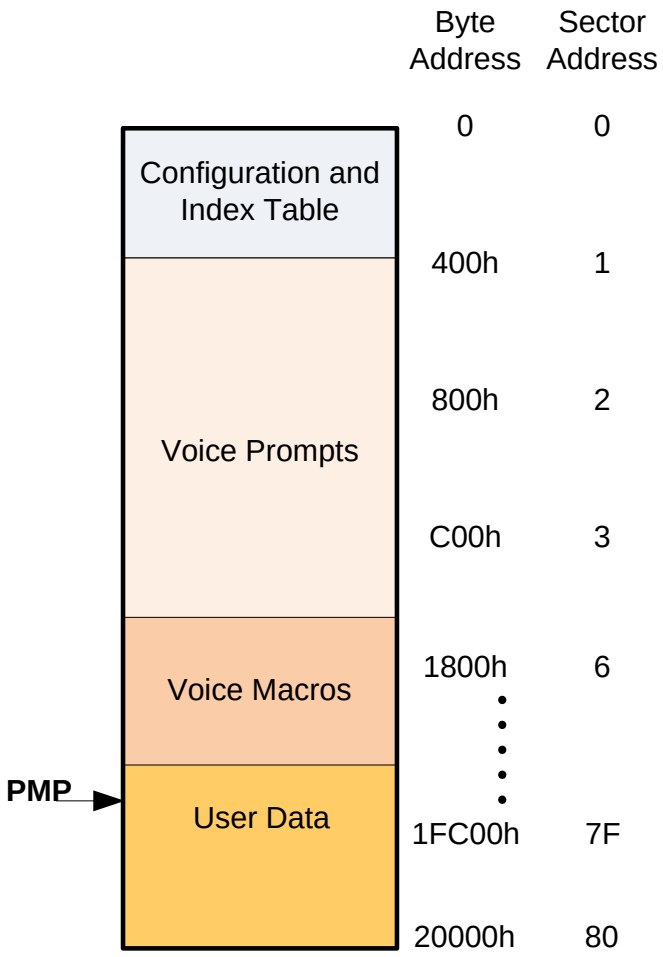


Figure 7-1 ISD2100 Memory Organization

7.1.1 Voice Prompts

Voice prompts are pre-recorded audio of any length, from short words, phrases or sound effects to long passages of music. These Voice Prompts can be played back in any order as determined by the application. A Voice Prompt consists of two components:

1. An index entry in the Index Table pointing to the pre-recorded audio.
2. Compressed pre-recorded audio data.

A Voice Prompt is addressed using its index number to locate and play the pre-recorded audio. This address free approach allows users to easily manage the pre-recorded audio without the need to update the code on the host controller. In addition, the users can store a multitude of pre-recorded audio without the overhead of maintaining a complicated lookup table. To assist customers in creating the Voice Prompts, ISD2100 Voice Prompt Editor and writer are available for development purposes.

7.1.2 Voice Macros

Voice Macros are a script that allows users to customize their own play patterns such as play Voice Prompts, insert silence, power-down the device and configure the signal path, including volume control. Voice Macros are executed using a single SPI command and are accessed using the same index structure as Voice Prompts. This means that a Voice Macro (or Voice Prompt) can be updated on the ISD2100 without the need to update code on the host micro-controller since absolute addresses are not needed.

The following locations have been reserved for special Voice Macros:

Index 0: Power-On Initialization (POI)

Index 1: Power-Up (PU)

Index 2: GPIO-Wakeup (WAKEUP)

These Voice Macros allow the users to customize the ISD2100 power-on, power-up and GPIO wake-up procedures and are executed automatically when utilized. If these Voice Macros are not used device will perform default operations on these events.

An example to illustrate the usage of the PU Voice Macro is:

- WR_CFG(VOLC, 0x0C) ; Set VOLC to 0x0C
- WR_CFG(REG2, 0x44) ; Set REG2 to 0x44
- WR_CFG (REG_GPIO_AF1 ,0xFF); Set REG_GPIO_AF1 to 0xFF
- WR_CFG (REG_GPIO_AF0 ,0x10) ; Set REG_GPIO_AF0 to 0x10
- FINISH ; Exit Voice Macro

The above PU Voice Macro will perform the following:

- Choose Volume Control for -3dB level.
- Configure and power up the signal path to decode compressed audio to speaker driver.
- Set up all GPIOs except GPIO4 for Falling edge trigger and set GPIO4 for both falling and rising edge trigger.

The following is the complete list of the command available for use in Voice Macros:

- WR_CFG_REG(*reg n*) – Set configuration register *reg* to value *n*.
- PWR_DN – Power down the ISD2100.
- PLAY_VP(*i*) – Play Voice Prompt index *i*.
- PLAY_VP@(*Rn*) – Indirect Play Voice Prompt of index in register *Rn*
- PLAY_VP_LP(*i,cnt*) – Loop Play Voice Prompt index *i, cnt* times.
- PLAY_VP_LP@(*Rn,cnt*) – Indirect Loop Play Voice Prompt index in *Rn, cnt* times.
- EXE_VM(*i*) – Execute Voice Macro index *i*.
- EXE_VM@(*Rn)* – Indirect Execute Voice Macro index in register *Rn*
- PLAY_SIL(*n*) – Play silence for *n* units. A unit is 32ms at master sampling rate of 32 kHz.
- WAIT_INT – Wait until current play command finishes before executing next macro instruction.
- FINISH – Finish the voice macro and exit.

The Voice Macro commands are executed by device's Voice Macro state machine. Function wise they are equivalent to the SPI commands.

7.1.3 User Data

User Data consists of 1KByte multiples of erasable sectors allocated by the user. This can be used as generic non-volatile storage by the host application. The developer has the freedom not to allocate or reserve any memory sectors. A software tool, the ISD2100 Voice Prompt Editor is available to assist customers in allocating such memory.

7.2 Memory Contents Protection

Under certain circumstances, it is desirable to protect portions of the internal memory from write/erase or interrogation (read). The ISD2100 provides a method to achieve this by setting a protection memory pointer (PMP) that allows the users to protect memory for an address range from the beginning of memory to this sector containing the PMP pointer. The type of protection is set by three bits in the memory header byte.

Memory protection is activated on power-up of the chip. Therefore, each time the user changes the setting of memory protection, the new setting will not be effective until the chip is reset.

8 SPI INTERFACE

This is a standard four-wire serial interface used for communication between ISD2100 and the host. It consists of an active low slave-select (SSB), a serial clock (SCLK), a data input (Master Out Slave In - MOSI), and a data output (Master In Slave Out - MISO). In addition, for some transactions requiring data flow control, a RDY/BSYB signal (pin) is available.

The ISD2100 supports **SPI mode 3:** (1) SCLK must be high when SPI bus is inactive, and (2) data is sampled at SCLK rising edge. A SPI transaction begins on the falling edge of SSB and its waveform is illustrated below:

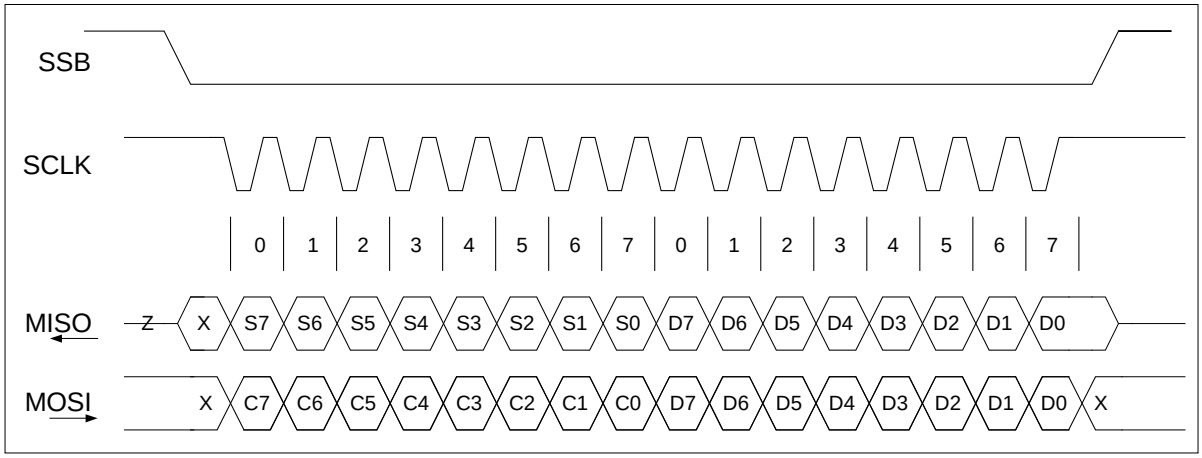


Figure 8-1 SPI Data Transaction.

A transaction begins with sending a command byte (C7-C0) with the most significant bit (MSB – C7) sent in first. During the byte transmission, the status (S7-S0) of the device is sent out via the MISO pin. After the byte transmission, depending upon the command sent, one or more bytes of data will be sent via the MISO pin.

RDY/BSYB pin is used to handshake data into or out of the device. Upon completion of a byte transmission, RDY/BSYB pin could change its state after the rising edge of the SCLK if the built-in 32-byte data buffer is either full or empty. At this point, SCLK must remain high until RDY/BSYB pin returns to high, indicating that the ISD2100 is ready for the next data transmission. See below for timing diagram.

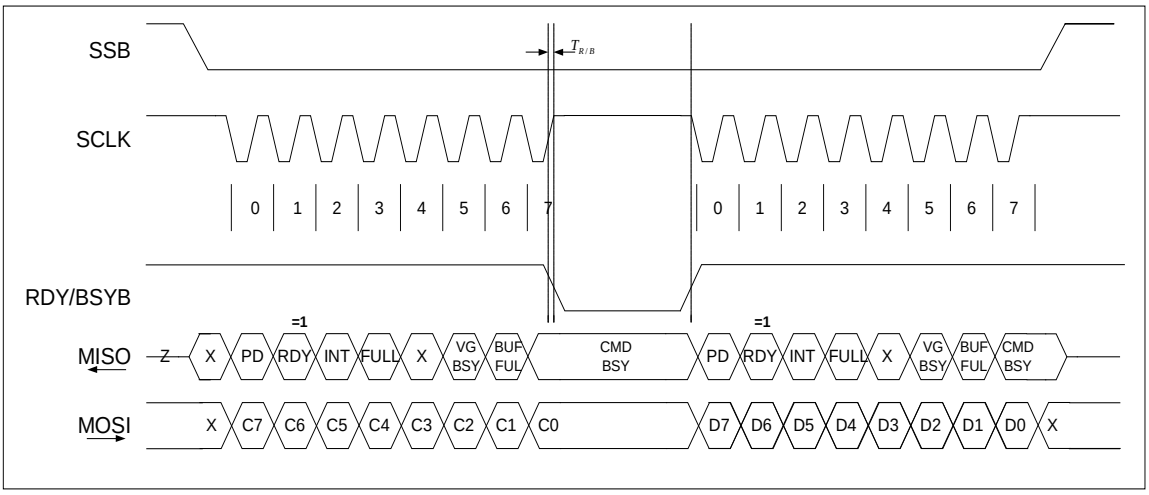


Figure 8-2 RDY/BSYB Timing for SPI Writing Transactions.

If the SCLK does not remain high, RDY bit of the status register will be set to zero and be reported via the MISO pin so the host can take the necessary actions (i.e., terminate SPI transmission and re-transmit the data when the RDY/BSYB pin returns to high).

For commands (i.e., DIG_READ, SPI_PCM_READ) that read data from the ISD2100 device, MISO is used to read the data; therefore, the host must monitor the status via the RDY/BSYB pin and take the necessary actions. The INT pin will go low to indicate (1) data overrun/overflow when sending data to the ISD2100; or (2) invalid data from ISD2100. See Figure 8-3 for the timing diagram.

To avoid RDY/BSYB polling for digital operations the following conditions must be met:

- Ensure device is idle (CMD_BSY=0 in status) before operation.
- Digital Write: Send 32 bytes of data or less in a digital write transaction **or** ensure that there is a 24µs period between each byte sent where SCLK is held high.
- Digital Read: Ensure a 2µs period between last address byte of digital read command and first data byte where SCLK is held high.

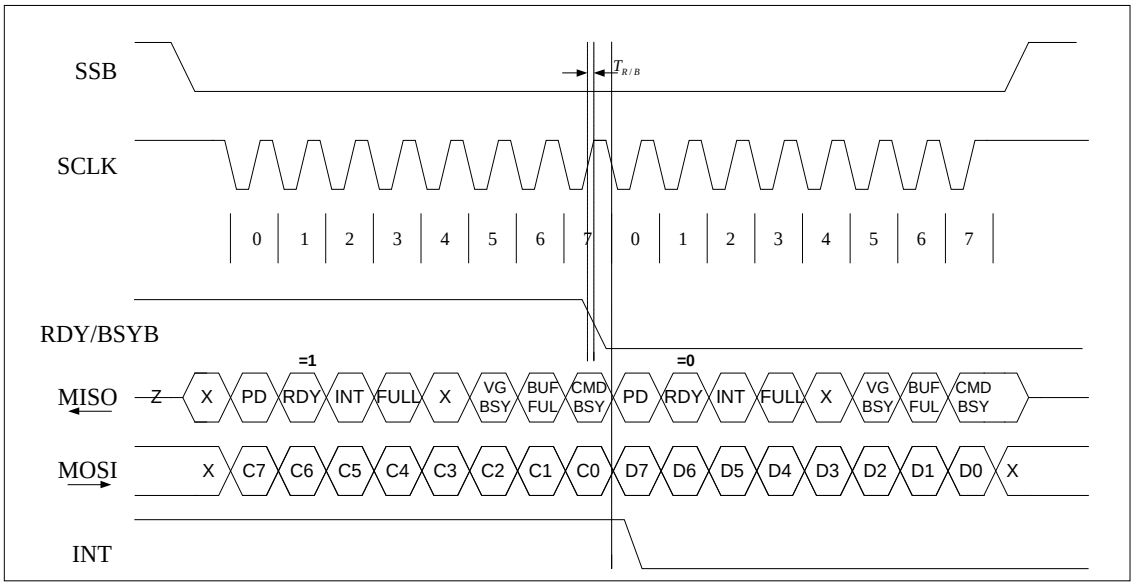


Figure 8-3 SPI Transaction Ignoring RDY/BSYB

9 SIGNAL PATH

The signal path performs filtering, sample rate conversion, volume control and decompression. A block diagram of the signal path is shown in Figure 9-1. The PWM driver output pins SPK- and SPK+ provide a differential output to drive an 8Ω speaker or buzzer. During power down these pins are in tri-state.

Pre-compressed audio transfers from memory or SPI interface through the de-compressor block to PWM driver or SPI out. The audio level is adjustable via VOLC before going out on to the PWM driver path. The possible path combinations are:

MEMORY → DECOMPRESS → SPKR (Playback to speaker)

MEMORY → DECOMPRESS → SPI_OUT (SPI playback)

SPI_IN → DECOMPRESS → SPKR (SPI decode to speaker)

For example, to playback audio to speaker, enable decompression and PWM (write 0x44 to register 0x02) then send a PLAY_VP command to play audio.

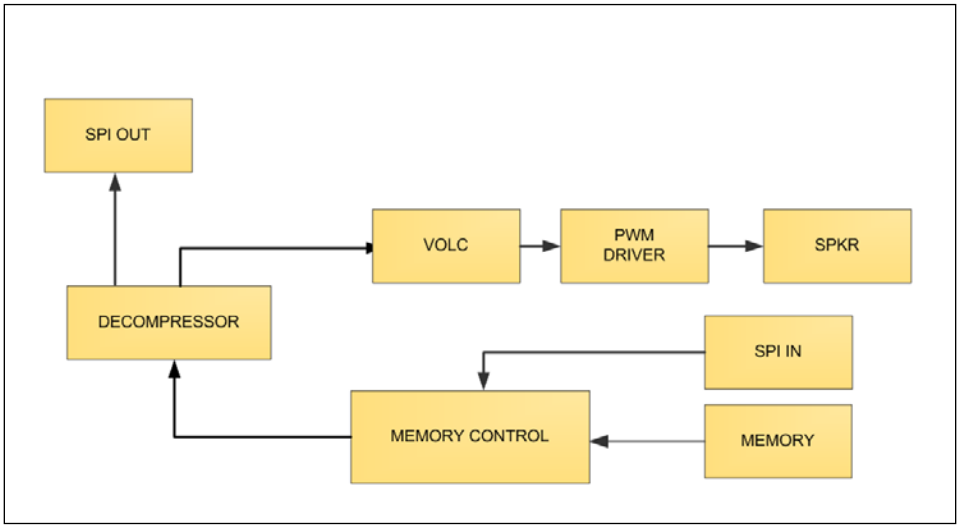


Figure 9-1 ISD2100 Signal Path

10 GPIO VOICE MACRO TRIGGERS

The ISD2100 Voice Macro capability and GPIO flexibility allows the user to configure the device to operate independently of the SPI interface or host micro-controller.

GPIO triggering utilizes the Jump registers R0 through R6. When a GPIO trigger event occurs the ISD2100 executes the Voice Macro whose index is stored in the corresponding Jump register: that is GPIO0 will execute the VM whose index is stored in R0, GPIO1 in R1 etc. The initial values of the R0-R6 registers can be set up in the POI Voice macro which is executed when a power-on reset condition is detected. When the ISD2100 responds to a trigger event, if a Voice Macro is currently being executed, that Voice Macro is first stopped before execution of new Voice Macro.

10.1 VOICE MACRO EXAMPLES

Below are some useful examples demonstrating the features Voice trigger macros. The example project can be found in the ISD2100VPE distribution as the ISD2100example project.

10.1.1 POI/PU/WAKEUP Voice Macros

These special purpose Voice Macros allow the user to configure the ISD2100 for subsequent trigger events. The POI macro is executed when the chip receives an internal power-on reset condition or the SPI SW_RESET command is sent.

The POI Voice macro is used to configure the ISD2100 for subsequent trigger events, for example:

```
a.  CFG(REG2, 0x44)            ; Configure signal path to playback
b.  CFG(VOLC, 0x00)            ; Set Volume to 0dB
c.  CFG(R5, 0x03)              ; Set Jump register R5 to 0x03, GPIO5 to trigger VM#3
d.  CFG(R4, 0x07)              ; Set Jump register R4 to 0x07, GPIO4 to trigger VM#7
e.  CFG(R3, 0x09)              ; Set Jump register R3 to 0x09, GPIO3 to trigger VM#9
f.  CFG(R2, 0x0a)              ; Set Jump register R2 to 0x0a, GPIO2 to trigger VM#A
g.  CFG(R1, 0x0c)              ; Set Jump register R1 to 0x0c, GPIO1 to trigger VM#C
h.  CFG(R0, 0x0e)              ; Set Jump register R0 to 0x0e, GPIO0 to trigger VM#E
i.  PLAY_VP(FastBeep)          ; Play Voice Prompt FastBeep
j.  CFG(REG_GPIO_AF1, 0xff)    ; Set up GPIOs to trigger off falling edges
k.  CFG(REG_GPIO_AF0, 0x00)
l.  PD                         ; Power Down
```

This POI macro will initialize the GPIO configuration such that all GPIO triggers are enabled for falling edges and performs initialization of the jump registers to point to appropriate Voice Macros. It also configures the play path and plays a beep. At the end of the macro the chip powers down.

The GPIO_WAKEUP is executed whenever the device is triggered from a power down state.

```
a.  CFG(REG2, 0x44)            ; Configure signal path to playback
b.  CFG(VOLC, 0x00)            ; Set Volume to 0dB
c.  CFG(R4, 0x07)              ; Set Jump register R4 to 0x07, GPIO4 to trigger VM#7
d.  CFG(R2, 0x0a)              ; Set Jump register R2 to 0x0a, GPIO2 to trigger VM#A
e.  Finish                     ; Exit Voice Macro, stay powered up.
```

This GPIO_WAKEUP macro sets up the play path as settings in these registers are reset during power down. It also resets jump registers R4 and R2 to default conditions.

10.1.2 Example: Cycle through a sequence of messages.

In this example a high-to-low transition on GPIO5 will initially trigger VM#3 as defined in the POI initialization macro. In VM#3 the Voice Prompt "One" is played and jump register R5 set to VM#4. Thus the next high-to-low transition on GPIO5 will trigger VM#4 and play Voice Prompt "Two". Similarly next trigger will play "Three" then "Four" and back to "One". Notice the difference in VM#4 where a WAIT_INTERRUPT command has been inserted before the setting of the jump register. If the GPIO5/SW6 button is pushed rapidly, so that play is interrupted, "Two" will continue to be repeated. Other Voice Macros, because the jump register is changed first, will always progress to the next step in sequence.

- **VM#3**: **R5_Count_One (GPIO5)**
    a. CFG(R5, 0x04) ; Configure GPIO5 to play VM#4 on next trigger
    b. Play(One) ; Play voice prompt "One"
    c. PD ; Power Down
- **VM#4:Two**
    a. Play(Two) ; Play voice prompt "Two"
    b. Wait Interrupt ; Wait until Play finishes
    c. CFG(R5, 0x05) ; Configure GPIO5 to play VM#5 on next trigger
    d. PD ; Power Down
- **VM#5: Three**
    a. CFG(R5, 0x06) ; Configure GPIO5 to play VM#6 on next trigger
    b. Play(Three) ; Play voice prompt "Three"
    c. PD ; Power Down
- **VM#6: Four**
    a. CFG(R5, 0x03) ; Configure GPIO5 to play VM# 3 on next trigger
    b. Play(Four) ; Play voice prompt "Four "
    c. PD ; Power Down

10.1.3 Example: Looping short sounds. Interrupt to stop playback.

This example demonstrates how to loop short sound samples and use a trigger interrupt to stop playback. A trigger on GPIO4 will play a series of Voice Prompts until it is interrupted by another trigger to stop playback. VM#7 was associated with the GPIO4 trigger in the POI routine. The first action of this VM is to change the trigger VM to VM#8, thus if GPIO4 is re-triggered while the Voice Macro is running it will execute the power down voice macro rather than start the play sequence again.

The next command sets the LRMP bit of REG1, under normal operation the compressor ramps signal level to zero after a sound sample is played to prevent a DC voltage appearing on the output. The LRMP bit prevents this from happening while a sample is looping allowing continuous audio. To loop a sound sample, the audio should be edited such that the last sample loops smoothly to the first. To do this, create the sample in a sound editor at the

sample rate desired for storage then find the first sample that returns to the initial condition and cut back audio to one before this sample. Note that tones require different lengths to fulfill these conditions at a given sample rate and thus loop numbers vary to produce the same length of output audio.

At the end of the VM REG1 is reset and the trigger is re-enabled back to VM#7 before powering down.

- **VM#7: R4_PlayLoop (GPIO4)**
    a. CFG(R4, 0x08) ; Configure GPIO4 to execute VM# 8 on next trigger.
    b. CFG(REG1, 0x20) ; Configure LRMP bit in REG1
    c. LOOP_VP(Do,20) ; LOOP “Do” 20 times.
    d. LOOP_VP(Re,250) ; LOOP “Re” 250 times.
    e. LOOP_VP(Mi,5) ; LOOP “Mi” 5 times.
    f. LOOP_VP(Fa,33) ; LOOP “Fa” 33 times.
    g. LOOP_VP(So,10) ; LOOP “So” 10 times
    h. LOOP_VP(La,10) ; LOOP “La” 10 times
    i. LOOP_VP(Si,7) ; LOOP “Si” 7 times.
    j. Silence (128 ms) ; Insert 128ms of silence
    k. CFG(REG1, 0x00) ; Reset REG1
    l. CFG(R4, 0x07) ; Configure GPIO4 to execute VM#7 on next trigger.
    m. PD ; Power Down
- **VM#8: PD_R4**
    a. CFG(REG1, 0x00) ; Configure Register one to its default value 00
    b. CFG(R4, 0x07) ; Configure GPIO4 to execute VM#7 on next trigger.
    c. PD ; Power Down

10.1.4 Example: Uninterruptable Trigger, smooth audio.

In this example a single trigger on GPIO3 will sequence through several messages until all messages are played the playback cannot be interrupted by any other trigger. The example also demonstrates how to use begin and end segments to create smooth playback. Each “note” consists of concatenating three voice prompts, for instance “So_begin” “So” and “So_end”. The begin and end prompts ramp the audio smoothly to avoid sudden transients in sound level. The middle, full amplitude, section is created by looping a short sample.

At the beginning of the Voice Macro, all triggers are disabled so that Voice Macro cannot be interrupted from any source. The NRMP bit of REG1 is set so that concatenation of audio occurs without any ramp down between prompts. At the end of the macro, interrupts are re-enabled and device is powered down.

- **VM#9: R3_Non-Int_Smooth (GPIO3)**
    a. CFG(REG_GPIO_AF1, 0x00) ; Disable all triggers.
    b. CFG(REG1, 0x04) ; Set NRMP bit
    c. PLAY_VP(So_begin) ; Play “So_begin”
    d. LOOP_VP(So,10) ; Loop “So” 10 times.
    e. PLAY_VP(So_end) ; Play “So_end”
    f. PLAY_VP(Fa_begin)
    g. LOOP_VP(Fa,33)
    h. PLAY_VP(Fa_end)
    i. PLAY_VP(Mi_begin)
    j. LOOP_VP(Mi,5)
    k. PLAY_VP(Mi_end)
    l. PLAY_VP(Re_begin)
    m. LOOP_VP(Re,250)
    n. PLAY_VP(Re_end)
    o. PLAY_VP(Do_begin)
    p. LOOP_VP(Do,20)
    q. PLAY_VP(Do_end)
    r. Wait Interrupt ; Wait for audio to finish
    s. CFG(REG1, 0x00) ; Reset NRMP bit
    t. CFG(REG_GPIO_AF1, 0x3f) ; Re-enable interrupts
    u. PD ; Power down device.

10.1.5 Example: Continuous Play until re-trigger.

In this example a single trigger on GPIO2 will sequence through several messages with pause in between each message. Messages are played in a loop indefinitely until another trigger occurs on GPIO2 to stop playback.

- **VM0#A: R2_Loop_VM (GPIO2)**
    a. CFG(R2, 0x0b) ; Set Trigger to VM#B (PD_R2)
    b. PLAY_VP(One) ; Play “One”
    c. Silence (256 ms) ; pause 256ms
    d. PLAY_VP(two) ; Play “Two”
    e. Silence (256 ms)
    f. PLAY_VP(three)
    g. Silence (736 ms)
    h. PLAY_VP(four)
    i. Silence (256 ms)
    j. EXE_VM(0xA) ; Execute VM#A (repeat)
    k. Finish

- **VM0#B: PD_R2**
    a. CFG(R2, 0x0a) ; Reset Trigger to VM#A
    b. PD ; Power Down.

10.1.6 Example: Level Hold Trigger.

In this example holding GPIO1 will play several messages. Releasing GPIO1 will stop the playback. No other triggers will affect operation.

- **VM#C: R1_Level_Hold (GPIO1)**
    a. CFG(REG_GPIO_AF0, 0x02) ; Enable rising edge trigger for GPIO2
    b. CFG(REG_GPIO_AF1, 0x02) ; Disable all triggers except GPIO2
    c. CFG(R1, 0x0d) ; Set Trigger to VM#D (PD_R1)
    d. CFG(REG1, 0x20)
    e. LOOP_VP(Re,200)
    f. Silence (32 ms)
    g. LOOP_VP(Mi,4)
    h. Silence (32 ms)
    i. LOOP_VP(Fa,20)
    j. Silence (32 ms)
    k. CFG(REG1, 0x00)
    l. PLAY_VP(applause)
    m. PD
- **VM#D: PD_R1**
    a. CFG(REG_GPIO_AF0, 0x00) ; Disable rising edge trigger
    b. CFG(REG_GPIO_AF1, 0x3f) ; Re-enable all triggers.
    c. CFG(REG1, 0x00) ; Ensure REG1 reset
    d. CFG(R1, 0x0c) ; Set trigger to VM#C
    e. PD ; Power Down.

11 ELECTRICAL CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	CONDITION	MIN	MAX	UNITS
DC Power Supply	V_{CCD}	V_{CCD} - V_{SSD}	-0.3	+4.0	V
	V_{CCPCM}	V_{CCPCM} – V_{SSPCM}	-0.3	+4.0	V
Digital Input Voltage	DV_{IN}	DV_{IN} - V_{SSD}	V_{SSD} – 0.3	V_{CCD} + 0.3	V
Junction Temperature	T_J	-	-40	+125	°C
Storage Temperature	T_{st}	-	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

11.2 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Supply voltage (V_{DD}) [1]	+2.7V to +3.6V
Ground voltage (V_{SS}) [2]	0V
Digital input voltage (DV_{IN})	0V to 3.6V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

NOTES: [1] V_{DD} = V_{CCD} = V_{CCPWM}

[2] V_{SS} = V_{SSD} = V_{SSPWM}

11.3 AC PARAMETERS

11.3.1 Internal Oscillator

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Sample rate with Internal Oscillator	F_{Smax}	-1%	32kHz	+1%	kHz	Vdd = 3V. At room temperature

11.3.2 Speaker Outputs

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SNR, Memory to SPK+/SPK-	SNR_{MEM_SPK}		60		dB	Load 150Ω [2][3]
Output Power	P_{OUT_SPK} VCC=3.0			0.4	W	Load 8Ω [2]
THD, Memory to SPK+/SPK-	THD %		<1%			Load 8Ω [2]
Minimum Load Impedance	$R_{L(SPK)}$	4	8		Ω	

Notes: [1] Conditions V_{cc}=3V, T_A=25°C unless otherwise stated.
[2] Based on 12-bit PCM.
[3] All measurements are C-message weighted.

11.4 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.7		3.6	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}-0.3		0.3xV_{DD}	V	I_{OL} = 1mA
Output High Voltage	V_{OH}	0.7xV_{DD}		V_{DD}	V	I_{OH} = -1mA
Pull-up Resistance	R_{PU}		50		kΩ	
Pull-down Resistance	R_{PD}		10		kΩ	
INTB Output Low Voltage	V_{OH1}			0.4	V	
Playback Current	$I_{DD\_Playback}$		5		mA	No Load [2]
Standby Current	I_{SB}		<1	10	µA	V_{DD}= 3.6V
Input Leakage Current	I_{IL}			±1	µA	Force V_{DD}

Notes: [1] Conditions V_{DD}=3V, T_A=25°C unless otherwise stated
[2] To calculate total current, add load dissipation into application specific load.

11.5 SPI TIMING

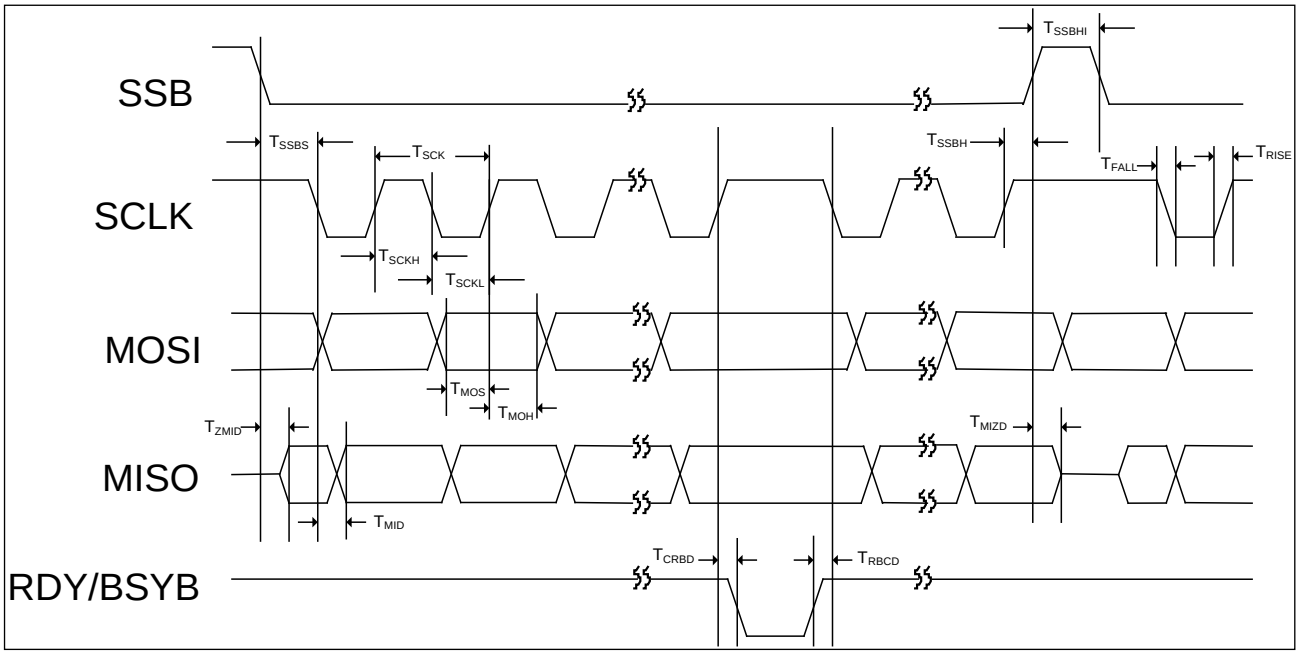


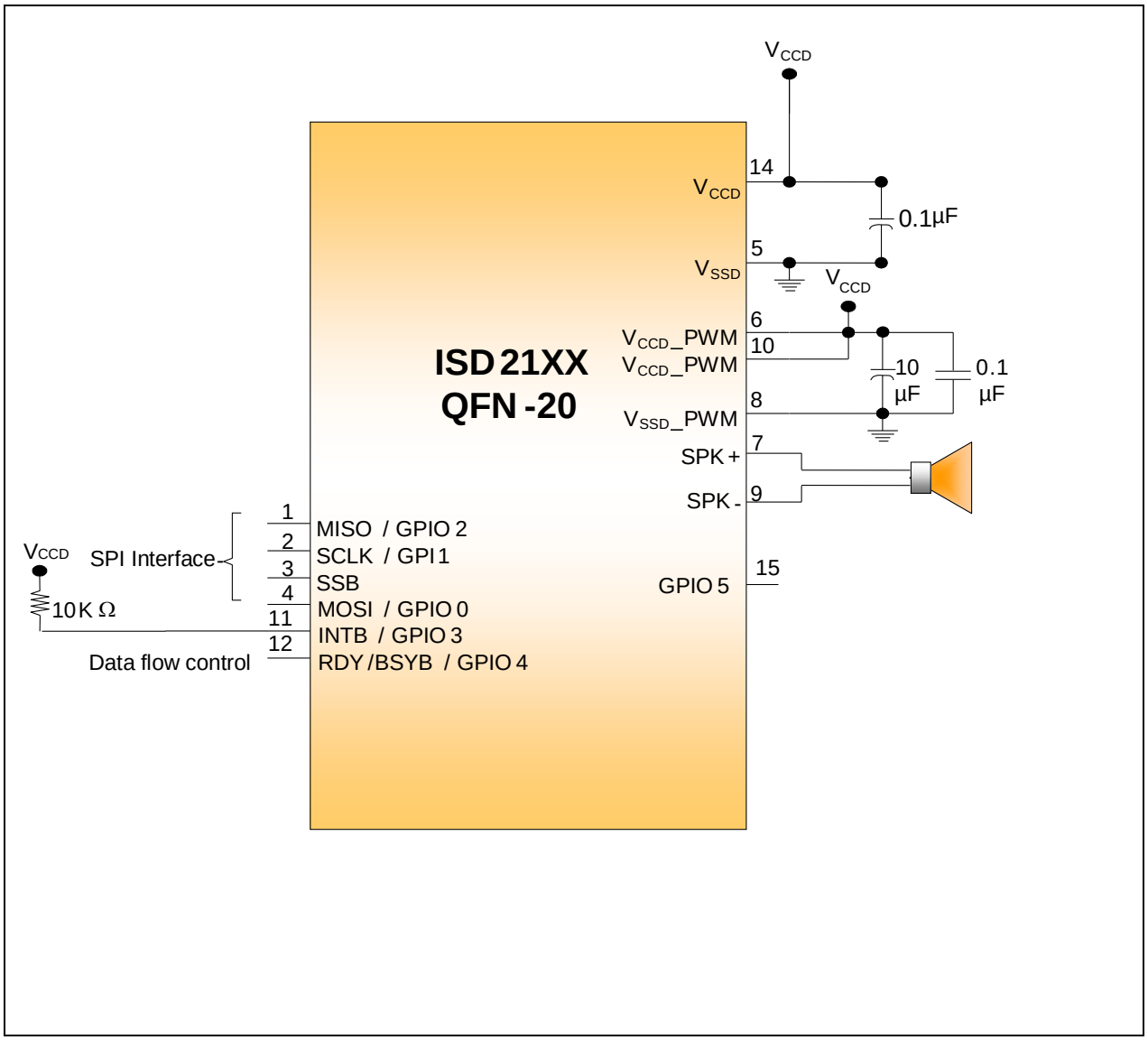
Figure 11-1 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	12	ns
T_{CRBD}	Delay Time: SCLK Rising Edge to RDY/BSYB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time: RDY/BSYB Rising Edge to SCLK Falling Edge	0	--	--	ns

12 APPLICATION DIAGRAM

12.1 SPI MODE APPLICATION

The following applications example is for reference only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionality etc.



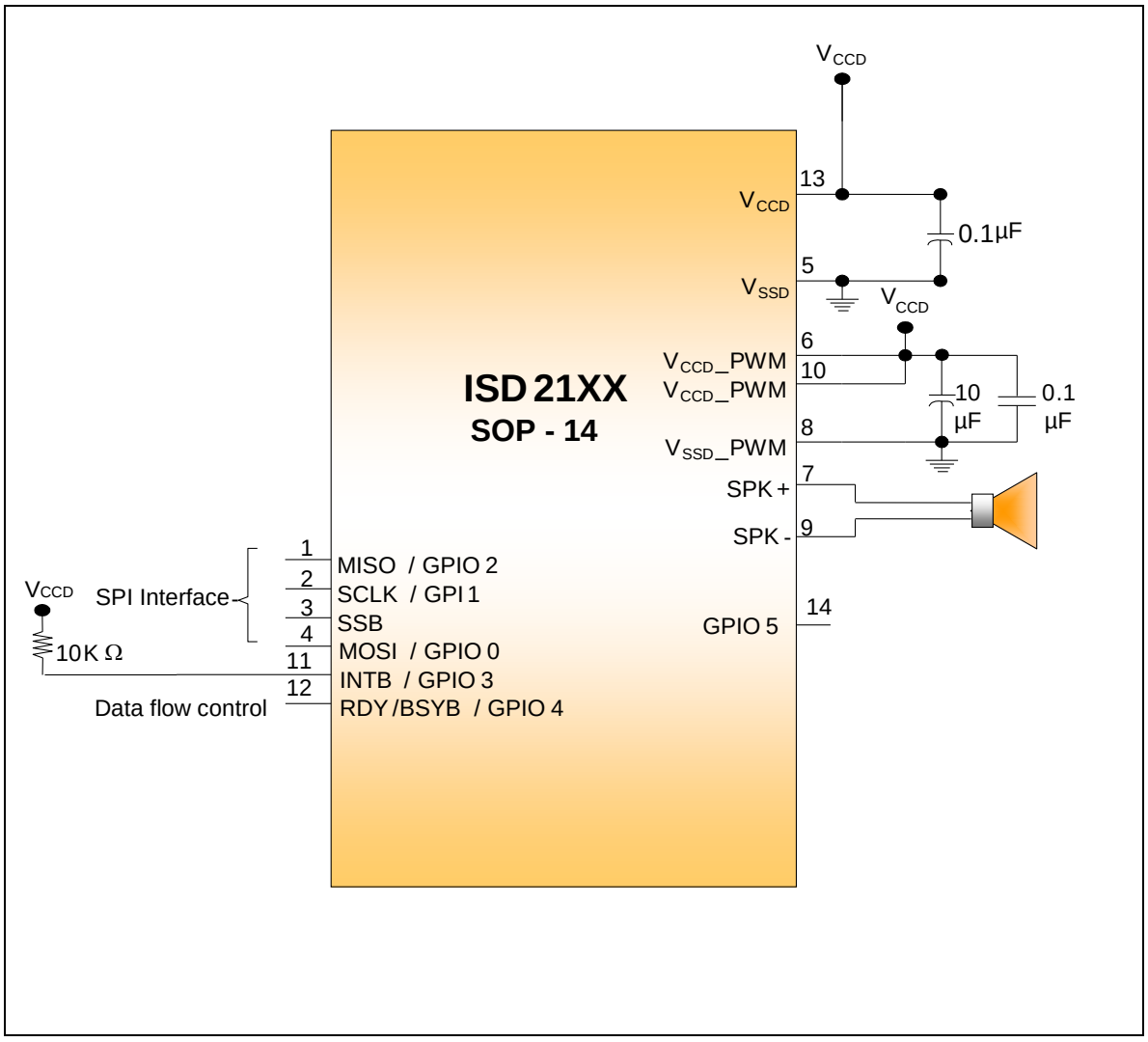
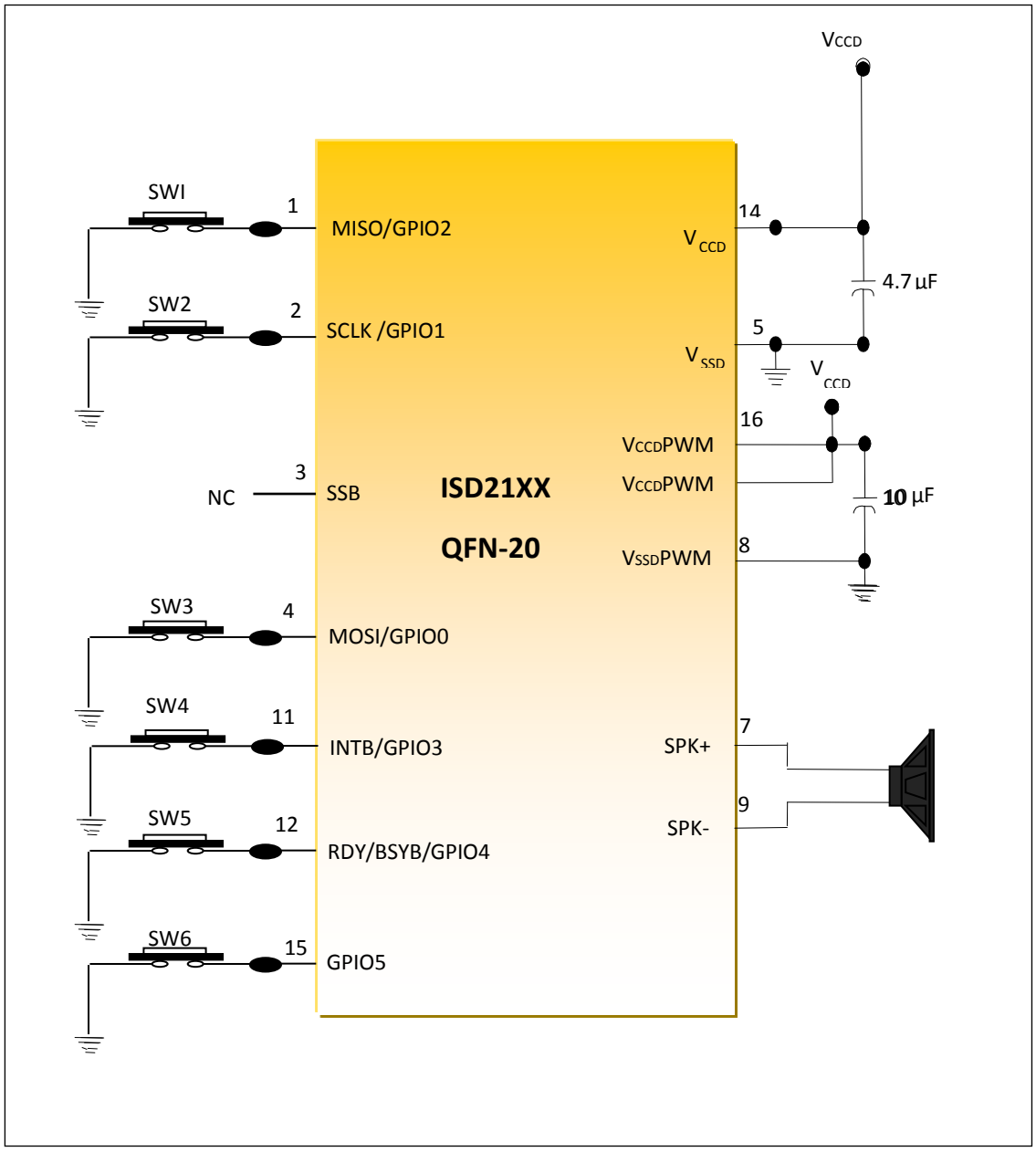


Figure 12-1 ISD2100 Application Diagram Example for programming with a Microcontroller SPI Mode

12.2 STANDALONE APPLICATION

The following applications example is for reference only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionality etc.



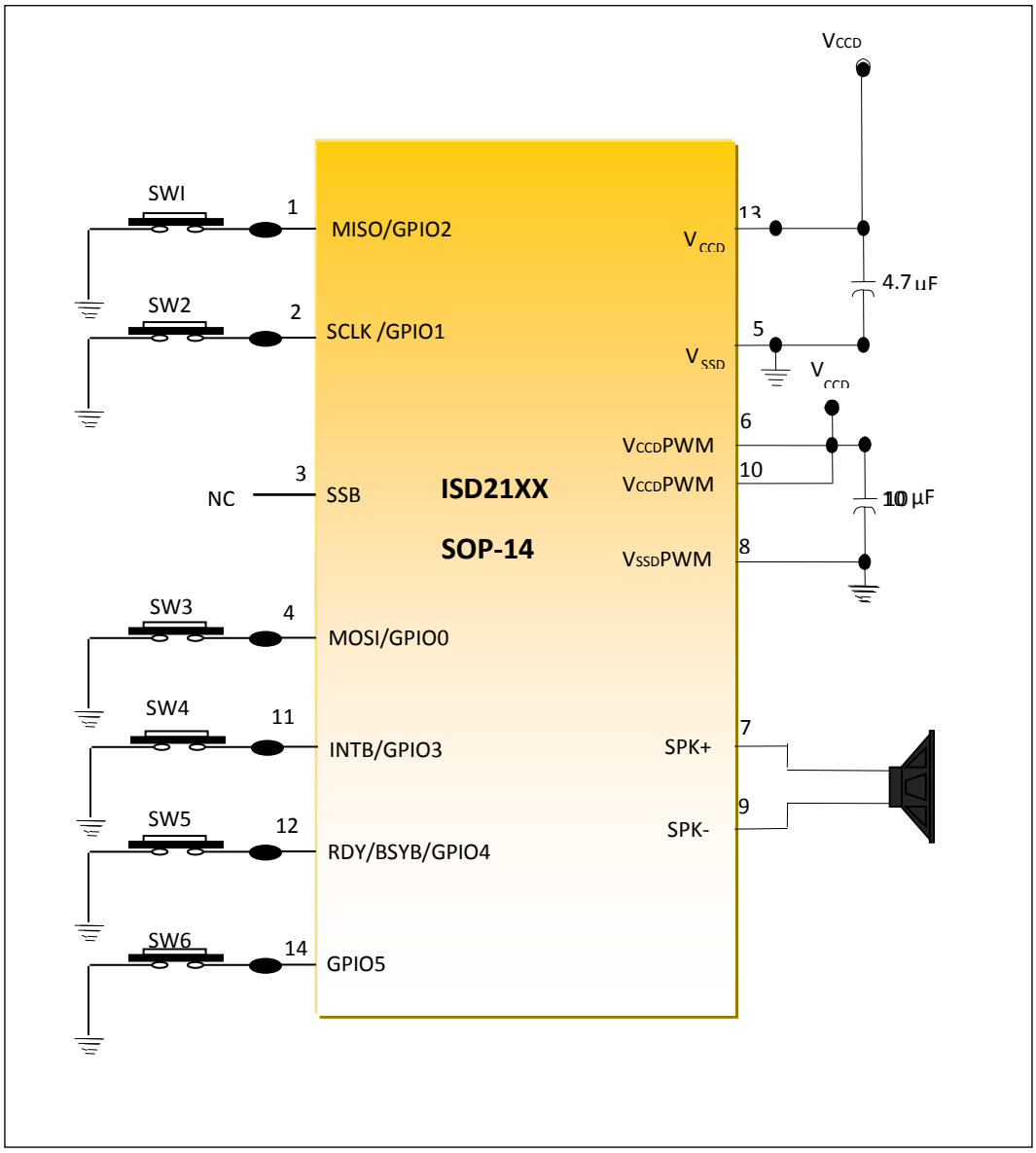
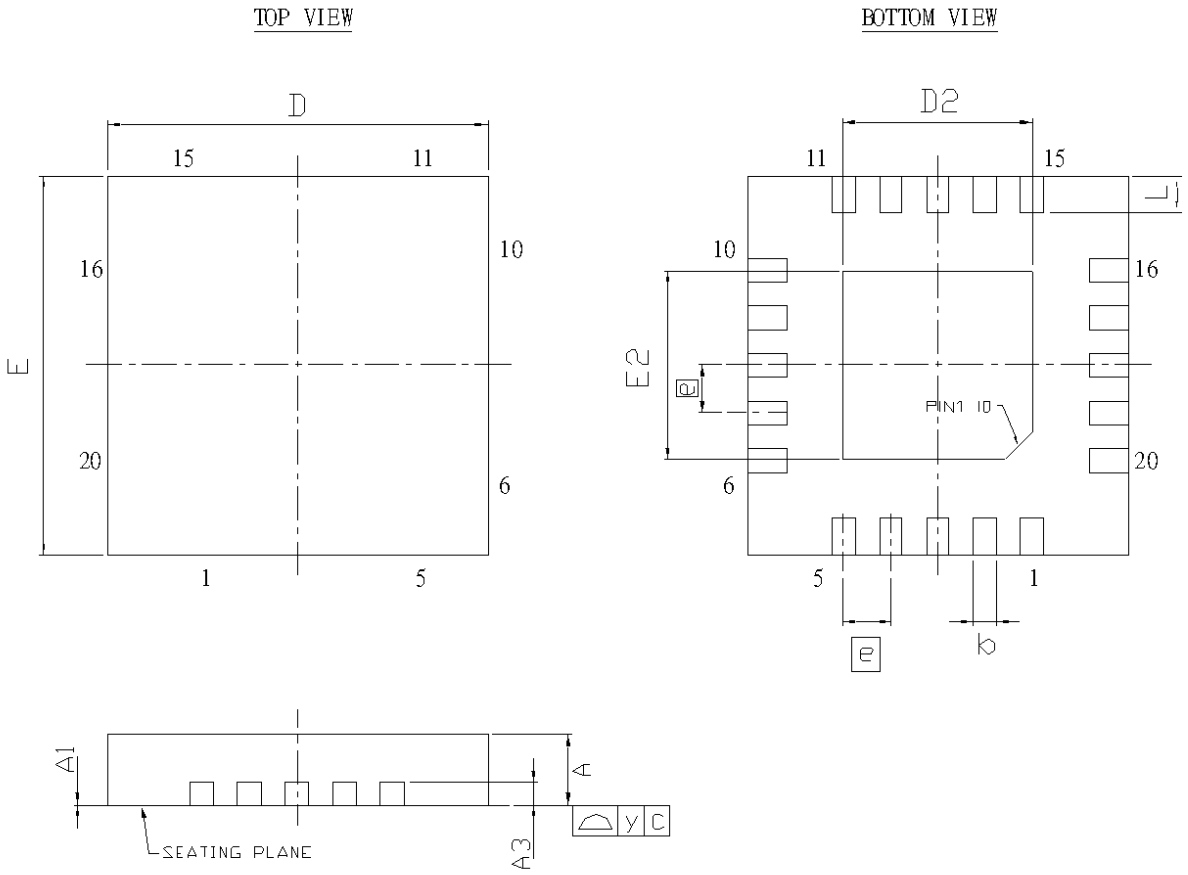


Figure 12-2 ISD2100 Application Diagram Stand-Alone Mode

13 PACKAGE SPECIFICATION

13.1 20 LEAD QFN PACKAGE

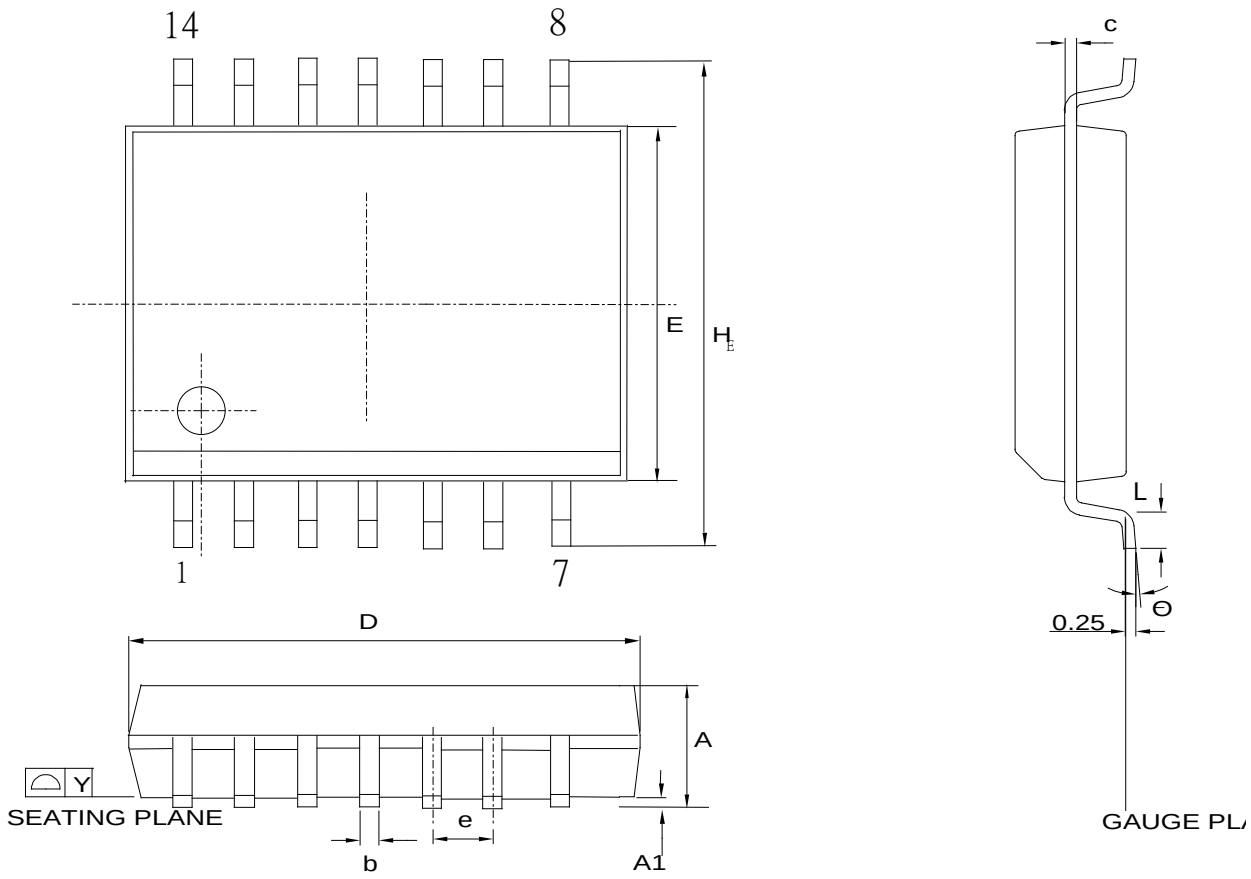


Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note.D2,E2 by die size difference .

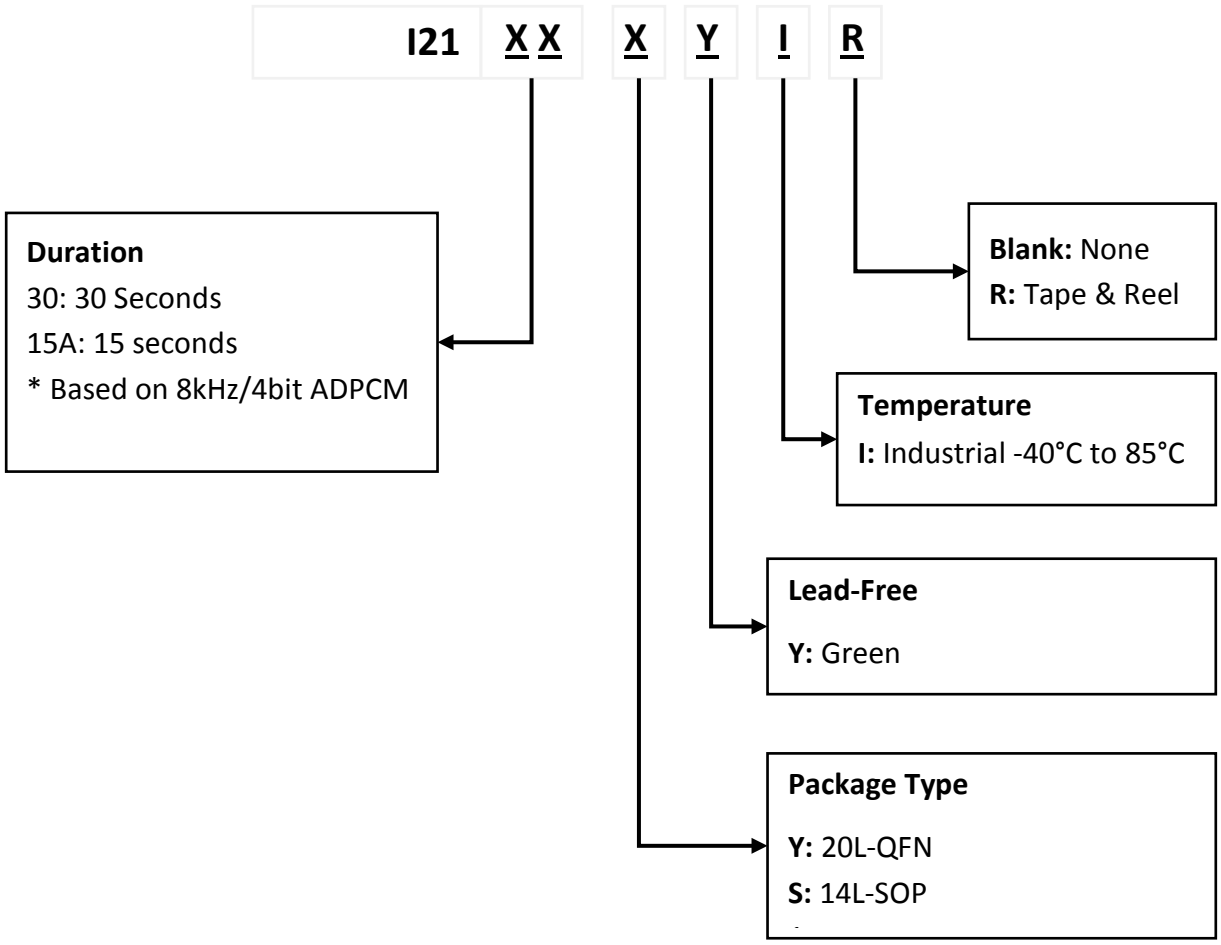
13.2 14 LEAD 150-MIL SMALL OUTLINE PACKAGE



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	8.55	8.75	0.337	0.344
e	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y	———	0.10	———	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

14 ORDERING INFORMATION



Duration	15 Seconds		30 Seconds	
Package	None	Tape & Reel	None	Tape & Reel
20L-QFN	I2115AYYI	I2115AYYIR	I2130YYI	I2130YYIR
14L-SOP	I2115ASYI	-	I2130SYI	I2130SYIR

15 REVISION HISTORY

Version	Date	Description
0.2	November 5, 2009	Initial draft.
0.45	August 5, 2009	Add Wake-Up VM description
0.46	November 11, 2009	Add Checksum Description
0.48	January 9, 2010	Simplify all Block diagrams
0.51	Feb 4, 2010	Update description
1.0	March 4, 2010	Update description
1.1	April 01, 2010	Update description
1.2	July 27, 2010	Add 2110 duration
1.3	Oct 26, 2010	Update description
1.4	Dec 03, 2010	$I_{DD\_Playback}$ Update
1.7	July 13, 2011	Add 2115 duration
1.8	Aug 21, 2013	Remove 2110 duration
1.9	July 13, 2016	Add storage temperature
2.0	Aug 1, 2016	Update Absolute Maximum Rating. Add V_{CCD}_PWM description.
2.01	Aug 8, 2016	Fix format error
2.02	Dec 13, 2017	Description update
2.1	Mar 30, 2020	Update document format
2.3	May 20, 2020	Add SOP-14 package and related description
2.4	July 24, 2020	Fix Page 7, Package Drawing Update Ordering information

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