National Semiconductor

ADVANCE INFORMATION

F100328
Low Power Octal ECL/TTL Bi-Directional Translator with Latch

General Description

The F100328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the F100328 transparent.

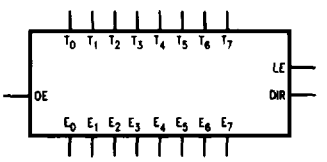
The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The F100328 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

Features

- Identical performance to the F100128 at 50% of the supply current
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- FAST® TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V

Logic Symbol



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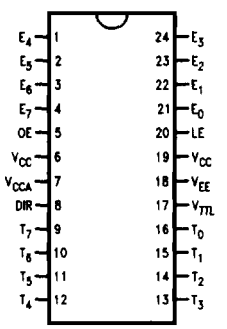
Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

Connection Diagrams

24-Pin DIP



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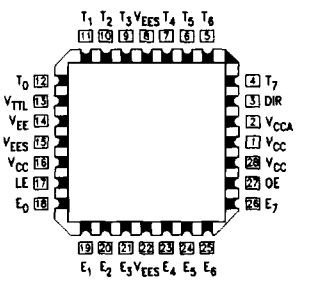
28-Pin PCC



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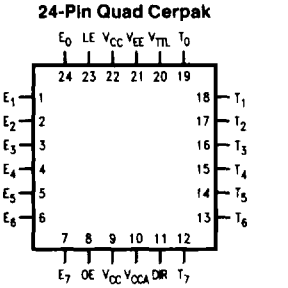
24-Pin Quad Cerpak



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