54F280A, 54F280B
Parity Generator Checker

9-Bit Odd/Even Parity Generator/Checker

Product Specification

Military Logic Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Buffered inputs — one normalized load**
- **Word length easily expanded by cascading**

DESCRIPTION

The 54F280A, 54F280B are 9-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is High when an even number of Data inputs (I_0 - I_8) are High. The odd parity output (Σ_O) is High when an odd number of Data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 25ns with the 54F280A, 54F280B.

The 54F280B is a speed enhanced version with better t_{PLH} to t_{PHL} matching.

ORDERING INFORMATION

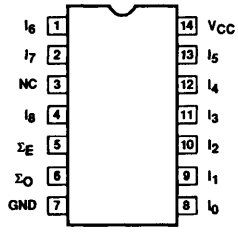
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F280A/BCA 54F280B/BCA
14-Pin Ceramic FlatPack	54F280A/BDA 54F280B/BDA
14-Pin Ceramic LLCC	54F280A/B2A 54F280B/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0 - I_8	Data inputs	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	50/33	1.0mA/20mA

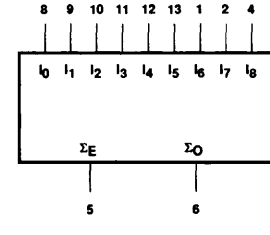
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

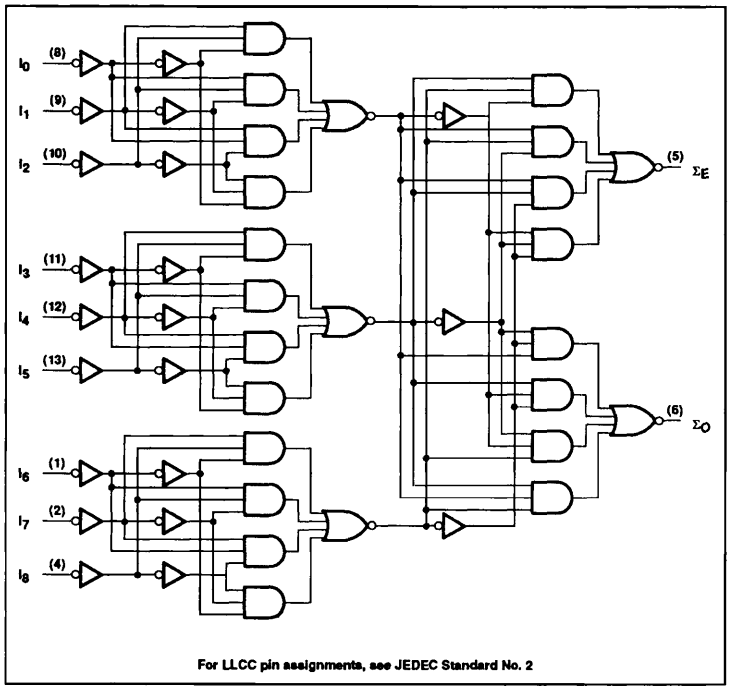
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Parity Generator Checker | 54F280A, 54F280B

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High Data Inputs (I_0 - I_8)	Σ_E	Σ_O
Even — 0, 2, 4, 6, 8	H	L
Odd — 1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{Ih} = Min, I_{OL} = Max		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		4.0	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.1	-20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V	-60	-114	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		26	35	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS – 54F280A					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	Waveform 1, 2	5.0 4.0	7.0 11.1	9.0 13.0	4.0 4.0	11.0 17.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	Waveform 1, 2	5.0 5.0	8.6 9.1	10.5 11.0	4.0 4.0	12.0 16.0	ns ns

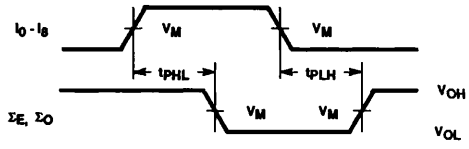
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS – 54F280B					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.0 3.5	11.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.0 3.5	11.0 12.0	ns ns

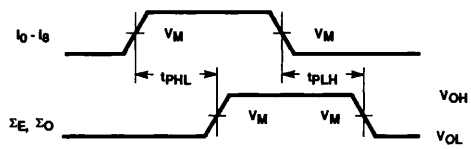
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with all outputs open.

AC WAVEFORMS



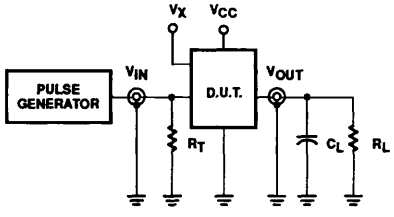
Waveform 1. Waveform for Inverting Outputs



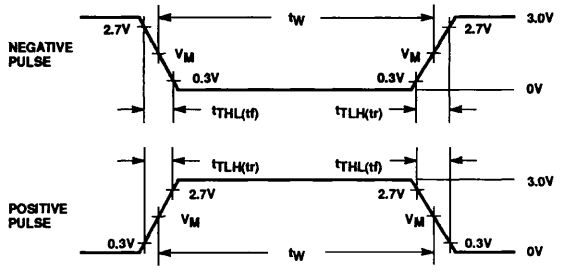
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns