

Matrix Multiplier

12 x 10 Bits, 40MHz

The TMC2250 is a flexible high-performance nine-multiplier array VLSI circuit which can execute a cascadeable 9-tap FIR filter, a cascadeable 4 x 2 or 3 x 3-pixel image convolution, or a 3 x 3 color space conversion. All configurations offer throughput at up to the maximum guaranteed 40MHz clock rate with 12-bit data and 10-bit coefficients. All inputs and outputs are registered on the rising edges of the clock.

The 3 x 3 matrix multiply or color conversion configuration can perform video standards conversion (YIQ or YUV to RGB, etc.) or three-dimensional perspective translation at real-time video rates.

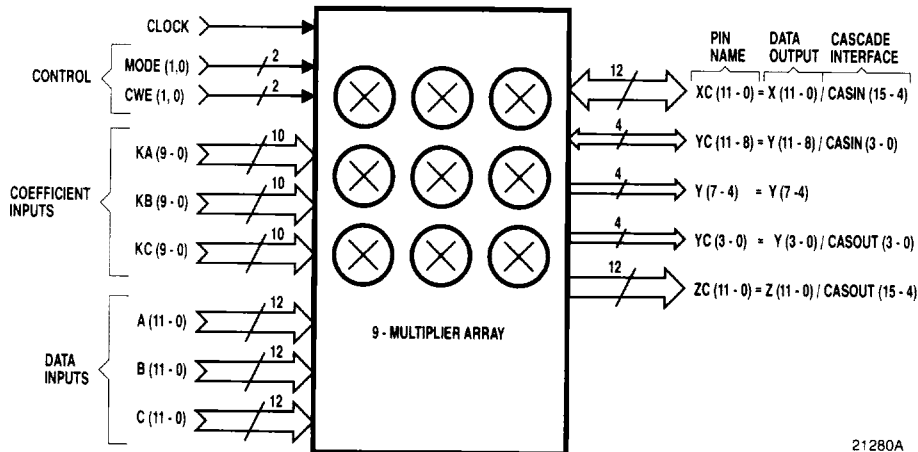
The 9-tap FIR filter configuration, useful in Video, Telecommunications, and Signal Processing, features

a 16-bit cascade input to allow construction of longer filters.

The cascadeable 3 x 3 and 4 x 2-pixel image convolver functions allow the user to perform numerous image processing functions, including static filters and edge detectors. The 16-bit cascade input port facilitates two-chip 40MHz cubic convolution (4 x 4-pixel kernel).

The TMC2250 is fabricated in TRW's OMICRON-C™ one-micron CMOS process and operates at clock speeds of up to 40MHz over the full commercial (0°C to 70°C) temperature and supply voltage ranges. It is available in a 121 pin plastic pin grid array (PPGA) package. All input and output signals are TTL compatible.

Logic Symbol



Features

- Four User-Selectable Filtering And Transformation Functions:
 - Triple Dot Product (3 x 3) Matrix Multiply
 - Cascadeable 9-Tap Systolic FIR Filter
 - Cascadeable 3 x 3-Pixel Image Convolver
 - Cascadeable 4 x 2-Pixel Image Convolver
- 40MHz (25ns) Pipelined Throughput
- 12-Bit Input And Output Data, 10-Bit Coefficients
- 16-Bit Cascade Input And Output Ports In All Filter Modes
- Onboard Coefficient Storage, With Three-Cycle Updating Of All Nine Coefficients

Applications

- Image Filtering And Manipulation
- Video Effects Generation
- Video Standards Conversion And Encoding/Decoding
- Three-Dimensional Image Manipulation
- Medical Image Processing
- Edge Detection For Object Recognition
- FIR Filtering For Communications Systems

Functional Description

General Information

The TMC2250 is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product) or cascadeable 9-tap FIR filter, 3 x 3-pixel convolver, or 4 x 2-pixel convolver, all in one monolithic circuit. With a 30MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A, B, C) accept 12-bit two's complement integer data, which is also the format for the output ports (X, Y, Z) in the matrix multiply mode (Mode 00). In the filter configurations (Modes 01, 10,

and 11), the cascade ports assume 12-bit integer, 4-bit fractional two's complement data on both input and output. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. **Table 1** details the bit weighting of the input and output data in all configurations.

Operating Modes

The TMC2250 can implement four different digital filter architectures. Upon selection of the desired function by the user (MODE₁₋₀), the device reconfigures its internal data paths and input and output buses appropriately. The output ports (XC, YC, and ZC) are configured in all filter modes as 16-bit Cascade In and Cascade Out ports so that multiple devices can be connected to build larger filters. These modes are described individually below. The I/O pin-function configurations for all four modes are shown in **Table 1**.

Definitions

The calculations performed by the TMC2250 in each mode are also shown below, utilizing the following notation:

A(1), B(5), C(2), CASIN(3)	Indicates the data word presented to that input port during the specified clock rising edge (x). Applies to all input ports A ₁₁₋₀ , B ₁₁₋₀ , C ₁₁₋₀ , and CASIN ₁₅₋₀ .
KA1(1), KB3(4)	Indicates coefficient data stored in the specified one of the nine onboard coefficient registers KA1 through KC3, as shown in the block diagram for that mode, input during or before the specified clock rising edge (x).
X(1), Y(4), Z(6), CASOUT(6)	Indicates data available at that output port t _{DD} after the specified clock rising edge (x). Applies to all output ports X ₁₁₋₀ , Y ₁₁₋₀ , Z ₁₁₋₀ , and CASOUT ₁₅₋₀ .

Table 1. Data Port Formatting by Mode

Mode	Inputs						Inputs/Outputs		Outputs		
	A ₁₁₋₀	B ₁₁₋₀	C ₁₁₋₀	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	XC ₁₁₋₀	YC ₁₁₋₈	Y ₇₋₄	YC ₃₋₀	ZC ₁₁₋₀
00	A ₁₁₋₀	B ₁₁₋₀	C ₁₁₋₀	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	X ₁₁₋₀	Y ₁₁₋₈	Y ₇₋₄	Y ₃₋₀	Z ₁₁₋₀
01	A ₁₁₋₀	A ₁₁₋₀	NC	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	CASIN ₁₅₋₄	CASIN ₃₋₀	NC	CASOUT ₃₋₀	CASOUT ₁₅₋₄
10	A ₁₁₋₀	B ₁₁₋₀	C ₁₁₋₀	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	CASIN ₁₅₋₄	CASIN ₃₋₀	NC	CASOUT ₃₋₀	CASOUT ₁₅₋₄
11	A ₁₁₋₀	B ₁₁₋₀	NC	KA ₉₋₀	KB ₉₋₀	KC ₉₋₀	CASIN ₁₅₋₄	CASIN ₃₋₀	NC	CASOUT ₃₋₀	CASOUT ₁₅₋₄

Numeric Format

Table 2 shows the binary weightings of the input and output ports of the TMC2250. Although the internal sums of products could grow to 23 bits, in the matrix multiply mode (Mode 00) the outputs X, Y, and Z are truncated to yield 12-bit integer words. Thus the output format is identical to the input data format. In the filter configurations (Modes 01, 10, and 11) the cascade output is always half-LSB rounded to 16 bits, specifically 12 integer bits and 4 fractional guard bits, with no overflow “headroom.” The user is of course free to half-LSB round the output word to any size less than 16 bits by forcing a 1 into the bit position of the cascade input immediately below the desired LSB. In all modes, bit weighting is easily adjusted if desired by applying the same scaling correction factor to both input and output data words. If the coefficients are rescaled, the relative weightings of the CASIN and CASOUT ports will differ accordingly.

Data Overflow

As shown in Table 2, the TMC2250’s matched input and output data formats accommodate 0 dB (unity) gain. Therefore, the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific algorithm performed to ensure that no overflow occurs.

Signal Definitions

Power

V_{DD}, GND The TMC2250 operates from a single +5V supply. All pins must be connected.

Clock

CLK The TMC2250 operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.



Table 2. Bit Weightings For Input and Output Data Words

Bit Weights	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	.	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	
Inputs																							
All Modes Data A, B, C	-1 ₁₁	1 ₁₀	1 ₉	1 ₈	1 ₇	1 ₆	1 ₅	1 ₄	1 ₃	1 ₂	1 ₁	1 ₀	.										
Coefficients KA, KB, KC												-K ₉	.	K ₈	K ₇	K ₆	K ₅	K ₄	K ₃	K ₂	K ₁	K ₀	
Modes 01, 10, 11 CASIN	-Cl ₁₅	Cl ₁₄	Cl ₁₃	Cl ₁₂	Cl ₁₁	Cl ₁₀	Cl ₉	Cl ₈	Cl ₇	Cl ₆	Cl ₅	Cl ₄	.	Cl ₃	Cl ₂	Cl ₁	Cl ₀						
Internal Sum	X ₂₀	X ₁₉	X ₁₈	X ₁₇	X ₁₆	X ₁₅	X ₁₄	X ₁₃	X ₁₂	X ₁₁	X ₁₀	X ₉	.	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	
Outputs																							
Mode 00 X, Y, Z	-O ₁₁	O ₁₀	O ₉	O ₈	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀	.										
Modes 01, 10, 11 CASOUT	-CO ₁₅	CO ₁₄	CO ₁₃	CO ₁₂	CO ₁₁	CO ₁₀	CO ₉	CO ₈	CO ₇	CO ₆	CO ₅	CO ₄	.	CO ₃	CO ₂	CO ₁	CO ₀						

Note: 1. A minus sign indicates a two’s complement sign bit.

3 x 3 Matrix Multiplier (Mode 00)

This mode utilizes all six input and output ports in the basic configuration to realize a "triple dot product," in which each output is the sum of all three input words in that column multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words

truncated to 12 bits are then available every clock cycle. See *Table 6* and the *Applications Discussion* section regarding encoded video standard conversion matrices.

$$X(5) = A(1)KA_1(1) + B(1)KB_1(1) + C(1)KC_1(1)$$

$$Y(5) = A(1)KA_2(1) + B(1)KB_2(1) + C(1)KC_2(1)$$

$$Z(5) = A(1)KA_3(1) + B(1)KB_3(1) + C(1)KC_3(1)$$

Figure 1. 3 x 3 Matrix Multiplier Impulse Response (Mode 00)

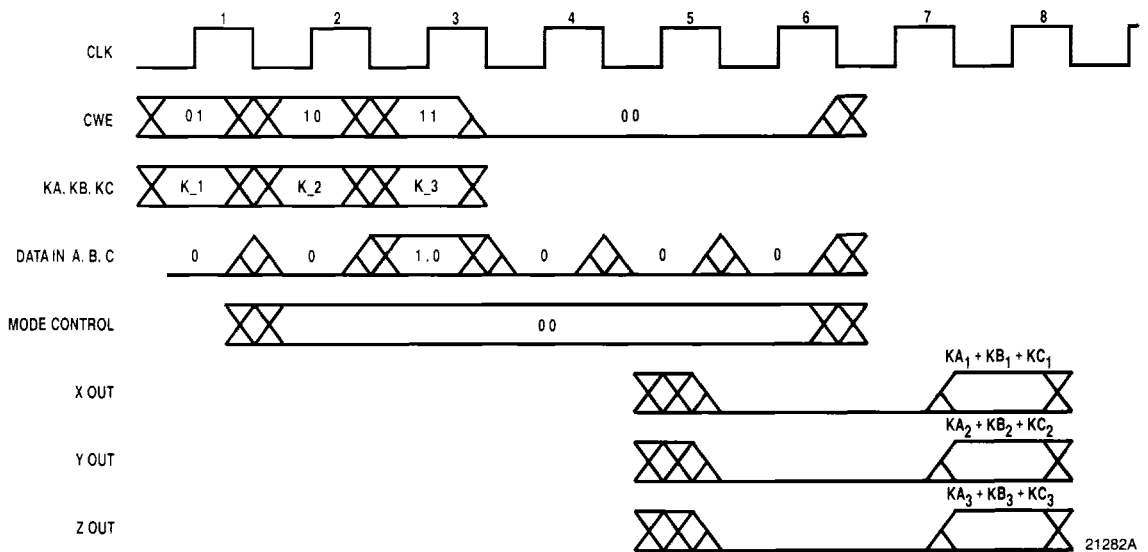
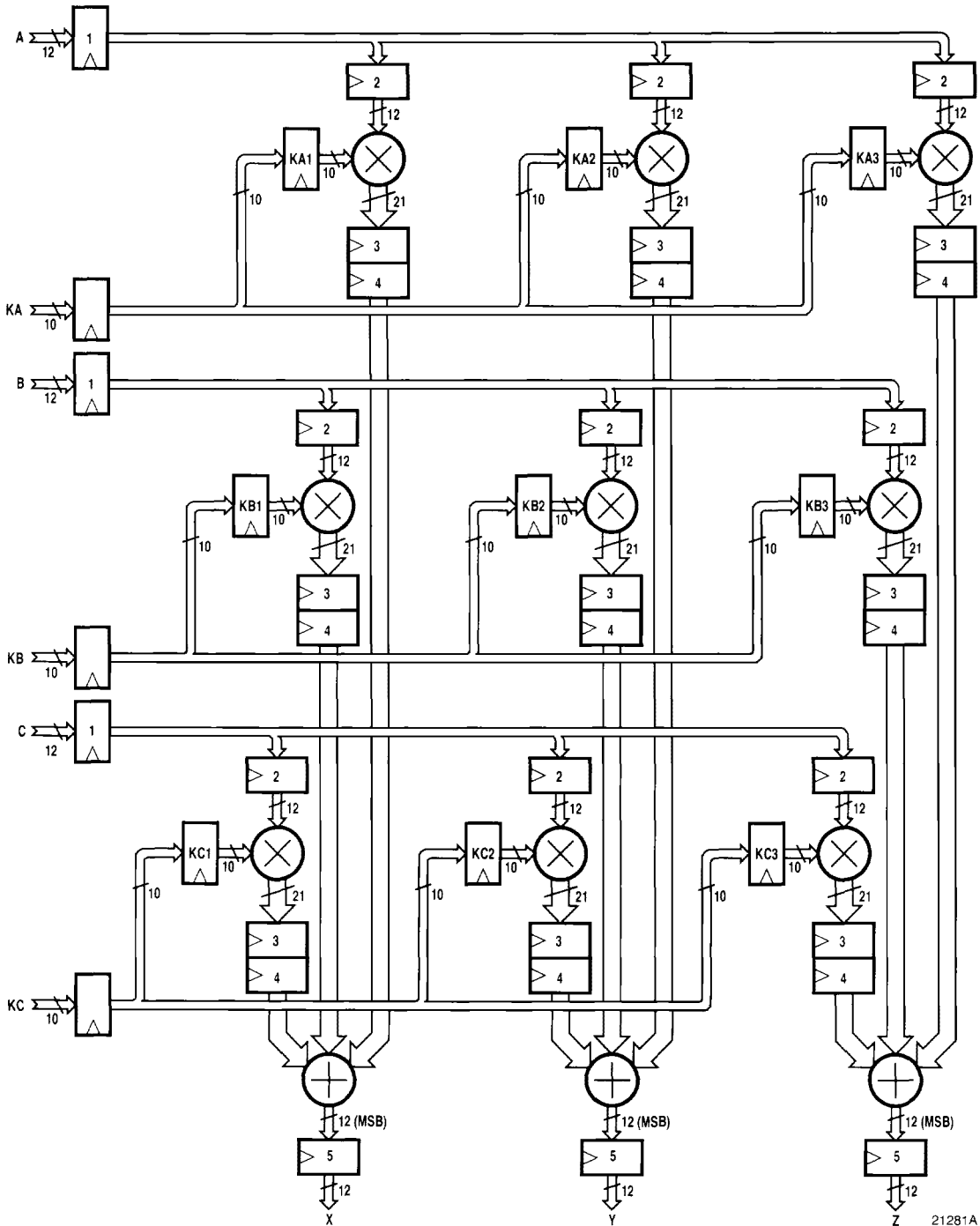


Figure 2. 3 x 3 Matrix Multiplier Configuration (Mode 00)



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9-Tap FIR Filter (Mode 01)

The architecture for this configuration is shown in *Figure 3*. The user loads the desired coefficient set, presents input data to ports A and B simultaneously (most applications will wire the A and B inputs together), and receives the resulting 9-sample response, half-LSB rounded to 16 bits, 5 to 13 clock cycles later. A new output data word is available every clock cycle. The figure shows that the input data are automatically right-shifted one location through the row of multiplier input

registers on every clock in anticipation of a new input data word.

$$\begin{aligned} \text{CASOUT}(13) = & A(9)KA3(9) + A(8)KA2(8) + A(7)KA1(7) \\ & + B(6)KB3(9) + B(5)KB2(8) + B(4)KB1(7) \\ & + B(3)KC3(9) + B(2)KC2(8) + B(1)KC1(7) \\ & + \text{CASIN}(10) \end{aligned}$$

Latency: Impulse in to center of 9-tap response = 9 registers. Cascade In to Cascade Out = 4 registers.

Figure 3. 9-Tap FIR Filter Impulse Response (Mode 01)

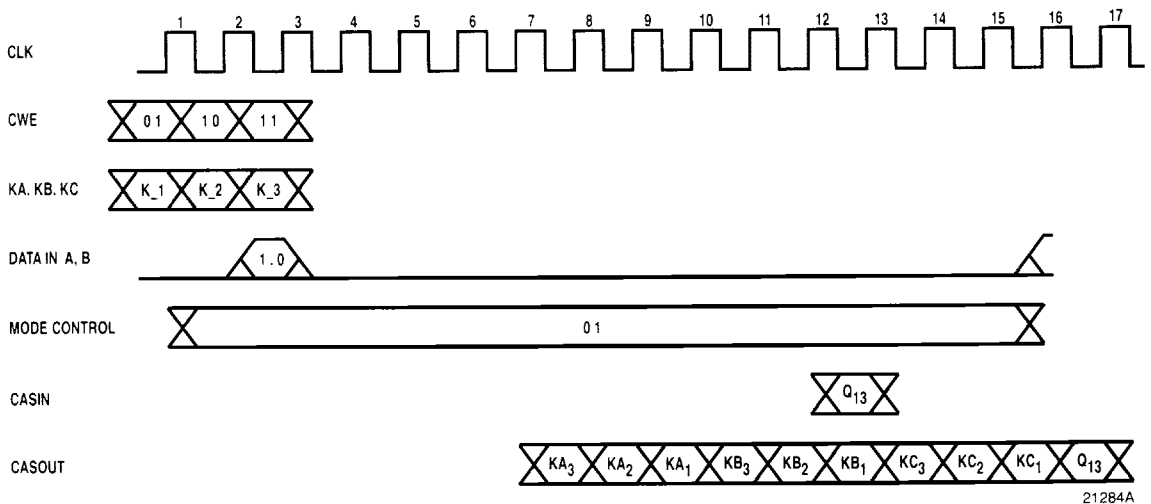
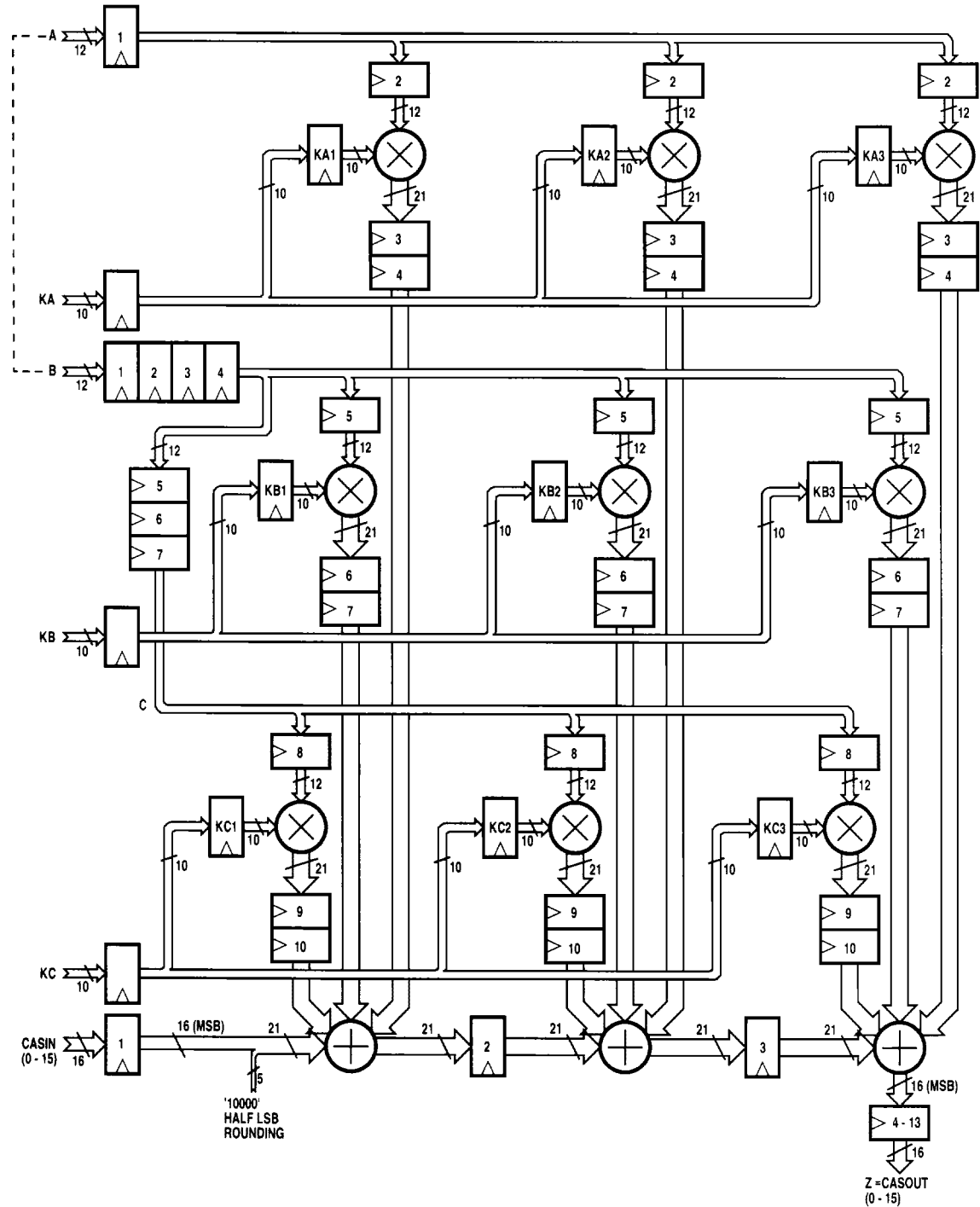


Figure 4. 9-Tap FIR Filter Configuration (Mode 01)



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3 x 3-Pixel Convolver (Mode 10)

This filter configuration accepts a 3-pixel-square neighborhood, side-loaded three pixels at a time through input ports A, B, and C, and multiplies the 9 most recent pixel values by the coefficient set currently stored in the registers. These products are summed with the data presented to the cascade input, and a new 3-cycle impulse response, rounded to 16 bits, is available at the output port 5-7 clocks later, with a new output available on every clock cycle. The input pixel data are automatically shifted one location to the right through the three rows of multiplier input registers on every clock in

anticipation of three new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned} \text{CASOUT}(7) = & A(3)KA3(3) + A(2)KA2(2) + A(1)KA1(1) \\ & + B(3)KB3(3) + B(2)KB2(2) + B(1)KB1(1) \\ & + C(3)KC3(3) + C(2)KC2(2) + C(1)KC1(1) \\ & + \text{CASIN}(4) \end{aligned}$$

Latency: Impulse in to center of 3-tap response = 6 registers. Cascade In to Cascade Out = 4 registers.

Figure 5. 3 x 3-Pixel Convolver Impulse Response (Mode 10)

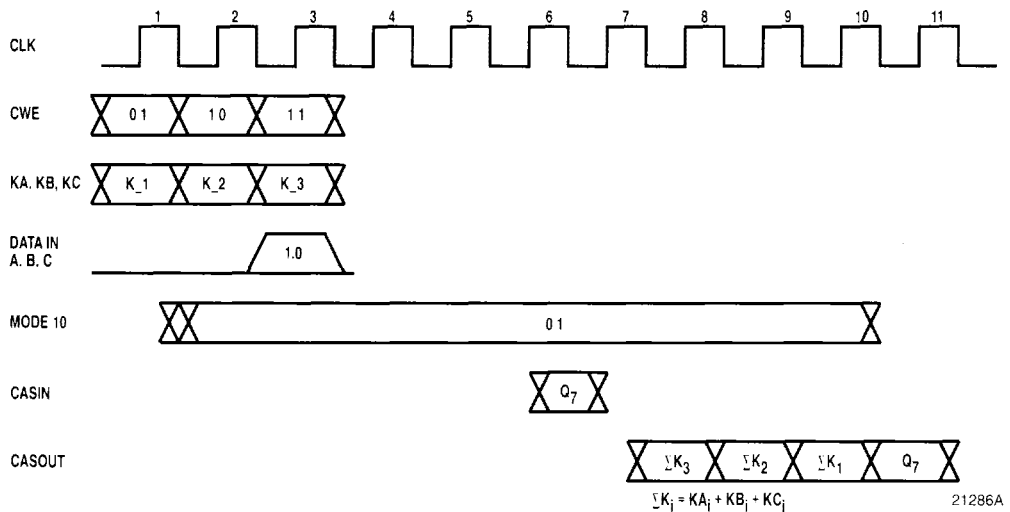
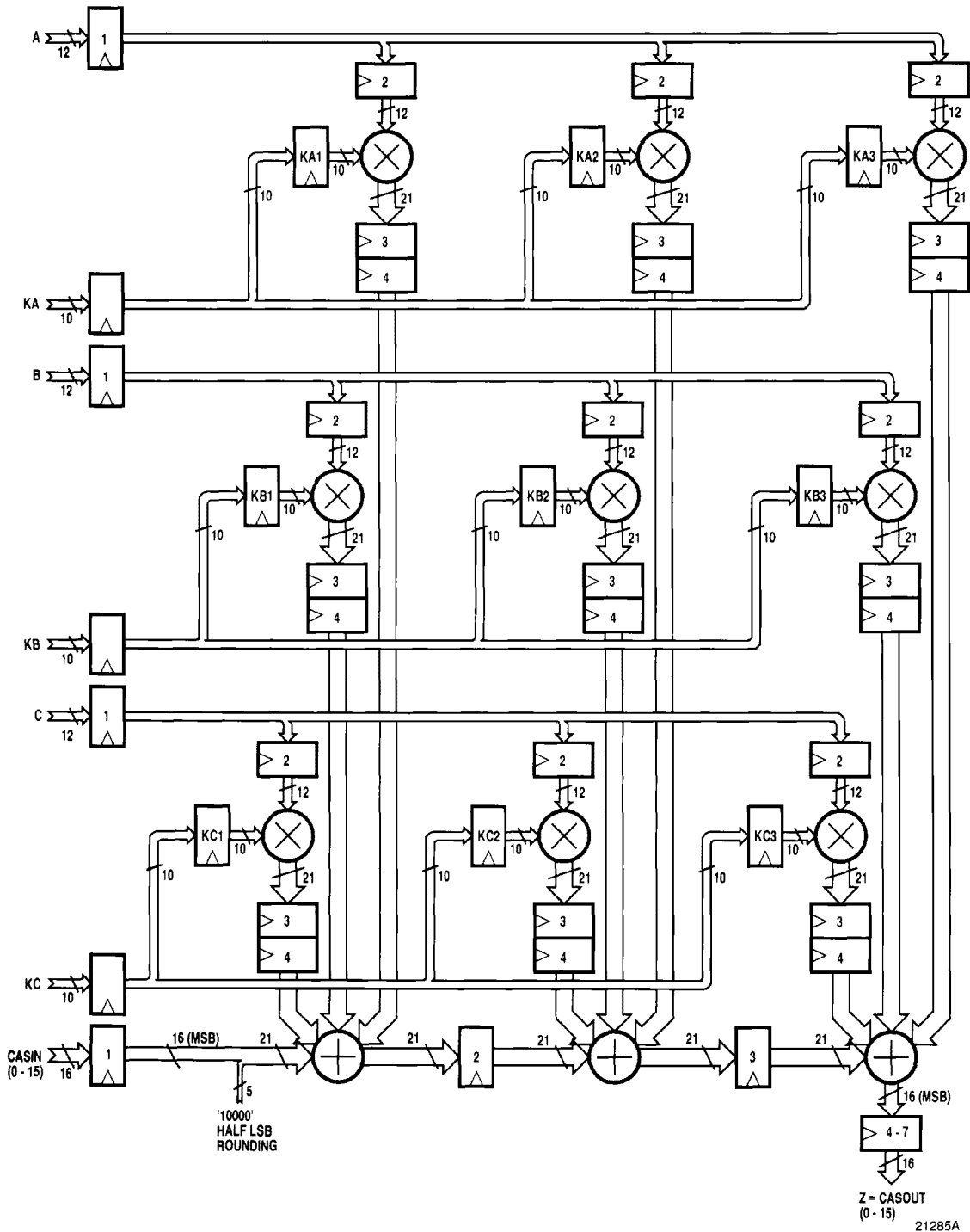


Figure 6. 3 x 3-Pixel Convolver Configuration (Mode 10)



4 x 2-Pixel Cascadeable Convolver (Mode 11)

Similar to Mode 10, the 4 x 2-pixel convolver allows the user to perform full-speed cubic convolution with only two TMC2250 devices and the TMC2111 Pipeline Delay Register to synchronize the cascade ports (see the *Applications Discussion* section). Pixel data are side-loaded into ports A and B, multiplied by the onboard coefficients, summed with the cascade input, and half-LSB rounded to 16 bits. The four-cycle impulse response emerges at the cascade output port 5 to 8 clock cycles later. A new output word is available on every clock cycle. Note that Multiplier KC2 is not used in this mode

and that its stored coefficient is ignored. As shown below, the column of input pixel data is automatically shifted one location to the right through the two rows of multiplier input registers on every clock in anticipation of two new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned} \text{CASOUT}(8) = & A(4)KA3(4) + A(3)KA2(3) + A(2)KA1(2) \\ & + A(1)KB3(4) + B(4)KB3(4) + B(3)KB2(3) \\ & + B(2)KB1(2) + B(1)KC1(2) + \text{CASIN}(5) \end{aligned}$$

Figure 7. 4 x 2-Pixel Convolver Impulse Response (Mode 11)

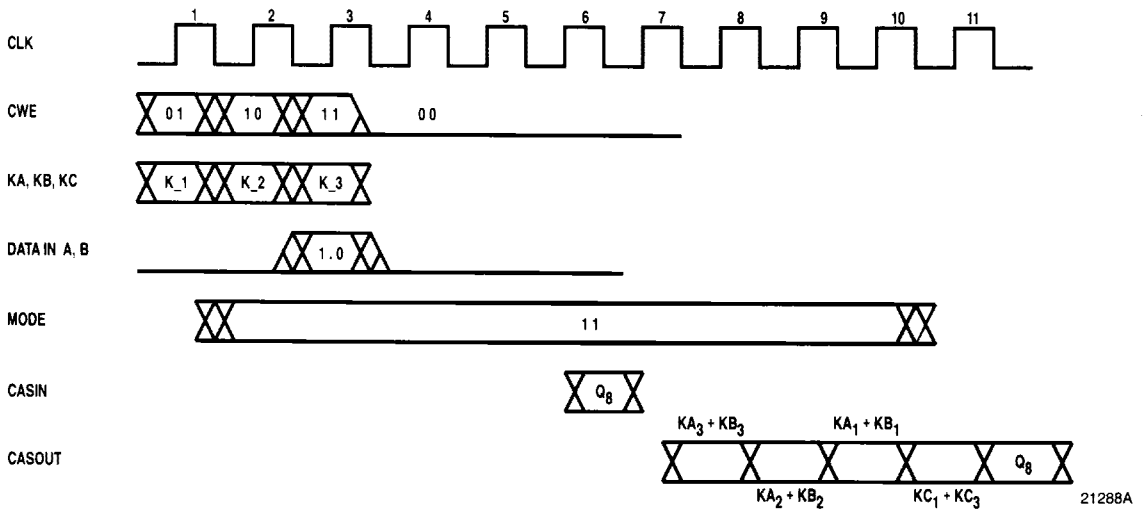
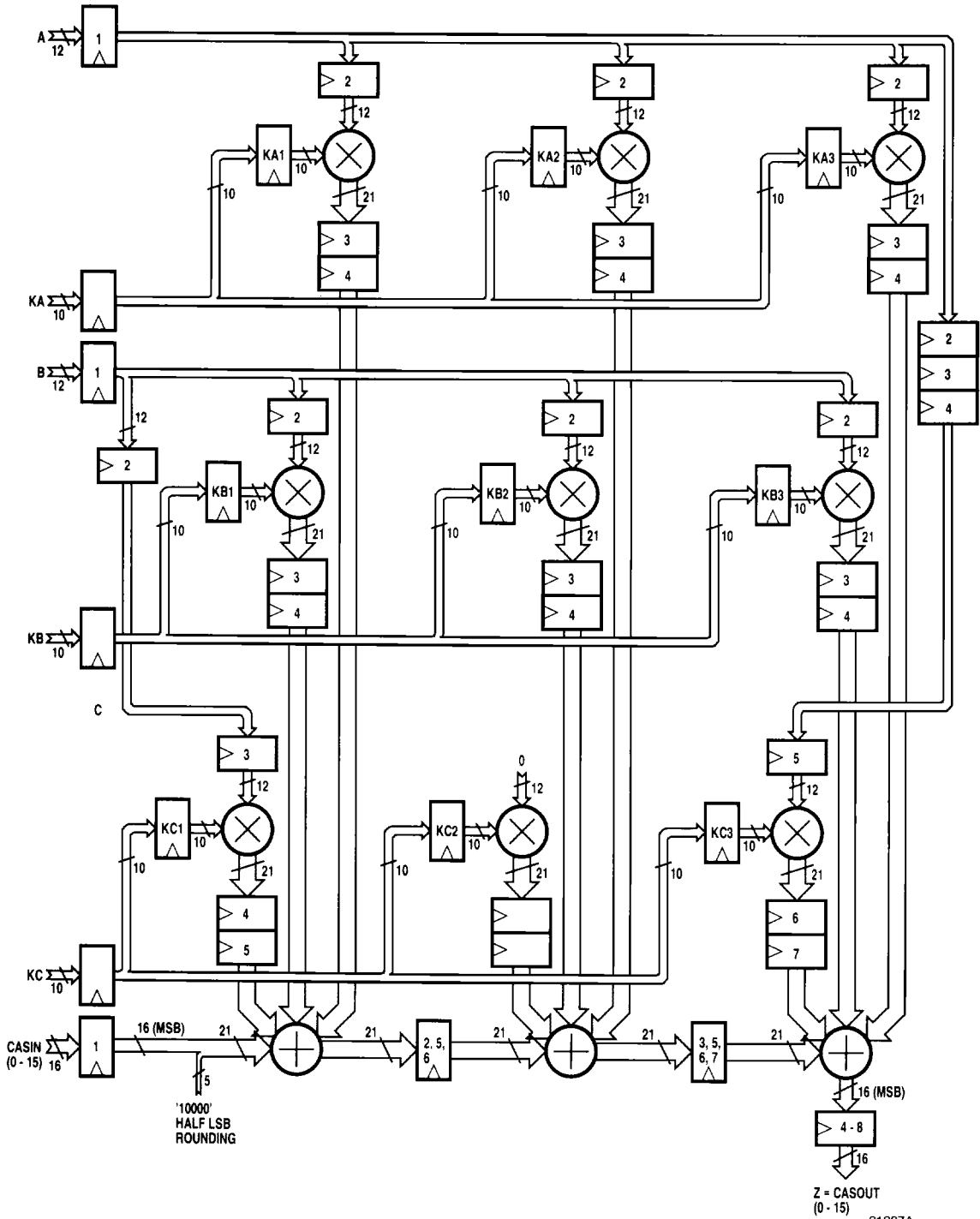


Figure 8. 4 x 2-Pixel Convolver Configuration (Mode 11)



Signal Definitions (cont.)

Controls

MODE_{1,0} The TMC2250 will switch to the configuration selected by the user (as shown in *Table 3*) on the next clock. This registered control is usually static; however, should the user wish to switch between modes, the internal pipeline latencies of the device must be taken into account. Valid data will not be available at the outputs in the new configuration until enough clocks in the new mode have passed to flush the internal registers.

Table 3. Configuration Mode Word

MODE _{1,0}	Configuration Mode
00	3 x 3 Matrix Multiply
01	9-Tap One-Dimensional FIR
10	3 x 3-Pixel Convolver
11	4 x 2-Pixel Convolver

CWE_{1,0} Data presented to the coefficient input ports (KA, KB, and KC) will update three of the internal coefficient storage registers, as indicated by the simultaneous Coefficient Write Enable select, on the next clock. See *Table 4* and the *Functional Block Diagram*.

Table 4. Coefficient Write Enable Word

CWE _{1,0}	Coefficient Set Selected
00	Hold all registers
01	Update KA1, KB1, KC1
10	Update KA2, KB2, KC2
11	Update KA3, KB3, KC3

Table 5. Coefficient Input Ports

Input Port	Registers Available
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

Inputs And Outputs

A₁₁₋₀, B₁₁₋₀, C₁₁₋₀ Data presented to the 10-bit registered data input ports A, B, and C are latched into the multiplier input registers for the currently selected configuration (*Table 3*). In all modes except Mode 00, new data are internally right-shifted to the next filter tap on each rising edge of CLK.

KA₉₋₀, KB₉₋₀, KC₉₋₀ Data presented to the 10-bit registered coefficient input ports KA, KB, and KC are latched three at a time into the internal coefficient storage register set indicated by the Coefficient Write Enable **CWE_{1,0}** on the next clock, as shown in *Table 4*.

CASIN₁₅₋₀ In all modes except Mode 00, the x port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Input port **CASIN₁₅₋₀**. Data presented to this input will be added to the weighted sums of the data words which were presented to the input ports (A, B, and C).

X₁₁₋₀, Y₁₁₋₀, Z₁₁₋₀ In the matrix multiply mode, data are available at the 12-bit registered output ports X, Y, and Z t_{DQ} after every clock. These ports are reconfigured in the filtering modes as 16-bit Cascade Input and Output ports.

NOTE: The output ports X, Y, Z and CASOUT, and the input port CASIN are internally reconfigured by the device as required for each mode of the device. The multiple-function pins have names which are combinations of these titles, as appropriate.

CASOUT₁₅₋₀ In all modes except Mode 00, the Z port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Output port **CASOUT₁₅₋₀**.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins
Power	V _{DD}	Supply Voltage	F3, H3, L7, C8, C4
	GND	Ground	E3, G3, J3, L4, L6, H11, C7, C5
Clock	CLK	System Clock	D11
Controls	MODE _{1,0}	Mode Control	B5, A4
	CWE _{1,0}	Coefficient Write Enable	J12, J13
Input/Output	A ₁₁₋₀	Data Input A	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12
	B ₁₁₋₀	Data Input B	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12
	C ₁₁₋₀	Data Input C	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9
	KA ₉₋₀	Coefficient Input A1, A2, A3	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13
	KB ₉₋₀	Coefficient Input B1, B2, B3	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8
	KC ₉₋₀	Coefficient Input C1, C2, C3	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5
	XC ₁₁₋₀	CASIN ₁₅₋₄ /Output X	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2
	YC ₁₁₋₈	CASIN ₃₋₀ /Output Y ₁₁₋₀	D1, E2, E1, F2
	Y ₇₋₄	Output Y ₇₋₄ Only	F1, G2, G1, H1
	YC ₃₋₀	CASOUT ₃₋₀ /Output Y ₃₋₀	K1, J2, J1, H2
ZC ₁₁₋₀	CASOUT ₁₅₋₄ /Output Z ₁₁₋₀	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2	

Figure 9. Input/Output Timing Diagram

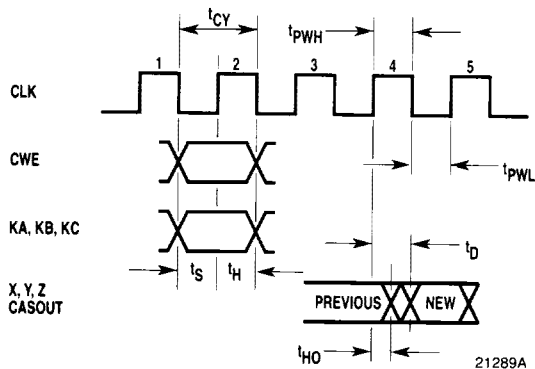


Figure 10. Equivalent Input Circuit

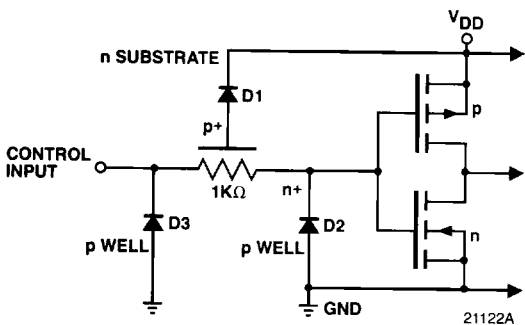
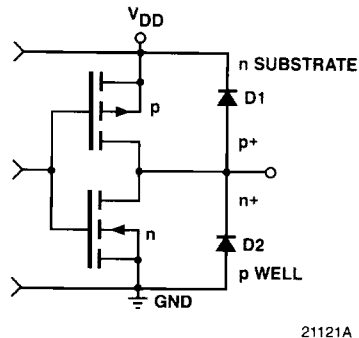


Figure 11. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) ¹

Supply Voltage	-0.5 to +7.0V
Input Voltage	-0.5 to (V _{DD} +5.0)V
Output	
Applied voltage	-0.5 to (V _{DD} +5.0)V ²
Forced current	-6.0 to 6.0mA ^{3,4}
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	-60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	-65 to 150°C

- Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
 2. Applied voltage must be current limited to specified range, and measured with respect to GND.
 3. Forcing voltage must be limited to specified range.
 4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter	Temperature Range						Units
	Standard			Extended			
	Min	Nom	Max	Min	Nom	Max	
V _{DD} Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V _{IL} Input Voltage, Logic LOW			0.8			0.8	V
CLK Only			0.8			0.6	V
V _{IH} Input Voltage, Logic HIGH	2.0			2.0			V
I _{OL} Output Current, Logic LOW			4.0			4.0	mA
I _{OH} Output Current, Logic HIGH			-2.0			-2.0	mA
t _{CY} Cycle Time							
TMC2250	33			33			ns
TMC2250-1	27.7			27.7			ns
TMC2250-2	25						ns
t _{PWL} Clock Pulse Width, LOW							
TMC2250	15			15			ns
TMC2250-1	12			12			ns
TMC2250-2	10						ns
t _{PWH} Clock Pulse Width, HIGH	10			10			ns
t _S Input Setup Time							
TMC2250	8			8			ns
TMC2250-1	7			7			ns
TMC2250-2	6						ns
t _H Input Hold Time							
TMC2250	3			3			ns
TMC2250-1	3			3			ns
TMC2250-2	2						ns
T _A Ambient Temperature, Still Air	0		70				°C
T _C Case Temperature				-55		125	°C

Electrical characteristics within specified operating conditions¹

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
I_{DDQ} Supply Current, Quiescent	$V_{DD} = \text{Max}, V_{IN} = 0V$		12		12	mA
I_{DDU} Supply Current, Unloaded	$V_{DD} = \text{Max}, f = 20\text{MHz}$		160		160	mA
I_{IL} Input Current, Logic LOW ²	$V_{DD} = \text{Max}, V_{IN} = 0V$		-10		-10	μA
I_{IH} Input Current, Logic HIGH ²	$V_{DD} = \text{Max}, V_{IN} = V_{DD}$		10		10	μA
I_{OIL} Input Current, Logic LOW ³	$V_{DD} = \text{Max}, V_{IN} = 0V$		-40		-40	μA
I_{OIH} Input Current, Logic HIGH ³	$V_{DD} = \text{Max}, V_{IN} = V_{DD}$		40		40	μA
V_{OL} Output Voltage, Logic LOW	$V_{DD} = \text{Min}, I_{OL} = 4\text{mA}$		0.4		0.4	V
V_{OH} Output Voltage, Logic HIGH	$V_{DD} = \text{Min}, I_{OH} = -2\text{mA}$	2.4		2.4		V
I_{OS} Short-Circuit Output Current	$V_{DD} = \text{Max}$, Output HIGH, one pin to to ground, one second duration max.	-20	-80	-20	-80	mA
C_I Input Capacitance	$T_A = 25^\circ\text{C}, f = 1\text{MHz}$		10		10	pF
C_O Output Capacitance	$T_A = 25^\circ\text{C}, f = 1\text{MHz}$		10		10	pF

- Notes:
- 1 Actual test conditions may vary from those shown but guarantee operation as specified.
 - 2 Except pins XC11-0, YC11-8.
 - 3 Pins XC11-0, YC11-8 only.

Switching characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range				Units	
		Standard		Extended			
		Min	Max	Min	Max		
t_D Output Delay	$V_{DD} = \text{Min}, C_{LOAD} = 25\text{pF}$		18		20	ns	
		TMC2250-1		17		18	ns
		TMC2250-2		16			ns
t_{HO} Output Hold Time	$V_{DD} = \text{Max}, C_{LOAD} = 25\text{pF}$		4		4	ns	
		TMC2250-1		3		3	ns
		TMC2250-2		3			ns



Applications Discussion

Converting Video Data from RGB to YIQ or YUV

The TMC2250 simplifies the task of converting encoded color video data between the RGB (color component) format and the YIQ (quadrature encoded chrominance) or YUV (color difference) format. Beginning with RGB component data, the standard relationships, with 8-bit quantization, are:

$$\begin{aligned}
 Y &= (77R + 150G + 29B)/256 & \text{and} & & Y &= (77R + 150G + 29B)/256 \\
 I &= (153R - 71G - 82B)/256 + 128 & & & U &= (131R - 110G - 21B)/256 + 128 \\
 Q &= (54R - 134G + 80B)/256 + 128 & & & V &= (-44R - 87G + 131B)/256 + 128
 \end{aligned}$$

In digital systems, I and Q or U and V are sometimes renormalized to:

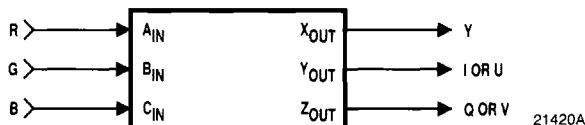
$$\begin{aligned}
 I &= (128R - 59G - 69B)/256 \\
 Q &= (52R - 128G + 76B)/256 \\
 U &= (128R - 107G - 21B)/256 \\
 V &= (-43R - 85G + 128B)/256
 \end{aligned}$$

With each coefficient expressed as a fraction of 256, these numbers are easily converted to binary for loading into the coefficient storage of the TMC2250. The half-scale (80_{hex}) offsets included in the chrominance and color-difference terms can easily be added to the appropriate sums after the matrix multiplication, if desired. **Table 6** contains the 10-bit two's complement coefficients to be loaded into the TMC2250 to perform the desired conversion from RGB format. Once these factors are in place the user can continuously convert encoded data at real-time video rates, with three new encoded outputs available on every clock cycle.

Table 6. Colorspace Conversion Coefficients ^{1, 2}

Conversion	KA1	KA2	KA3	KB1	KB2	KB3	KC1	KC2	KC3
RGB to YIQ	04D	099	036	096	3B9	37A	01D	3AE	050
RGB to YIQ ³	04D	080	034	096	3C5	380	01D	3BB	04C
RGB to YUV	04D	083	3D4	096	392	3A9	01D	3EB	083
RGB to YUV ³	04D	080	3D5	096	395	3AB	01D	3EB	080

- Notes: 1. All entries are given in 10-bit two's complement hexadecimal, such that all entries beginning in "2" or "3" are negative.
 2. This table assumes the following bus assignments:



3. Second and fourth entries are renormalized such that largest coefficient = .5 (080_{hex}).

Converting Video Data from YIQ or YUV to RGB

With a different set of coefficients, the TMC2250 can perform the inverse conversions, whose governing equations are:

$$\begin{aligned}
 R &= (256Y + 243I + 159Q) / 256 & \text{and} & & R &= (256Y + 0U + 292V) / 256 \\
 G &= (256Y - 72I - 164Q) / 256 & & & G &= (256Y - 101U - 149V) / 256 \\
 B &= (256Y - 284I + 443Q) / 256 & & & B &= (256Y + 520U + 0V) / 256
 \end{aligned}$$

The values corresponding to digital normalization (see *Converting Video Data from RGB to YIQ or YUV*) are:

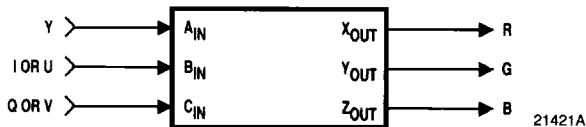
$$\begin{aligned}
 R &= 256Y + 292I + 167Q) / 256 & \text{and} & & R &= (256Y + 0U + 359V) / 256 \\
 G &= (256Y - 86I - 172Q) / 256 & & & G &= (256Y - 88U - 183V) / 256 \\
 B &= (256I - 341I + 456Q) / 256 & & & B &= (256Y + 453U + 0V) / 256
 \end{aligned}$$

Since the first YUV to RGB equation set includes the coefficient "520," which won't fit into a 10-bit two's complement integer format, we must either divide all coefficients by 2, degrading precision by one bit, or by 520/511. In *Table 7*, the 520/511 correction factor was selected.

Table 7. Colorspace Conversion Coefficients ^{1, 2}

Conversion	KA1	KA2	KA3	KB1	KB2	KB3	KC1	KC2	KC3
YIQ to RGB	100	100	100	0F3	3B8	3E4	09F	35C	1BB
YIQ to RGB ³	100	100	100	124	3AA	2AB	0A7	354	101
YUV to RGB	0FC	0FC	0FC	000	39D	1FF	11F	36E	000
YUV to RGB ³	100	100	100	000	3A8	125	167	349	000

- Notes:
1. All entries are given in 10-bit two's complement hexadecimal, such that all entries beginning in "2" or "3" are negative.
 2. This table assumes the following bus assignments:

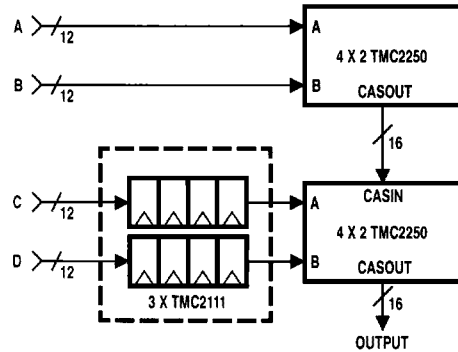


3. Second and fourth entries are renormalized such that largest coefficient = .5 (080_{hex}).

Performing Large-Kernel Pixel Interpolation

The Cascade Input and Output Ports of the TMC2250 allow the user to stack multiple devices to perform larger interpolation kernels with no decrease in pixel throughput. **Figure 12** illustrates a basic application utilizing Mode 11 to realize a 4 x 4-pixel kernel, also called Cubic Convolution. This example utilizes the TMC2011 Variable-Length Shift Register to compensate for the internal latency of each TMC2250. Alternatively, some applications may utilize RAM, FIFOs, or other methods to store multiple-line pixel data. In these cases the user may compensate for latency by simply offsetting the access sequencing of the storage devices.

Figure 12. Performing Cubic Convolution with Two TMC2250s

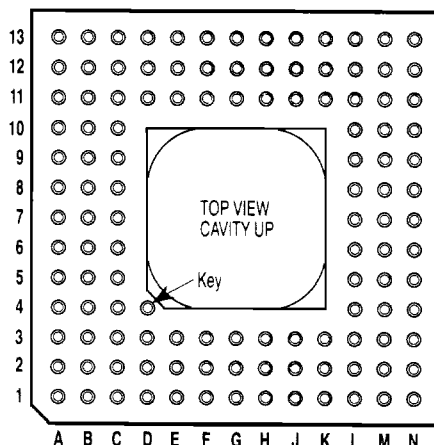


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Pin Assignments — 121 Pin Plastic (H5) or Ceramic (G1) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	XC ₇	B3	XC ₈	C5	GND	E1	YC ₉	G11	A ₃	K1	YC ₃	L10	KB ₈	M12	KA ₂
A2	XC ₉	B4	XC ₁₁	C6	C ₁₀	E2	YC ₁₀	G12	A ₂	K2	ZC ₀	L11	KA ₁	M13	KA ₃
A3	XC ₁₀	B5	MODE ₁	C7	GND	E3	GND	G13	A ₄	K3	ZC ₃	L12	KA ₅	N1	ZC ₅
A4	MODE ₀	B6	C ₉	C8	V _{DD}	E11	A ₁₁	H1	Y ₄	K11	KA ₄	L13	KA ₆	N2	ZC ₈
A5	C ₁₁	B7	C ₆	C9	C ₀	E12	A ₉	H2	YC ₀	K12	KA ₇	M1	ZC ₂	N3	ZC ₁₀
A6	C ₈	B8	C ₄	C10	B ₈	E13	A ₈	H3	V _{DD}	K13	KA ₉	M2	ZC ₇	N4	KC ₁
A7	C ₇	B9	C ₂	C11	B ₅	F1	Y ₇	H11	GND	L1	ZC ₁	M3	ZC ₉	N5	KC ₃
A8	C ₅	B10	B ₁₁	C12	B ₃	F2	YC ₈	H12	A ₀	L2	ZC ₄	M4	ZC ₁₁	N6	KC ₅
A9	C ₃	B11	B ₉	C13	B ₁	F3	V _{DD}	H13	A ₁	L3	ZC ₆	M5	KC ₂	N7	KC ₇
A10	C ₁	B12	B ₆	D1	YC ₁₁	F11	A ₇	J1	YC ₁	L4	GND	M6	KC ₄	N8	KC ₈
A11	B ₁₀	B13	B ₂	D2	XC ₀	F12	A ₆	J2	YC ₂	L5	KC ₀	M7	KC ₆	N9	KB ₁
A12	B ₇	C1	XC ₁	D3	XC ₃	F13	A ₅	J3	GND	L6	GND	M8	KC ₉	N10	KB ₃
A13	B ₄	C2	XC ₂	D11	CLK	G1	Y ₅	J11	KA ₈	L7	V _{DD}	M9	KB ₂	N11	KB ₆
B1	XC ₄	C3	XC ₆	D12	B ₀	G2	Y ₆	J12	CWE ₁	L8	KB ₀	M10	KB ₅	N12	KB ₇
B2	XC ₅	C4	V _{DD}	D13	A ₁₀	G3	GND	J13	CWE ₀	L9	KB ₄	M11	KB ₉	N13	KA ₀

D4 Index Pin (Unconnected)



21041A

Ordering Information

Product Number	Speed (MHz)	Temperature Range	Screening	Package	Package Marking
TMC2250H5C	30	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C
TMC2250H5C-1	36	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C-1
TMC2250H5C-2	40	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C-2
TMC2250G1V	30	MIL- $T_C = -55^{\circ}\text{C}$ to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V
TMC2250G1V1	36	MIL- $T_C = -55^{\circ}\text{C}$ to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V1

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