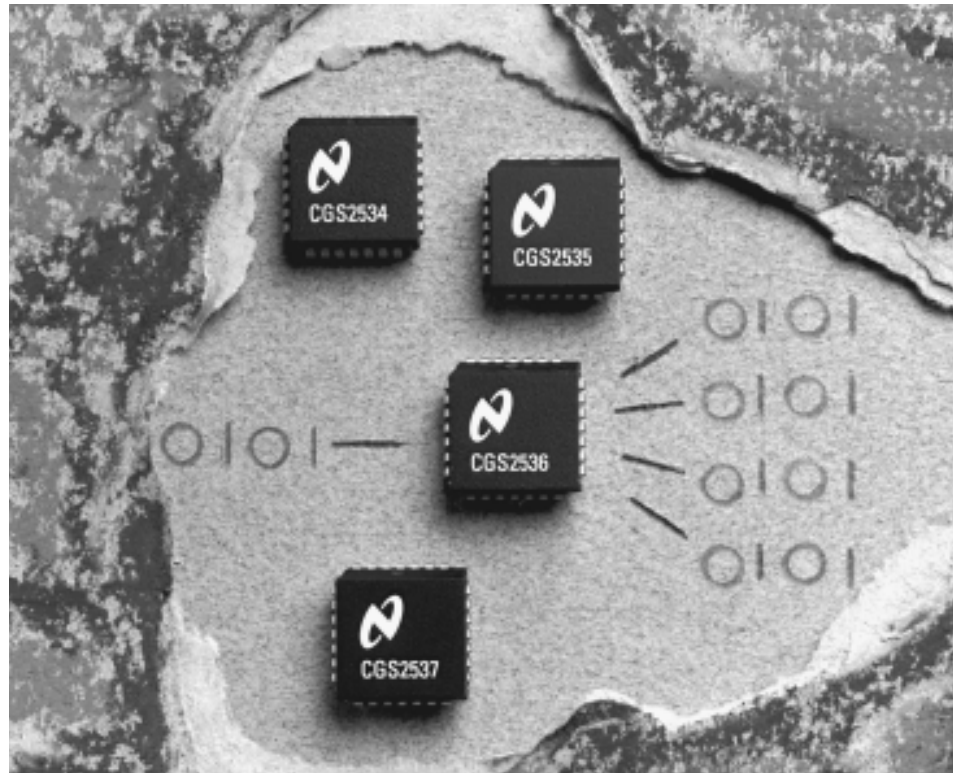


CGS253x Quad 1 to 4 Clock Drivers

- Pin-to-Pin Skew of Less Than 350 ps
- Part-to-Part Skew of Less Than 650 ps
- Output Series Resistor Integrated Into CGS2537
- Supports TTL and CMOS Output Clock Rates to 125 MHz
- Accepts TTL and CMOS Inputs
- Maximum Propagation Delays of 3.5 to 4.5 ns
- Greater Than 125 MHz Maximum Frequency
- 5V/3.3V Options
- 1X and 0.5X Output Capability

National Semiconductor's Clock Generation and Support (CGS*) family offers you a complete portfolio of clock generation and distribution timing solutions. The newest family of high performance clock drivers offers you the highest performance and flexibility available in a cost-effective device – High speed as measured by maximum frequency, accuracy as measured by skew, and flexibility as measured by supply voltages and output configurations. National's clock drivers save time and effort by offering synchronous signals that reduce timing errors and system failures. These clock drivers also integrate output series resistors that reduce undershoot and simplify line termination design. They further aid designers by offering high fanout that reduces component count and saves board real estate. In addition, for today's mixed voltage systems, the inputs are 5V tolerant when using a 3.3V supply. National's CGS253x family of clock drivers (CGS2534V/CGS2535V/CGS2536V/CGS2537V) is optimized to drive large loads with sub-3.5ns propagation delays, 1.5ns edge rates, and 36mA drive.

IBIS models for the CGS253x, along with all of National's clock generators and drivers, can be downloaded (via FTP) from the Internet at vhdl.org, where all of the semiconductor industry's IBIS models are



located. In addition, one can access the models at URL: <http://www/vhdl.org/pub/ibis> (and click on 'models' and 'national') or using a modem to dial up (415) 335-0110. IBIS (I/O Buffer Information Specification) is a fast and accurate behavioral method of modeling I/O buffers based on V/I curve data derived from measurements or full circuit simulation. IBIS uses a standardized software parsable format to create the behavioral information needed to model analog characteristics of ICs and can be used by almost any analog simulator/EDA tool in the industry. IBIS is developed by the IBIS Open Forum and most forum activities are handled through email discussions using the reflector ibis@vhdl.org.

PROCESSORS SUPPORTED:
80186, 80C186, 80C186XL/EA/EB/EC, 80L186EA/EB/EC, 80188, 80C188, 80C188XL/EA/EB/EC, 80L188EA/EB/EC, Intel386™ CX/EX/SX/SXSA/DX, and Intel486™ SX, IntelDX2™, IntelDX4™ Processors

AVAILABILITY:
Now

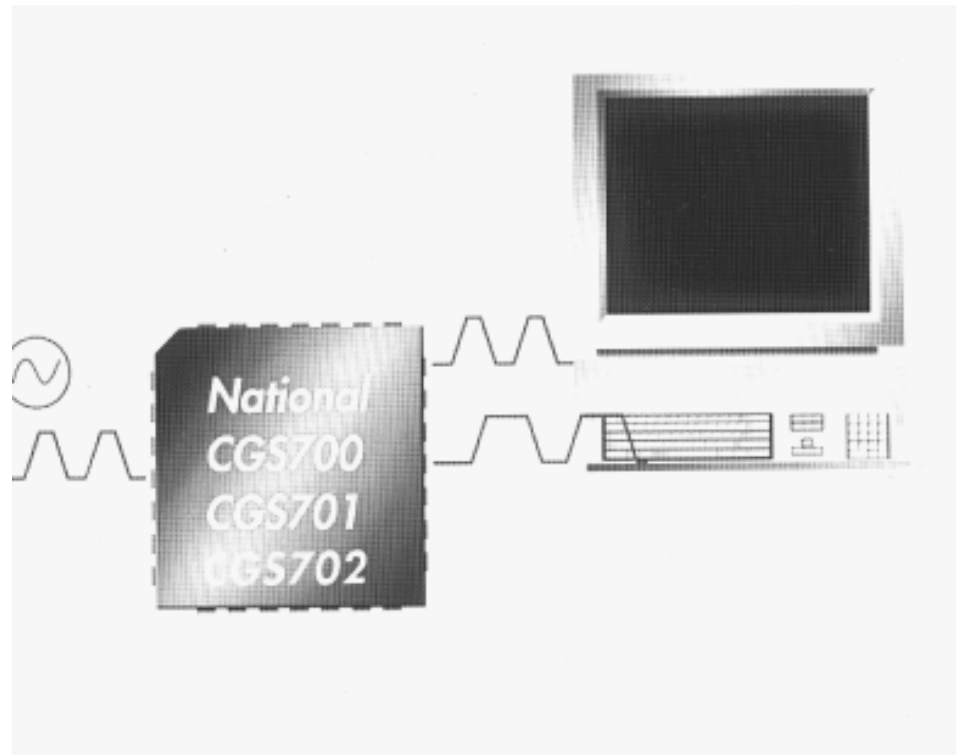
CONTACT:
National Semiconductor
Phone: (800) 272-9959
For international contacts see Appendix B.

CGS70x Low Skew Clock Generators

- Up to 9 CMOS Clock Outputs
- 25-160 MHz Output Frequency Range
- Less Than 400 ps Pin-to-Pin Skew
- Supports Clock Doubling and Quadrupling
- Internal Phase Locked Loop (PLL) With VCO Operating Greater Than 160 MHz
- CGS702 Has Reduced EMI
- Sub-300 ps Long Term Jitter
- 30mA Drive
- PLCC Packaging For Optimum Skew Performance

National Semiconductor's Clock Generation and Support (CGS*) family offers a complete portfolio of clock generation and distribution timing solutions for all embedded Intel Architecture microprocessors. National's newest family of high performance clock generators offers high performance and flexibility in a cost-effective device. The CGS700V/701V/702V have on-chip PLLs that are used to generate 25-160 MHz outputs from 25-40 MHz inputs. The CGS701 has external feedback for output edge placement control.

IBIS models for the CGS70x, along with all of National's clock generators and drivers, can be downloaded (via FTP) from the Internet at vhdl.org, where all of the semiconductor industry's IBIS models are located. In addition, one can access the models at URL: <http://www/vhdl.org/pub/ibis> (and click on 'models' and 'national') or using a modem to dial up (415) 335-0110. IBIS (I/O Buffer Information Specification) is a fast and accurate behavioral method of modeling I/O buffers based on V/I curve data derived from measurements or full circuit simulation. IBIS uses a standardized software parsable format to create the behavioral information needed to model analog characteristics of ICs and can be used by almost any analog simulator/EDA tool in the industry. IBIS is developed by



the IBIS Open Forum and most forum activities are handled through e-mail discussions using the reflector ibis@vhdl.org.

PROCESSORS SUPPORTED:
80186, 80C186, 80C186XL/EA/EB/EC, 80L186EA/EB/EC, 80188, 80C188, 80C188XL/EA/EB/EC, 80L188EA/EB/EC, Intel386™ CX/EX/SX/SXSA/DX, and Intel486™ SX, IntelDX2™, IntelDX4™ Processors

AVAILABILITY:

Now

CONTACT:

National Semiconductor

Phone: (800) 272-9959

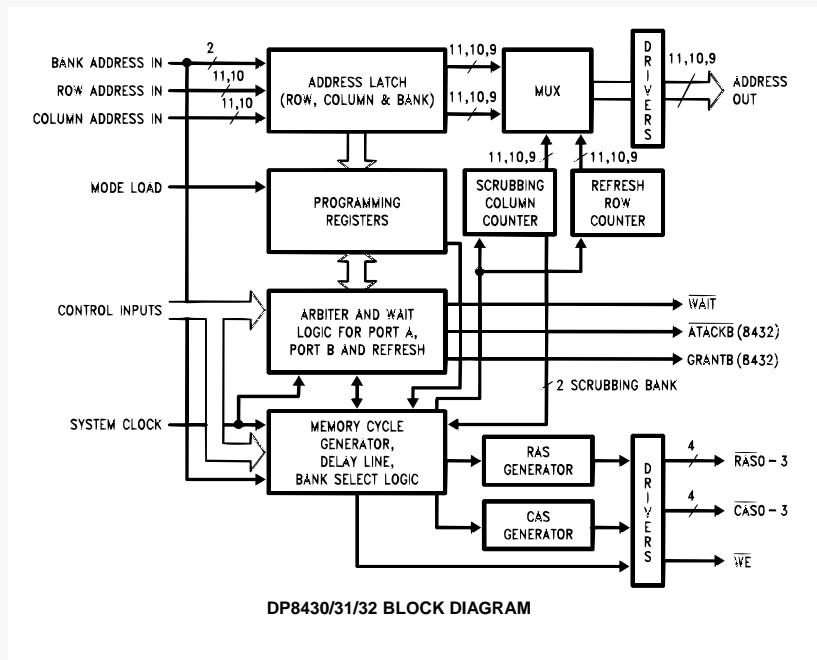
For international contacts see Appendix B.

DP843x Programmable DRAM Controllers

- Supports Nibble, Page, and Static Column DRAMs
- 33 MHz Operation
- Dual Access Ports (DP8432 only)
- Addresses Up to 64MB DRAM Arrays
- Supports Up to 4MB DRAMs
- 4 RAS and 4 CAS Drivers

The DP8430V/31V/32V DRAM controllers provide a low cost, single chip interface between DRAM and all embedded Intel Architecture microprocessors. The DP8430V/31V/32V generate all the required access control signal timing for DRAMs and an on-chip refresh request clock is used to automatically refresh the DRAM array. Refreshes and accesses are arbitrated on chip. If necessary, a WAIT or DTACK output inserts wait states into system access cycles, including burst mode accesses. RAS low time during refreshes and RAS precharge time after refreshes and back to back accesses are guaranteed through the insertion of wait states. Separate on-chip precharge counters for each RAS output can be used for memory interleaving to avoid delayed back to back accesses because of precharge. An additional feature of the DP8432V is two access ports to simplify dual accessing. Arbitration among these ports and refresh is done on chip.

The DP8430V and DP8431V are available in a 68-pin PLCC package while the DP8432V is available in an 84-pin PLCC package. All are available in 33 MHz speeds.



PROCESSORS SUPPORTED:

80186, 80C186, 80C186XL/EA/EB/EC, 80L186EA/EB/EC, 80188, 80C188, 80C188XL/EA/EB/EC, 80L188EA/EB/EC, Intel386™ CX/EX/SX/SXSA/DX, and Intel486™ SX, IntelDX2™, IntelDX4™ Processors

AVAILABILITY:

Now

CONTACT:

National Semiconductor

Phone: (800) 272-9959

For international contacts see Appendix B.

DP844x Programmable DRAM Controllers

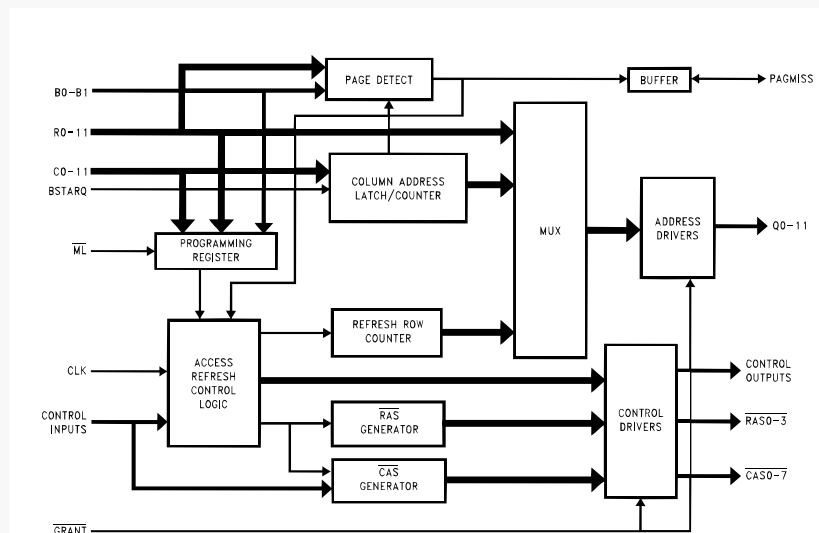
- 25 MHz and 40 MHz Operation
- Supports Up to 64-Bit Bus Widths
- Addresses Up to 1/2 GB of Memory
- Supports Up to 64MB DRAMs
- Supports Fast Page, Nibble, and Static Column DRAMs
- Page Detection
- Automatic CPU Burst Accesses
- Automatic Internal Refresh
- Burst and RAS-Before-CAS Refresh

National Semiconductor's DP8440 and DP8441 DRAM Controllers provide an easy interface between DRAM arrays and embedded Intel Architecture microprocessors. These DRAM Controllers generate all necessary control and timing signals to successfully interface and design dynamic memory systems and support page and burst accesses for fast page, static column, and nibble DRAMs.

The DP8440 supports DRAMs as large as 16MB with a maximum addressable space of 256MB while the DP8441 can support 64MB DRAMs with a maximum addressable space of 1/2 GB. Both devices support microprocessor bus widths of up to 32-bits while the DP8441 supports 64-bit bus widths as well.

Programmable features make the DP8440/41 flexible enough to fit many memory systems. These controllers include page comparators, burst mode support, and CAS-before-RAS refresh features. Burst length is programmable on both chips. They also include on-chip Phase-Locked Loops (PLLs) which provide a high-precision delay line that generates sub-clock cycle delays to improve system performance. Because the CMOS circuits support high-capacitance drive capabilities, system designers are not required to add memory buffers.

Both devices are available in 25 MHz and 40 MHz versions and are packaged in a 100-pin PQFP package. Additionally, the DP8440 is also available in a 84-pin PLCC package (40 MHz version only).



DP8440/41 BLOCK DIAGRAM

PROCESSORS SUPPORTED:

80186, 80C186,
80C186XL/EA/EB/EC,
80L186EA/EB/EC, 80188, 80C188,
80C188XL/EA/EB/EC,
80L188EA/EB/EC, Intel386™
CX/EX/SX/SXSA/DX, and Intel486™
SX,
IntelDX2™, IntelDX4™ Processors

AVAILABILITY:

Now

CONTACT:

National Semiconductor
Phone: (800) 272-9959
For international contacts see Appendix B.

Intel Architecture and ISA Compatible Solutions

PCMCIA Host Adapters

- VG365
 - Dual Socket PC Card Controller
- VG465
 - Single Socket PC Card Controller
- VG468
 - Single Socket PC Card Controller
- VG469
 - Dual Socket Mixed Voltage PC Card Controller

VGA LCD/CRT Controller

- VG660
 - 100 Pin Low Cost VGA LCD/CRT Controller

Vadem's PCMCIA Host Adapters, VG465, VG365, VG468 and VG469 offer full compatibility with Intel's ExCA and PCMCIA, and are Intel "B" step register set and software compatible. Vadem's PCMCIA controllers offer OEMs an easy and safe upgrade path to mixed voltage systems and plug-and-play standards. They also are designed to help end-users easily use the standard. Applications include desktop docking systems for portables, conventional desktops, information appliances, subnotebook computers and portable peripherals.

The VG660, is an industry standard LCD VGA controller specifically designed to support small flat panels with enhanced features and VGA compatibility at the same time. Using the highly integrated VG660, designers can create an entire VGA LCD subsystem in less than 3 square inches. The device supports a variety of memory display types including DRAMS, PSRAMS, and SRAMS. Built-in power management capabilities support sleep, suspend and standby modes.

HOST SYSTEMS SUPPORTED:

N/A

PROCESSORS SUPPORTED:

Intel386™ CX/EX/SX/SXSA/DX, and Intel486™ SX, IntelDX2™, and IntelDX4 Processors

AVAILABILITY:

Immediately available and in volume production.

CONTACT:

Vadem

1960 Zanker Road

San Jose, CA 95112

Phone: (408) 467-2100

FAX: (408) 467-2199

For international contacts see Appendix B.



V A D E M