I²C-BUS CONTROLLED YUV/RGB SWITCH

GENERAL DESCRIPTION

The TDA8443A is a general purpose two-channel switch for YUV or RGB signals. One channel provides matrixing from RGB to YUV, which can be bypassed.
The IC ic controlled via I²C-bus by seven different addresses or can be used in a non-I²C-bus mode. In the non-I²C-bus mode, control of the circuit is achieved by DC voltages.

Features

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- 3-state switching with an OFF-state
- Selectable gain
- I²C-bus or non-I²C-bus mode
- Address selection for 7 devices
- Fast switching

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 18)		$V_P = V_{18-22}$	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
+/–3 dB	mode 1	B	–	10	–	MHz
Maximum output amplitude of YUV signals (peak-to-peak)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

24-lead DIL; plastic with internal heat spreader (SOT101B).

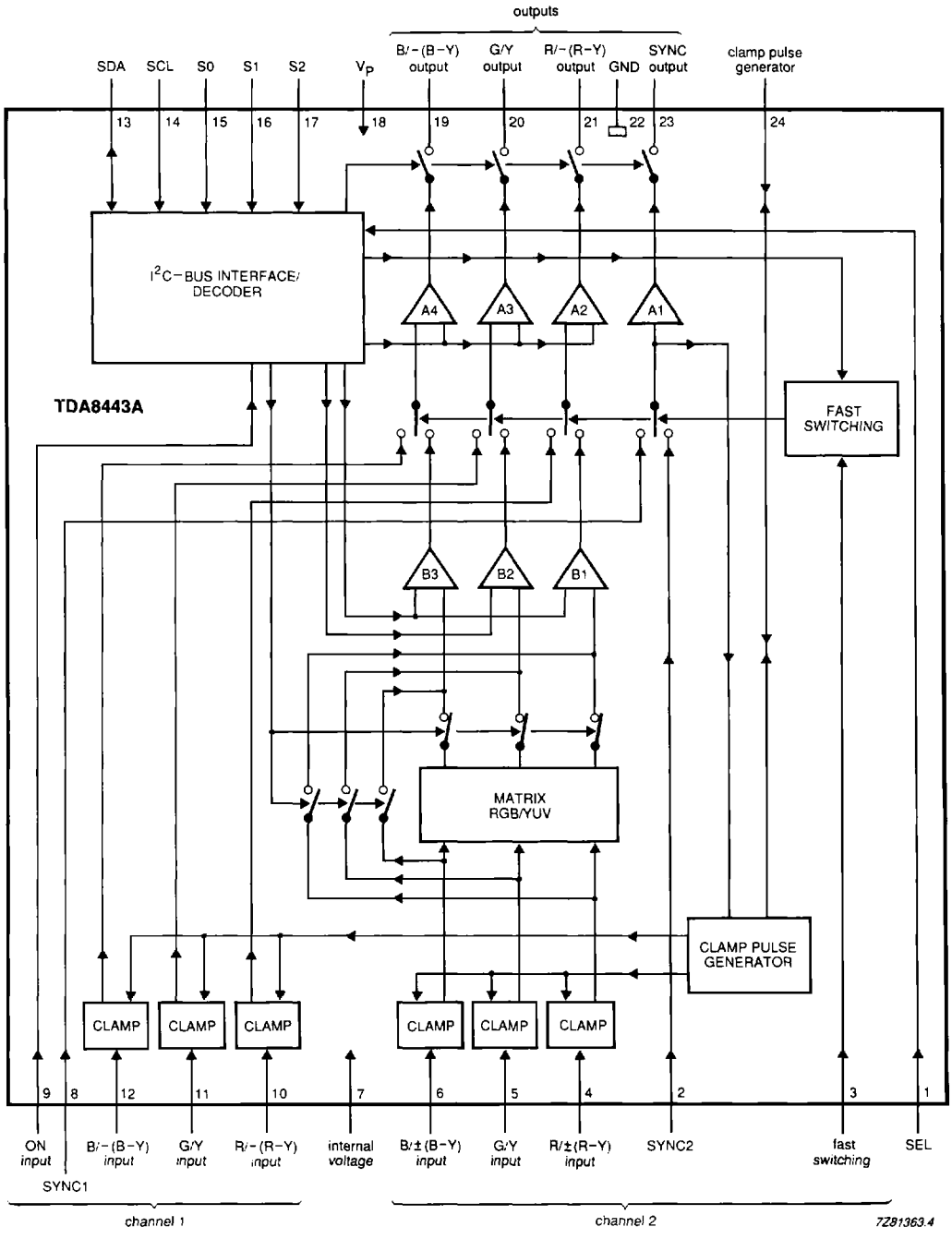

Fig.1 Block diagram.

PINNING

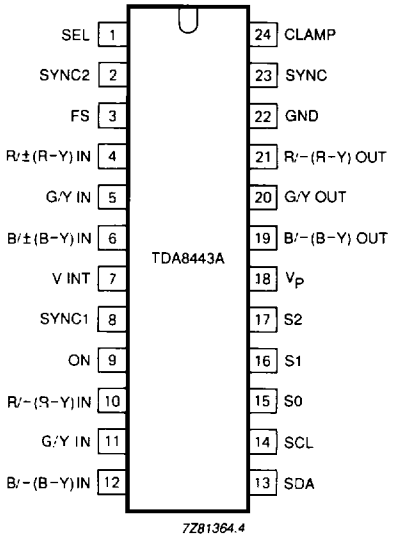

Fig.2 Pinning diagram.

1	SEL	select input (non-I²C-bus mode only)	
2	SYNC2	synchronization input for channel 2	
3	FS	fast switching input	
4	R/± (R-Y) IN	R or (R-Y) signal input	
5	G/Y IN	G or Y signal input	
6	B/± (B-Y) IN	B or (B-Y) signal input	
7	V INT	internal voltage supply	
8	SYNC1	synchronization input for channel 1	
9	ON	ON input	
10	R/−(R-Y) IN	R or −(R-Y) signal input	
11	G/Y IN	G or Y signal input	
12	B/−(B-Y) IN	B or −(B-Y) signal input	
13	SDA	serial data input/output	I²C-bus
14	SCL	serial clock input	I²C-bus
15	S0	address selection inputs	I²C-bus
16	S1	address selection inputs	I²C-bus
17	S2	address selection inputs	I²C-bus
18	V_P	positive supply voltage	
19	B/−(B-Y)	B or −(B-Y) signal output	
20	G/Y OUT	G or Y signal output	
21	R/−(R-Y)	R or −(R-Y) signal output	
22	GND	ground	
23	SYNC	synchronization output	
24	CLAMP	clamping pulse generator input/output	

FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs (see Fig.1). Both channels can receive RGB or YUV signals. Each set of inputs has its own synchronization input, which internally generates a pulse to clamp the inputs. The internal clamping pulse can also be controlled by a signal (e.g. a sandcastle pulse) applied to pin 24. The pulse will occur during the time that the signal at pin 24 is between 5.5 and 6.5 V. If both a sync signal and a pin 24 signal are used the signal should be applied to pin 24 via a 1 kΩ resistor.

RGB signals of channel 2 can be matrixed to YUV signals.

The outputs can be set in a high impedance OFF state, which allows the use of up to seven devices in parallel (I^2C-bus mode).

The circuit can be controlled by an I^2C-bus compatible microcontroller or directly by DC voltages. The fast switching input can be operated via pin 16 of the peritelevision connector.

I²C-bus mode

The protocol for the devices in I²C-bus mode is shown in Fig.3.

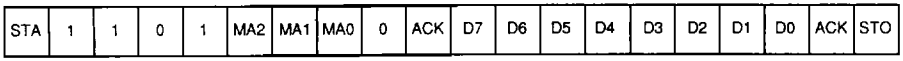

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Fig.3 I²C-bus protocol.

Where:

STA : start condition
MA2, MA1, MA0 : address selection bits, see Table 1
ACK : acknowledge bit
D7 : channel selection bit, see Table 2
D6 : matrix selection bit, see Table 2
D5, D4, D3 : gain control bits, see Table 3
D2 : fast switching priority bit, see Table 4
D1, D0 : output state control bits, see Table 5
STO : stop condition

Table 1 Address selection

address select pins			address select bits		
S2 pin 17	S1 pin 16	S0 pin 15	MA2	MA1	MA0
L	L	L	*	*	*
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	1	1	1

Where:

L = input voltage LOW
H = input voltage HIGH
* = non-I²C-bus operation

Table 2 Mode control bits D7, D6

mode	D7	D6	function
0	0	0	channel 2 selected, no matrix
1	0	1	channel 2 selected, matrix active
2	1	0	channel 1 selected
–	1	1	not allowed

I²C-bus mode (continued)

Table 3 Gain setting (see also Table 9)

D5	D4	D3	A1	A2, A3, A4	B1, B3	B2
0	0	0	1	1	−1	0.45
0	0	1	1	1	1	1
0	1	0	not allowed			
0	1	1	1	1	−1	0.45
1	0	0	2	2	−1	0.45
1	0	1	2	1	1	1
1	1	0	2	2	1	1
1	1	1	2	1	−1	0.45

Matrix equations

The relationship between output and input signals of the matrix is as follows:

$Y = 0.3\ R + 0.59\ G + 0.11\ B$
$R\text{-}Y = 0.7\ R - 0.59\ G - 0.11\ B$
$B\text{-}Y = -0.3\ R - 0.59\ G + 0.89\ B$

Table 4 Priority/fast switching bit D2

D2	fast switching pin 3	mode
0	X	0 to 2, depending on D7, D6
1	0.4 V	2

Where:
X = don't care

Table 5 Output state control bits

D1	D0	pin 9	function
0	X	X	OFF
1	0	L	OFF
1	0	H	ON
1	1	X	ON

Where:
X = don't care

Power-on reset

If the circuit is switched on in the I²C-bus mode, all bits of D0 to D7 are set to zero.

Timing specifications

I²C-bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	max.	unit
Bus free before start	t_{BUF}	4.7	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	μs
SCL and SDA LOW time	t_{LOW}	4.7	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	μs
SCL and SDA rise time	t_r	–	1.0	μs
SCL and SDA fall time	t_f	–	0.3	μs
Data set-up time (write)	$t_{SU;DAT}$	250	–	ns
Data hold time (write)	$t_{HD;DAT}$	1.0	–	μs
Acknowledge set-up time	$t_{SU;ACK}$	–	2	μs
Acknowledge hold time	$t_{HD;ACK}$	0	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	μs

Note

Timing $t_{HD;DAT}$ deviates from the I²C-bus specification. After reset has been activated, a delay of 50 μs must occur before transmission may be resumed.

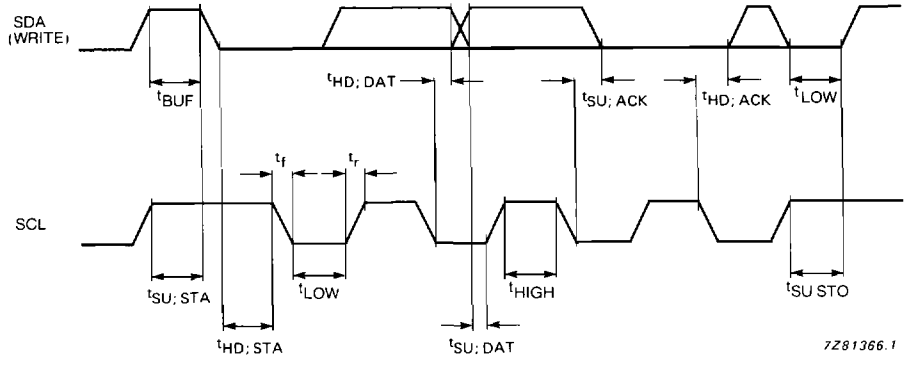


Fig.4 I²C-bus timing diagram.

Non-I²C-bus mode

Table 6 Non-I²C-bus mode (S2 = S1 = S0 = L)

control			mode switched	gain settings			
pin 13	pin 14	pin 1	by FS (pin 3)	A1	A4, A3, A2	B1, B3	B2
L	L	L	2/0	1	1	1	1
L	L	H	2/0	1	2	1	1
L	H	L	2/1	1	1	−1	0.45
L	H	H	2/0	1	1	−1	0.45
H	L	L	2/0	2	1	1	1
H	L	H	2/0	2	2	1	1
H	H	L	2/1	2	1	−1	0.45
H	H	H	2/0	2	1	−1	0.45

Table 7 Fast switching input (pin 3)

FS	*mode selected*
⩽ 0.4 V	mode 2
1 to 3 V	mode 0 or mode 1 as set by control

Table 8 ON input (pin 9)

ON	function
L	OFF, no output signal, high impedance OFF state
H	function is determined in Table 6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 18)	V_P	–	14	V
Input voltage range				
SDA (pin 13)	V_I	−0.3	14	V
SCL (pin 14)	V_I	−0.3	14	V
any other pin	V_I	−0.3	V_P + 0.3	V
Maximum output current	I_O	–	20	mA
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 125	°C
Maximum junction temperature	T_j	–	+ 125	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 18)		V_P	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Absolute gain difference (programmed value)			–	0	10	%
Relative gain difference between Y output and the (R-Y) and (B-Y) channel inputs			–	0	10	%
between any two other channels			–	0	5	%
Input current		I_I	–	0.5	1.0	μA
Output impedance						
pin 19		$\lvert Z_{19\text{-}22}\rvert$	–	7	30	Ω
pin 20		$\lvert Z_{20\text{-}22}\rvert$	–	7	30	Ω
pin 21		$\lvert Z_{21\text{-}22}\rvert$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
±3 dB	mode 1	B	–	10	–	MHz
Mutual time difference at output	all inputs of one source connected together		–	–	25	ns
Maximum output amplitude of YUV signals (peak-to-peak value)	gain x 1	$V_{O(p\text{-}p)}$	2.1	–	–	V
	gain x 2	$V_{O(p\text{-}p)}$	4.2	–	–	V
Crosstalk between	note 1					
inputs of same source	f = 5 MHz	α	–	–	–30	dB
different sources		α	–	–	–40	dB
Isolation (OFF state)	f = 10 MHz		50	–	–	dB

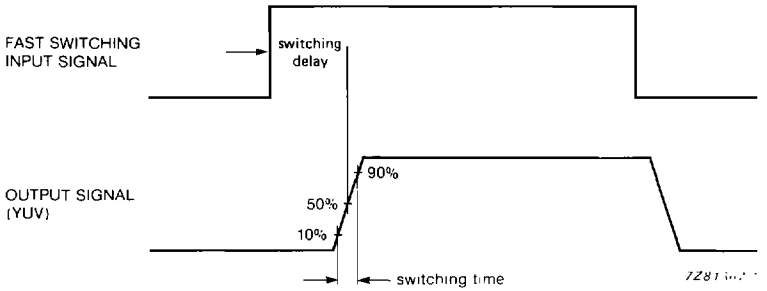
parameter	conditions	symbol	min.	typ.	max.	unit
Differential gain at nominal output signals (peak-to-peak value)	R-Y = 1.05 $V_{(p-p)}$		–	–	10	%
	B-Y = 1.33 $V_{(p-p)}$		–	–	10	%
	Y = 0.34 $V_{(p-p)}$		–	–	10	%
Signal-to-noise ratio nominal input	note 2 B = 5 MHz	S/N	50	–	–	dB
Supply voltage ripple rejection	note 3	RR	30	–	–	dB
DC output levels during clamping		V_O	–	5.3	–	V
Synchronization channels						
Gain difference (programmed value)			–	–	10	%
Bandwidth						
–3 dB		B	–	50	–	MHz
+ 3 dB gain x 1		B	–	20	–	MHz
+ 3 dB gain x 2		B	–	13	–	MHz
Input amplitude of sync signal for correct operation of clamp pulse generator (peak-to-peak value)		$V_{I(p-p)}$	0.2	–	2.5	V
Output impedance (pin 23)		$\lvert Z_{23-22} \rvert$	–	20	30	Ω
Maximum undistorted output amplitude (pin 23) (peak-to-peak value)		$V_{O(p-p)}$	2.5	–	–	V
DC output level on top of sync pulse		V_O	1.5	1.9	2.4	V
I²C-bus inputs						
SDA, SCL						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA
I²C-bus output						
SDA (open collector)						
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.4	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Address selection inputs						
S0, S1, S2						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
Fast switching input						
Input voltage HIGH		V_{IH}	1	–	3	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	500	μA
Input current LOW		I_{IL}	−100	–	–	μA
Switching time	see Fig.5	t	–	10	–	ns
Switching delay	see Fig.5	t_d	–	20	–	ns
Select input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
ON input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA

Notes to the characteristics

1. Crosstalk is defined as the unwanted data transfer from an output, driven at nominal level, to other inputs and outputs on the IC and is expressed as a ratio in dBs.
2. Signal-to-noise ratio = $20 \log \frac{V_{O(p\text{-}p)}}{V_O \text{ noise (RMS) } B = 5 \text{ MHz}}$
3. Supply voltage ripple rejection = $20 \log \frac{V_{RR} \text{ supply}}{V_{RR} \text{ on the output}}$



Input = 0 V (input 1; Mode 2)
Input = 0.75 V (RGB; Mode 1)

Fig.5 Fast switching signal diagram.

APPLICATION INFORMATION

Table 9 Application information

input 1	input 2	output	mode	G2	G1	G0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	1	1
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	1	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	0	0
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	0	0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	0	1
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	0	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	1	0
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	1	0

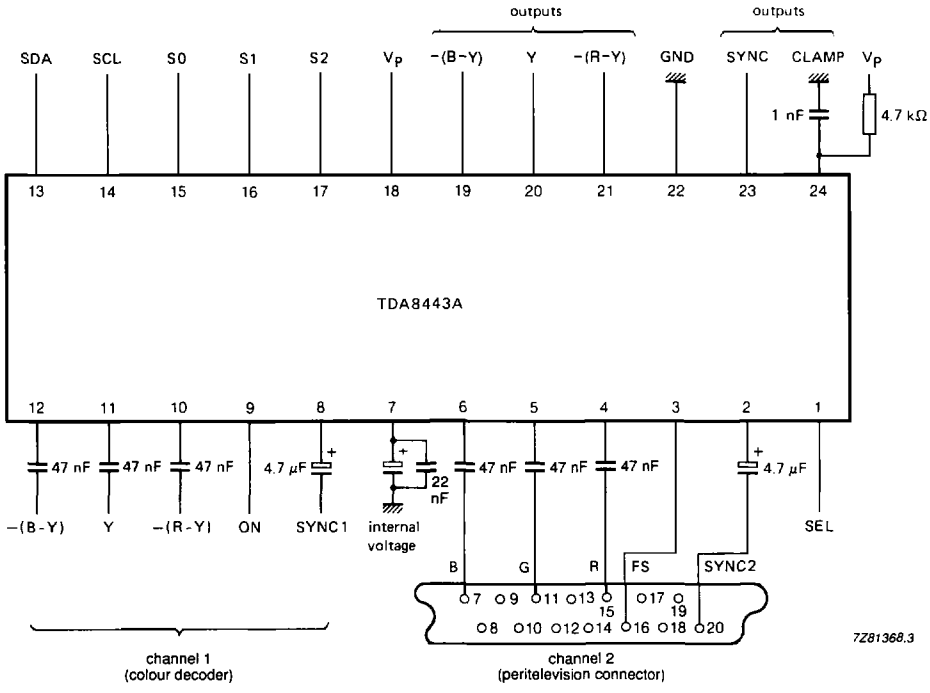


Fig.6 Application diagram (example).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.