PARADIGM®

PDM4M6143
PDM4M6144

256KB and 512KB Second Level Cache Modules for the PowerPC™ CPUs

Features

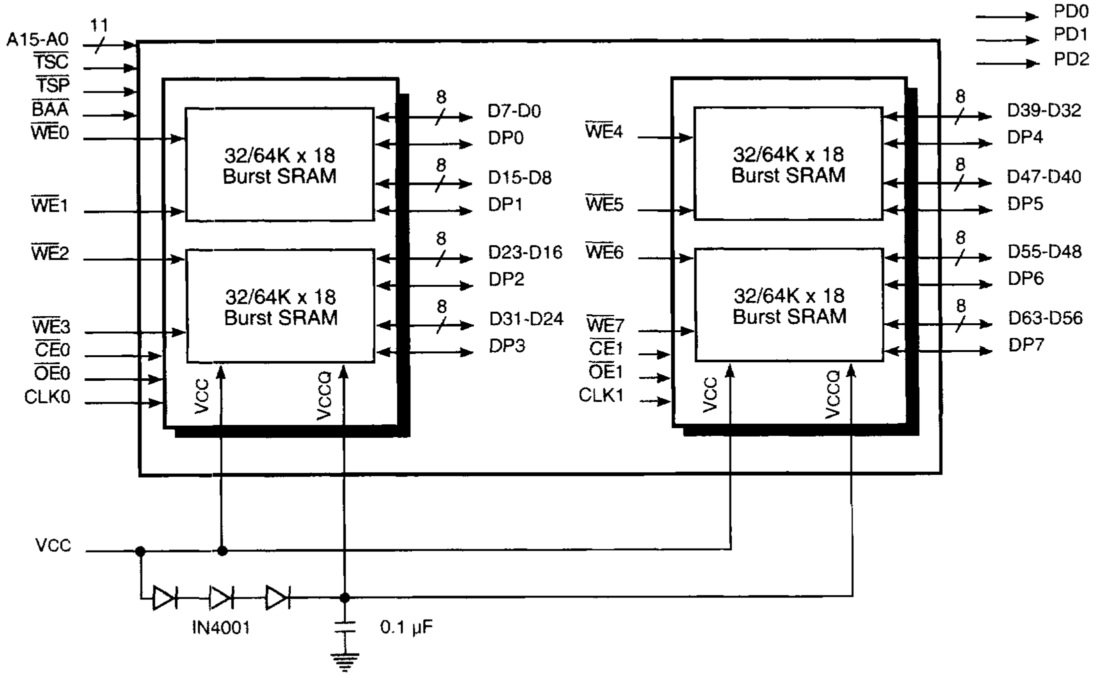
- 256KB and 512KB secondary cache module family
- Ideal for use with PowerPC™ CPU-based Systems using Motorola's Eagle chipset
- 68-position dual read-out DIMM (Dual In-Line Memory Module) with 136 leads
- Operates from a single 5.0V power supply with 3.3V I/O compatibility
- Multiple ground pins and decoupling capacitors for maximum noise immunity

Description

The PDM4M6143 and PDM4M6144 are high-performance CMOS static RAM modules. They are designed for use as second level cache for PowerPC™ CPUs. These modules are designed to be compatible with the Eagle memory controller from Motorola. The PDM4M6143 is organized as 32K x 72 and provides 256KB of cache memory by using 32K x 18 Linear Burst SRAMs. The PDM4M6144 is organized as 64K x 72 and provides 512KB of cache memory by using 64K x 18 Linear Burst SRAMs.

The PDM4M6143 and PDM4M6144 are both available in a 136-pin DIMM package. This low profile package allows for modules with a maximum height of 1.100", a maximum length of 4.050", and a maximum thickness of 0.250". Equal clock-line trace lengths ensure minimum clock skew. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Functional Block Diagram



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Pin Assignment

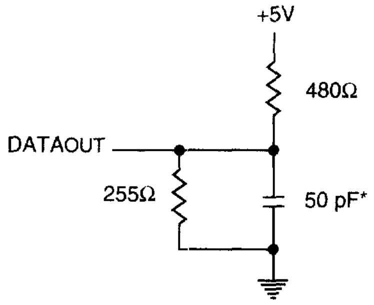
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PD0	35	$\overline{\text{WE6}}$	69	V_{SS}	103	$\overline{\text{WE7}}$
2	PD1	36	D32	70	PD2	104	$\overline{\text{CE1}}$
3	D0	37	D33	71	V_{CC}	105	D34
4	D1	38	V_{SS}	72	D2	106	D35
5	V_{CC}	39	D36	73	D3	107	D37
6	D4	40	D38	74	D5	108	V_{CC}
7	D6	41	D39	75	D7	109	DP4
8	DP0	42	D40	76	V_{SS}	110	D41
9	D8	43	V_{CC}	77	D9	111	D42
10	D10	44	D43	78	D11	112	D44
11	V_{SS}	45	D45	79	D12	113	V_{SS}
12	CLK0	46	D46	80	V_{SS}	114	D47
13	V_{SS}	47	DP5	81	D13	115	D48
14	D14	48	V_{SS}	82	D15	116	D49
15	Vcc	49	CLK1	83	DP1	117	V_{SS}
16	D16	50	V_{SS}	84	V_{SS}	118	D50
17	D17	51	D52	85	D18	119	D51
18	D19	52	D53	86	D20	120	D54
19	D21	53	D55	87	D22	121	D56
20	V_{CC}	54	DP6	88	D23	122	V_{SS}
21	DP2	55	V_{CC}	89	V_{SS}	123	D57
22	D24	56	D58	90	D25	124	D59
23	D26	57	D60	91	D27	125	D61
24	D28	58	D62	92	D29	126	D63
25	V_{SS}	59	DP7	93	D30	127	V_{CC}
26	D31	60	A0	94	V_{SS}	128	A1
27	DP3	61	A2	95	$\overline{\text{CE0}}$	129	A3
28	V_{SS}	62	A4	96	$\overline{\text{WE1}}$	130	A5
29	$\overline{\text{WE0}}$	63	A6	97	$\overline{\text{WE3}}$	131	A7
30	$\overline{\text{WE2}}$	64	A8	98	$\overline{\text{OE0}}$	132	NC
31	$\overline{\text{TSP}}$	65	A10	99	$\overline{\text{TSC}}$	133	A9
32	$\overline{\text{BAA}}$	66	A12	100	V_{SS}	134	A11
33	V_{CC}	67	A14	101	$\overline{\text{OE1}}$	135	A13
34	$\overline{\text{WE4}}$	68	V_{SS}	102	$\overline{\text{WE5}}$	136	A15

Pin Names

Pin	Signal
A15-A0	Address Inputs
D63-D0	Inputs/Outputs
DP0-DP7	Parity Inputs/Outputs
$\overline{CE1}$-$\overline{CE0}$	Module Enable
$\overline{WE7}$-$\overline{WE0}$	Byte Write Enable Inputs
$\overline{OE1}$-$\overline{OE0}$	Module Output Enable
$\overline{TSC}$	Controller Address Status
$\overline{TSP}$	Processor Address Status
$\overline{BAA}$	Burst Counter Advance
CLK1-CLK0	Clock Inputs
PD2-PD0	Presence Detect Pins
NC	No Connect
V_{SS}	Ground
V_{CC}	Power Supply

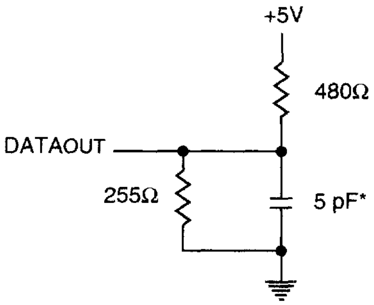
AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



* Including scope and jig

Figure 1. Output Load



* Including scope and jig

Figure 2. Output Load
(for tOHZ, tCHZ, tOLZ, and tCLZ)

Presence Detection Code

Part No.	Description	PD2	PD1	PD0
	No Cache Present	NC	NC	NC
	Reserved	NC	NC	V_{SS}
PDM4M6142	256KB Asynchronous	V_{SS}	V_{SS}	V_{SS}
PDM4M6143	256KB Linear Burst	NC	V_{SS}	NC
PDM4M6144	512KB Linear Burst	V_{SS}	NC	NC

Absolute Maximum Ratings(1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +85	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	–55 to +125	°C
P_T	Power Dissapation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{SS}	Supply Voltage	0	0	0.0	V
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Address, Control)	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	20	µA
I_{LI}	Input Leakage Current ($\overline{CE}$, $\overline{OE}$, CLK)	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	10	µA
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	5	µA
I_{LO}	Ouput Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4 mA, V_{CC} = Min.	2.4	—	V
V_{IH}	Input High Voltage		2.2	6.0	V
V_{IL}	Input Low Voltage		–0.5(1)	0.8	V

NOTE: 1 V_{IL} (Min.) = –3.0V for pulse widths less than 20 ns.

Power Supply Characteristics (V_{CC} = 5.0V ± 5%)

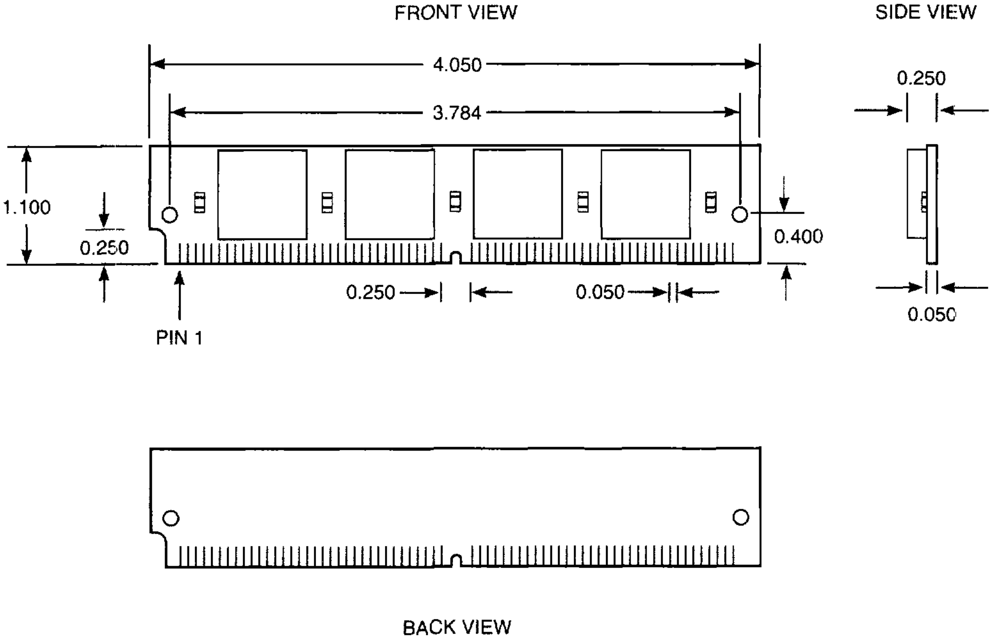
Symbol	Parameter	Max.	Unit
I_{CC}	Operating Current $\overline{CE} \leq V_{IL}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	1000	mA
I_{SB}	Standby Current $\overline{CE} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	200	mA
I_{SB1}	Full Standby Current $\overline{CE} \geq V_{CC} - 0.2V$, V_{CC} = Max., f = 0, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ Outputs Open	120	mA

Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max	Unit
C_{IN1}	Input Capacitance (Address, Control), V_{IN} = 0V	25	pF
C_{IN2}	Input Capacitance ($\overline{CE}$, $\overline{OE}$, CLK), V_{IN} = 0V	15	pF
C_{IN3}	Input Capacitance ($\overline{WE}$), V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance, V_{OUT} = 0V	10	pF

NOTE: 1. This parameter is determined by device characteristics but is not production tested.

Physical Dimension



Ordering Information

PDM4M XXXXX X XX X X

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
Package	M	68 position dual read-out SIMM (Single In-line Memory Module)
Speed	8 9 10	Speed in SRAMs used (nanoseconds)
Power	S	Standard Power
Device Type	6143 6144	256KB Linear Burst Cache Module 512KB Linear Burst Cache Module