

MOS INTEGRATED CIRCUIT

μ PD42S4210AL, 424210AL

3.3 V OPERATION 4 M-BIT DYNAMIC RAM

256 K-WORD BY 16-BIT, HYPER PAGE MODE, BYTE READ/WRITE MODE

Description

The μ PD42S4210AL, 424210AL are 262,144 words by 16 bits CMOS dynamic RAMs with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

Besides, the μ PD42S4210AL can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

The μ PD42S4210AL, 424210AL are packaged in 44-pin plastic TSOP (II) and 40-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 262,144 words by 16 bits organization
- Single +3.3 V \pm 0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD42S4210AL-A60, 424210AL-A60	288 mW	60 ns	104 ns	25 ns
μ PD42S4210AL-A70, 424210AL-A70	252 mW	70 ns	124 ns	30 ns
μ PD42S4210AL-A80, 424210AL-A80	216 mW	80 ns	144 ns	35 ns

- The μ PD42S4210AL can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

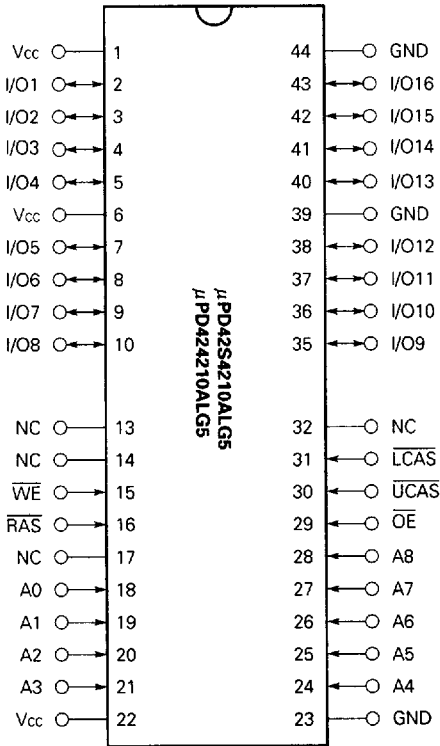
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S4210AL	512 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.288 mW (CMOS level input)
μ PD424210AL	512 cycles / 8 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

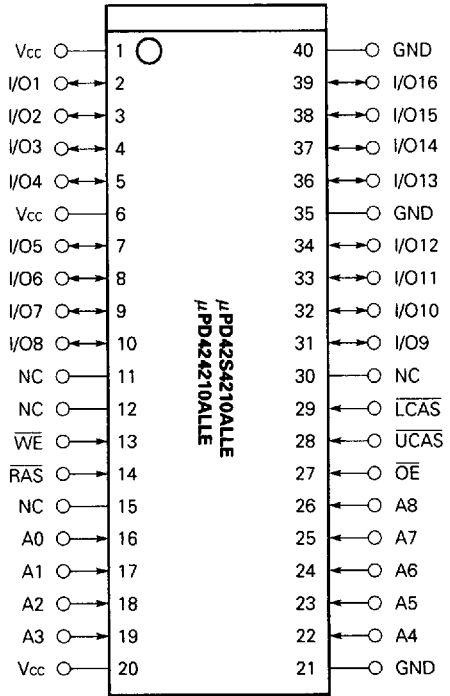
Part number	Access time (MAX.)	Package	Refresh
μPD42S4210ALG5-A60	60 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S4210ALG5-A70	70 ns		
μPD42S4210ALG5-A80	80 ns		
μPD42S4210ALLE-A60	60 ns	40-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S4210ALLE-A70	70 ns		
μPD42S4210ALLE-A80	80 ns		
μPD424210ALG5-A60	60 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD424210ALG5-A70	70 ns		
μPD424210ALG5-A80	80 ns		
μPD424210ALLE-A60	60 ns	40-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD424210ALLE-A70	70 ns		
μPD424210ALLE-A80	80 ns		

Pin Configurations (Marking Side)

44-pin Plastic TSOP (II) (400 mil)



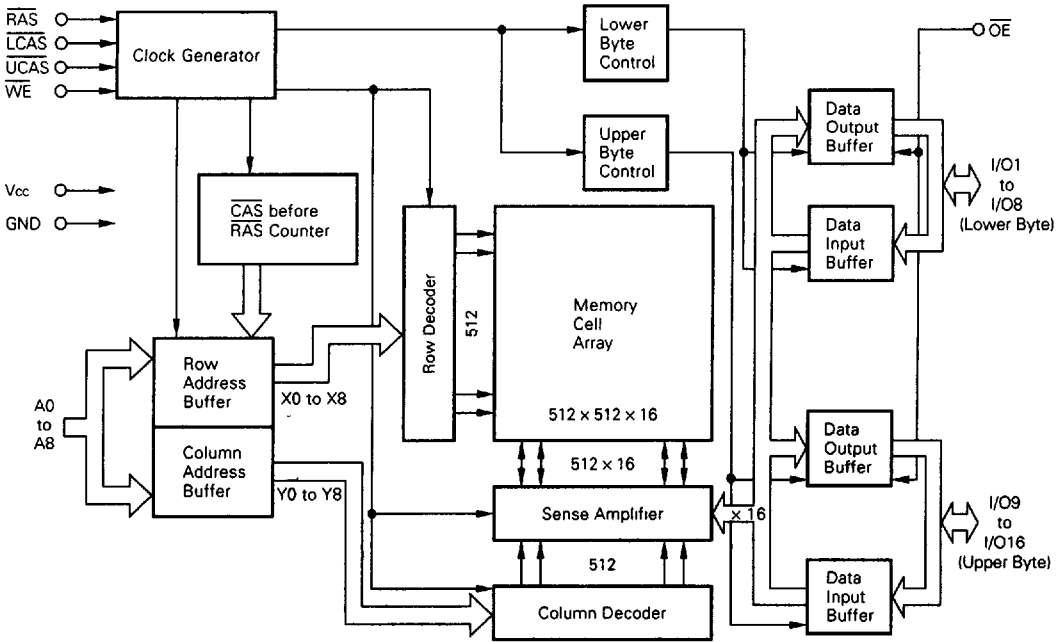
40-pin Plastic SOJ (400 mil)



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{UCAS}}$: Column Address Strobe (upper)
- $\overline{\text{LCAS}}$: Column Address Strobe (lower)
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

6427525 0061106 T23

Block Diagram



■ 6427525 0061107 96T ■

Input/Output Pin Functions

The μPD42S4210AL, 424210AL have input pins \overline{RAS} , \overline{CAS} ^{Note}, \overline{WE} , \overline{OE} , A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
\overline{RAS} (Row address strobe)	Input	\overline{RAS} activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • \overline{CAS} before \overline{RAS} refresh
\overline{CAS} (Column address strobe)	Input	\overline{CAS} activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	Address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 262,144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating \overline{RAS} . Then, switch the address bus to column address and activate \overline{CAS} . Each address is taken into the device when \overline{RAS} and \overline{CAS} are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of \overline{RAS} and \overline{CAS} .
\overline{WE} (Write enable)	Input	Write control signal. Write operation is executed by activating \overline{RAS} , \overline{CAS} and \overline{WE} .
\overline{OE} (Output enable)	Input	Read control signal. Read operation can be executed by activating \overline{RAS} , \overline{CAS} and \overline{OE} . If \overline{WE} is activated during read operation, \overline{OE} is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note \overline{CAS} means \overline{UCAS} and \overline{LCAS} .

Cautions when using the hyper page mode

1. $\overline{\text{CAS}}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of read cycle)
 $\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active
 t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.
 t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{OEZ} is effective.
 - (3) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{\text{CAS}}$ signal when controlling data output with the $\overline{\text{OE}}$ signal.
 - (1) $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 - (2) $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V _T		-0.5 to +4.6	V
Supply voltage	V _{CC}		-0.5 to +4.6	V
Output current	I _O		20	mA
Power dissipation	P _D		1	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{STG}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		V _{CC} + 0.3	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	Address			5	pF
	C _{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data input/output capacitance	C _{I/O}	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

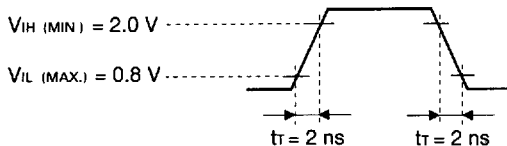
Parameter		Symbol	Test Condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	80	mA	1, 2, 3
				$t_{RAC} = 70 \text{ ns}$	70		
				$t_{RAC} = 80 \text{ ns}$	60		
Standby current	μPD42S4210AL	I _{CC2}	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN)}$, $I_O = 0 \text{ mA}$ $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$, $I_O = 0 \text{ mA}$		0.5	mA	
					0.08		
	μPD424210AL				2.0		
				0.5			
\overline{RAS} only refresh current		I _{CC3}	\overline{RAS} Cycling, $\overline{CAS} \geq V_{IH(MIN)}$ $t_{RC} = t_{RC(MIN)}$, $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	80	mA	1, 2, 3, 4
				$t_{RAC} = 70 \text{ ns}$	70		
				$t_{RAC} = 80 \text{ ns}$	60		
Operating current (Hyper page mode)		I _{CC4}	$\overline{RAS} \leq V_{IL(MAX)}$, \overline{CAS} Cycling $t_{HPC} = t_{HPC(MIN)}$, $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	80	mA	1, 2, 5
				$t_{RAC} = 70 \text{ ns}$	70		
				$t_{RAC} = 80 \text{ ns}$	60		
\overline{CAS} before \overline{RAS} refresh current		I _{CC5}	\overline{RAS} Cycling $t_{RC} = t_{RC(MIN)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	80	mA	1, 2
				$t_{RAC} = 70 \text{ ns}$	70		
				$t_{RAC} = 80 \text{ ns}$	60		
\overline{CAS} before \overline{RAS} long refresh current (512 cycles / 128 ms, only for the μPD42S4210AL)		I _{CC6}	\overline{CAS} before \overline{RAS} refresh : $t_{RC} = 250.0 \mu\text{s}$ $\overline{RAS}, \overline{CAS}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ Standby : $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{WE}, \overline{OE} : V_{IH}$ $I_O = 0 \text{ mA}$	$t_{RAS} \leq 200 \text{ ns}$	80	μA	1, 2
				$t_{RAS} \leq 1 \mu\text{s}$	100	μA	1, 2
\overline{CAS} before \overline{RAS} self refresh current (only for the μPD42S4210AL)		I _{CC7}	$\overline{RAS}, \overline{CAS}$: $t_{RASS} = 5 \text{ ms}$ $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $I_O = 0 \text{ mA}$		80	μA	2
Input leakage current		I _{I(L)}	$V_I = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5	+5	μA	
Output leakage current		I _{O(L)}	$V_O = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage		V _{OH}	$I_O = -2.0 \text{ mA}$	2.4		V	
Low level output voltage		V _{OL}	$I_O = +2.0 \text{ mA}$		0.4	V	

- Notes**
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
 - Specified values are obtained with outputs unloaded.
 - I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX)}$ and $\overline{CAS} \geq V_{IH(MIN)}$.
 - I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 - I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

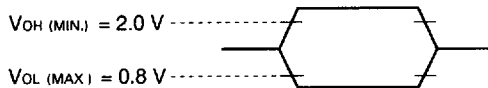
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{rac} = 60 ns		t _{rac} = 70 ns		t _{rac} = 80 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write Cycle Time	t _{rc}	104	-	124	-	144	-	ns		
RAS Precharge Time	t _{rp}	40	-	50	-	60	-	ns		
CAS Precharge Time	t _{cpn}	10	-	10	-	10	-	ns		
RAS Pulse Width	t _{ras}	60	10,000	70	10,000	80	10,000	ns		
CAS Pulse Width	t _{cas}	10	10,000	12	10,000	15	10,000	ns		
RAS Hold Time	t _{rsh}	10	-	12	-	15	-	ns		
CAS Hold Time	t _{ctsh}	40	-	50	-	60	-	ns		
RAS to CAS Delay Time	t _{rcd}	14	45	14	52	14	60	ns	1	
RAS to Column Address Delay Time	t _{rad}	12	30	12	35	12	40	ns	1	
CAS to RAS Precharge Time	t _{crp}	5	-	5	-	5	-	ns	2	
Row Address Setup Time	t _{asr}	0	-	0	-	0	-	ns		
Row Address Hold Time	t _{rah}	10	-	10	-	12	-	ns		
Column Address Setup Time	t _{asc}	0	-	0	-	0	-	ns		
Column Address Hold Time	t _{cah}	10	-	12	-	15	-	ns		
OE Lead Time Referenced to RAS	t _{oes}	0	-	0	-	0	-	ns		
CAS to Data Setup Time	t _{clz}	0	-	0	-	0	-	ns		
OE to Data Setup Time	t _{olz}	0	-	0	-	0	-	ns		
OE to Data Delay Time	t _{oed}	13	-	15	-	15	-	ns		
Masked Byte Write Hold Time Referenced to RAS	t _{mwh}	0	-	0	-	0	-	ns		
Transition Time (Rise and Fall)	t _r	1	50	1	50	1	50	ns		
Refresh Time	μPD42S4210AL	t _{ref}	-	128	-	128	-	128	ms	3
	μPD424210AL		-	8	-	8	-	8	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD (MAX)}$ and $t_{RCD} \leq t_{RCD (MAX)}$	$t_{RAC (MAX)}$	$t_{RAC (MAX)}$
$t_{RAD} > t_{RAD (MAX)}$ and $t_{RCD} \leq t_{RCD (MAX)}$	$t_{AA (MAX)}$	$t_{RAD} + t_{AA (MAX)}$
$t_{RCD} > t_{RCD (MAX)}$	$t_{CAC (MAX)}$	$t_{RCD} + t_{CAC (MAX)}$

$t_{RAD (MAX)}$ and $t_{RCD (MAX)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD (MAX)}$ and $t_{RCD} \geq t_{RCD (MAX)}$ will not cause any operation problems.

- $t_{CRP (MIN)}$ requirement is applied to \overline{RAS} , \overline{CAS} cycles preceded by any cycle.
- This specification is applied only to the μPD42S4210AL.

Read Cycle

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from \overline{RAS}	t_{RAC}	-	60	-	70	-	80	ns	1
Access Time from \overline{CAS}	t_{CAC}	-	15	-	18	-	20	ns	1
Access Time from Column Address	t_{AA}	-	30	-	35	-	40	ns	1
Access Time from \overline{OE}	t_{OEA}	-	15	-	18	-	20	ns	
Column Address Lead Time Referenced to \overline{RAS}	t_{RAL}	30	-	35	-	40	-	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to \overline{RAS}	t_{RRH}	0	-	0	-	0	-	ns	2
Read Command Hold Time Referenced to \overline{CAS}	t_{RCH}	0	-	0	-	0	-	ns	2
Output Buffer Turn-off Delay Time from \overline{OE}	t_{OEZ}	0	13	0	15	0	15	ns	3
\overline{CAS} Hold Time to \overline{OE}	t_{CHO}	5	-	5	-	5	-	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD (MAX)}$ and $t_{RCD} \leq t_{RCD (MAX)}$	$t_{RAC (MAX)}$	$t_{RAC (MAX)}$
$t_{RAD} > t_{RAD (MAX)}$ and $t_{RCD} \leq t_{RCD (MAX)}$	$t_{AA (MAX)}$	$t_{RAD} + t_{AA (MAX)}$
$t_{RCD} > t_{RCD (MAX)}$	$t_{CAC (MAX)}$	$t_{RCD} + t_{CAC (MAX)}$

$t_{RAD (MAX)}$ and $t_{RCD (MAX)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD (MAX)}$ and $t_{RCD} \geq t_{RCD (MAX)}$ will not cause any operation problems.

- Either $t_{RCH (MIN)}$ or $t_{RRH (MIN)}$ should be met in read cycles.
- $t_{OEZ (MAX)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
\overline{WE} Hold Time Referenced to \overline{CAS}	twch	10	-	10	-	15	-	ns	1
\overline{WE} Pulse Width	twp	10	-	10	-	15	-	ns	1
\overline{WE} Lead Time Referenced to \overline{RAS}	trwl	10	-	12	-	15	-	ns	
\overline{WE} Lead Time Referenced to \overline{CAS}	tcwl	10	-	12	-	15	-	ns	
\overline{WE} Setup Time	twcs	0	-	0	-	0	-	ns	2
\overline{OE} Hold Time	toeh	0	-	0	-	0	-	ns	
Data-in Setup Time	t _{DS}	0	-	0	-	0	-	ns	3
Data-in Hold Time	t _{DH}	10	-	10	-	12	-	ns	3

- Notes**
1. t_{WP(MIN)} is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH(MIN)} should be met.
 2. If t_{WCS} ≥ t_{WCS(MIN)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS(MIN)} and t_{DH(MIN)} are referenced to the \overline{CAS} falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the \overline{WE} falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	133	-	157	-	179	-	ns	
\overline{RAS} to \overline{WE} Delay Time	trwd	77	-	89	-	100	-	ns	1
\overline{CAS} to \overline{WE} Delay Time	tcwd	32	-	37	-	42	-	ns	1
Column Address to \overline{WE} Delay Time	tawd	47	-	54	-	60	-	ns	1

- Note 1.** If t_{WCS} ≥ t_{WCS(MIN)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{TRWD} ≥ t_{TRWD(MIN)}, t_{TCWD} ≥ t_{TCWD(MIN)}, t_{AWD} ≥ t_{AWD(MIN)} and t_{CPWD} ≥ t_{CPWD(MIN)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t _{TRAC} = 60 ns		t _{TRAC} = 70 ns		t _{TRAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	25	-	30	-	35	-	ns	1
RAS Pulse Width	t _{RASP}	60	125,000	70	125,000	80	125,000	ns	
CAS Pulse Width	t _{HCAS}	10	10,000	12	10,000	15	10,000	ns	
CAS Precharge Time	t _{CP}	10	-	10	-	10	-	ns	
Access Time from CAS Precharge	t _{ACP}	-	35	-	40	-	45	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	52	-	59	-	65	-	ns	2
RAS Hold Time from CAS Precharge	t _{RHCP}	35	-	40	-	45	-	ns	
Read Modify Write Cycle Time	t _{HPRWC}	66	-	75	-	84	-	ns	
Data Output Hold Time	t _{DHC}	5	-	5	-	5	-	ns	
OE to CAS Hold Time	t _{OCH}	5	-	5	-	5	-	ns	4
OE Precharge Time	t _{OEP}	5	-	5	-	5	-	ns	
Output Buffer Turn-off Delay from WE	t _{WEZ}	0	13	0	15	0	15	ns	3,4
WE Pulse Width	t _{WPZ}	10	-	10	-	13	-	ns	4
Output Buffer Turn-off delay from RAS	t _{OFR}	0	13	0	15	0	15	ns	3,4
Output Buffer Turn-off delay from CAS	t _{OFC}	0	13	0	15	0	15	ns	3,4

Notes 1. t_{HPC} (MIN.) is applied to CAS access.

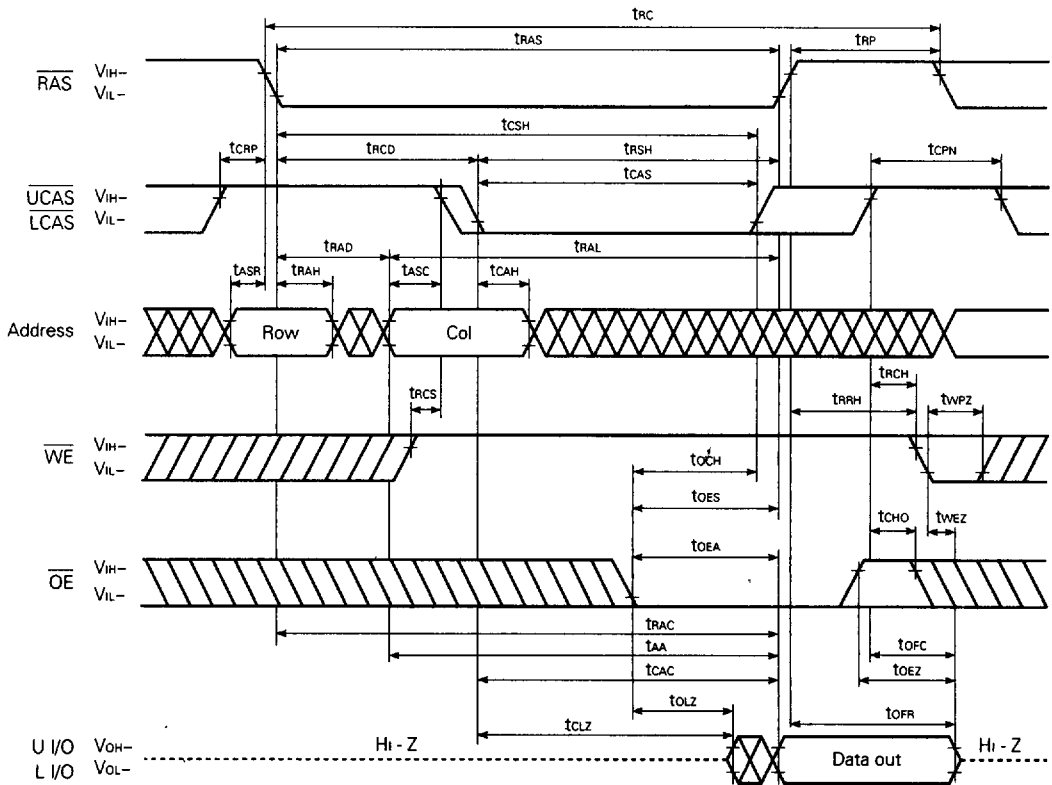
2. If t_{WCs} ≥ t_{WCs} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{TRWD} ≥ t_{TRWD} (MIN.), t_{TCWD} ≥ t_{TCWD} (MIN.), t_{TAWD} ≥ t_{TAWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
3. t_{OFC} (MAX.), t_{OFR} (MAX.) and t_{WEZ} (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.
4. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) Both RAS and CAS are inactive (at the end of the read cycle)
 WE: inactive, OE: active
 t_{OFC} is effective when RAS is inactivated before CAS is inactivated.
 t_{OFR} is effective when CAS is inactivated before RAS is inactivated.
 - (2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)
 WE, OE: inactive t_{OEZ} is effective.
 - (3) Both RAS and CAS are inactive or RAS is active and CAS is inactive (at the end of read cycle)
 WE, OE: active and either t_{TRRH} or t_{TRCH} must be met t_{WEZ} and t_{WPZ} are effective.
 - (4) WE: inactive (in read cycle)
 CAS: inactive, OE: active t_{CHO} is effective.
 CAS, OE: active t_{OCH} is effective.

Refresh Cycle

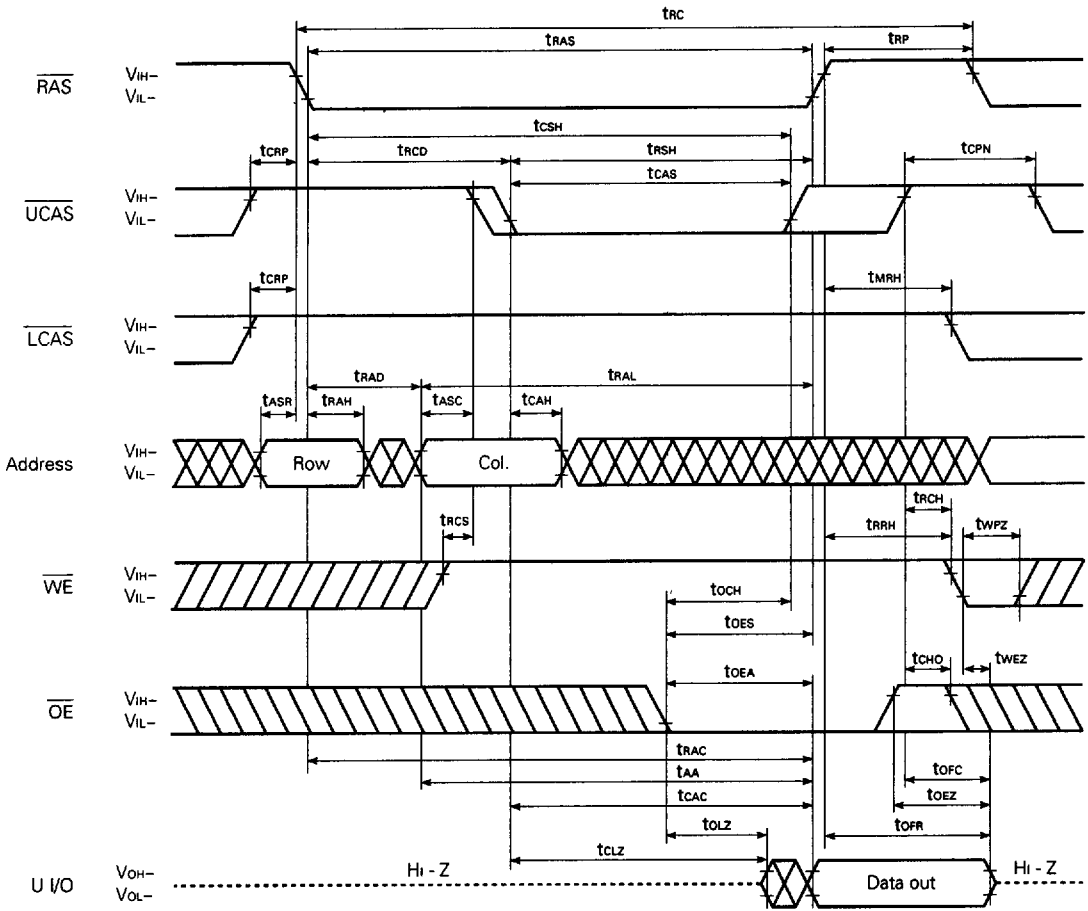
Parameter	Symbol	trac = 60 ns		trac = 70 ns		trac = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	tCSR	5	-	5	-	5	-	ns	
CAS Hold Time (CAS before RAS Refresh)	tCHR	10	-	10	-	10	-	ns	
RAS Precharge CAS Hold Time	trPC	5	-	5	-	5	-	ns	
RAS Pulse Width (CAS before RAS Self Refresh)	trASS	100	-	100	-	100	-	μs	1
RAS Precharge Time (CAS before RAS Self Refresh)	trPS	110	-	130	-	150	-	ns	1
CAS Hold Time (CAS before RAS Self Refresh)	tCHS	-50	-	-50	-	-50	-	ns	1
WE Hold Time	tWHR	15	-	15	-	15	-	ns	

Note 1. This specification is applied only to the μPD42S4210AL.

Read Cycle

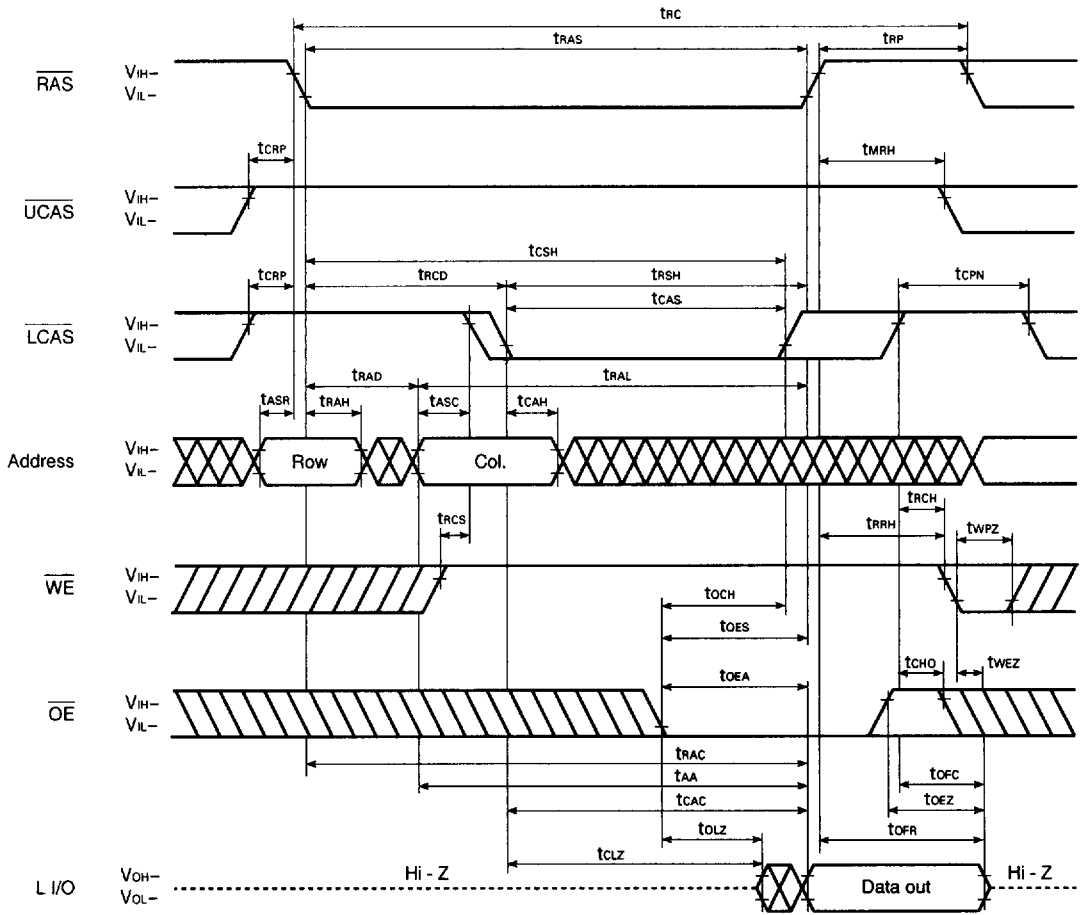


Upper Byte Read Cycle



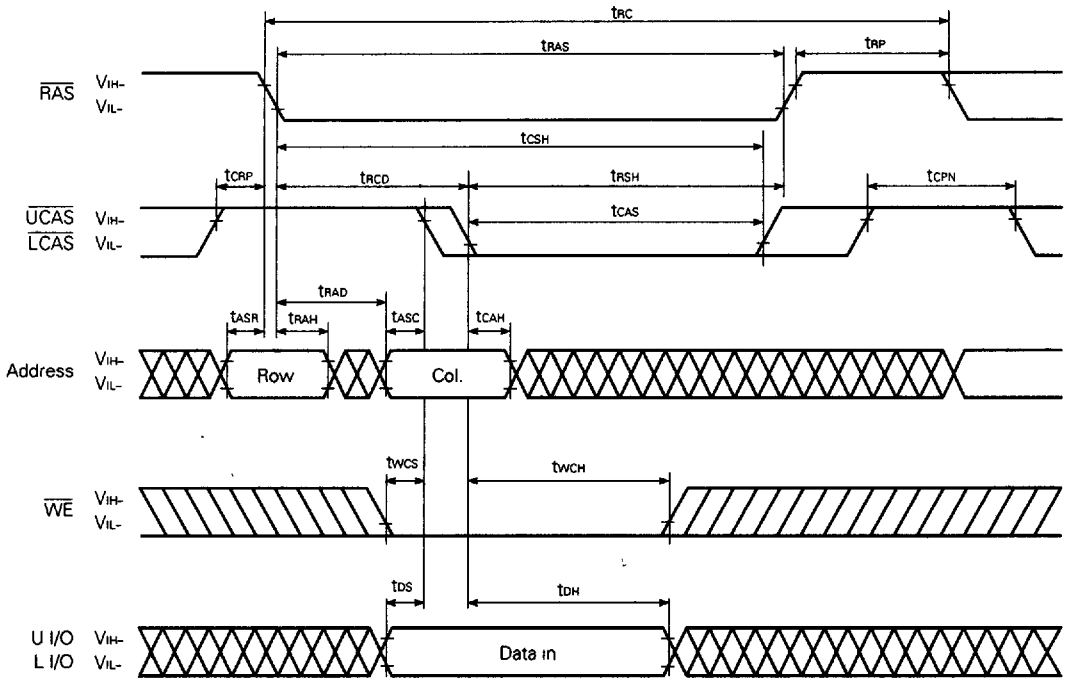
Remark L I/O: Hi-Z

Lower Byte Read Cycle



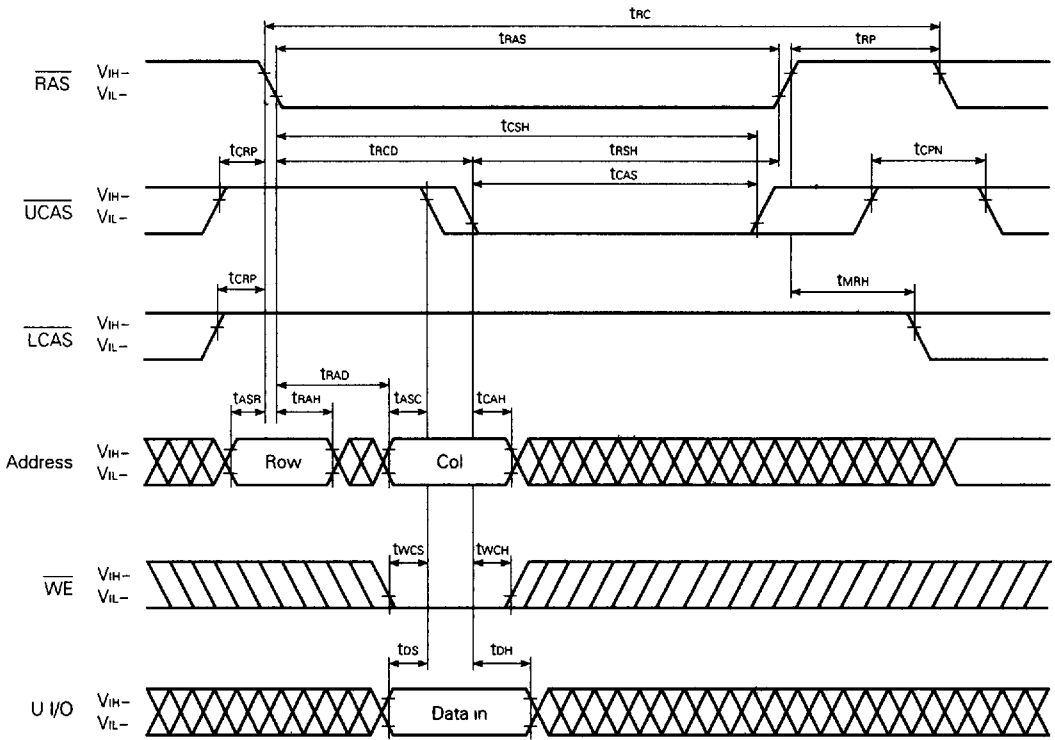
Remark U I/O: Hi-Z

Early Write Cycle



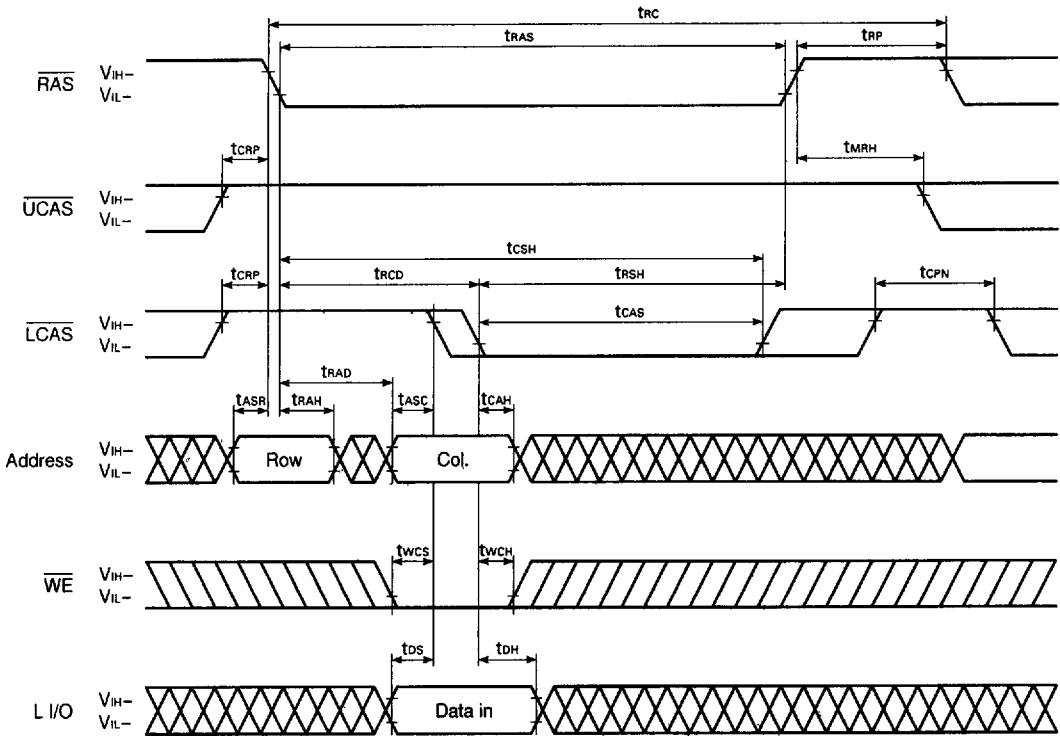
Remark \overline{OE} : Don't care

Upper Byte Early Write Cycle



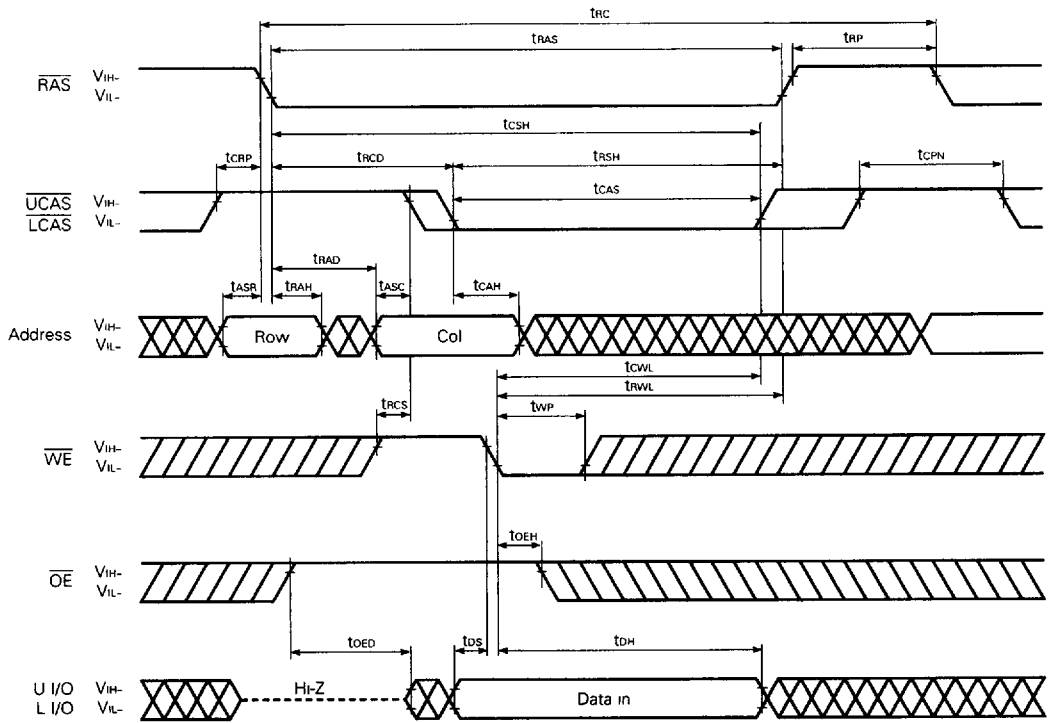
Remark \overline{OE} , L I/O: Don't care

Lower Byte Early Write Cycle

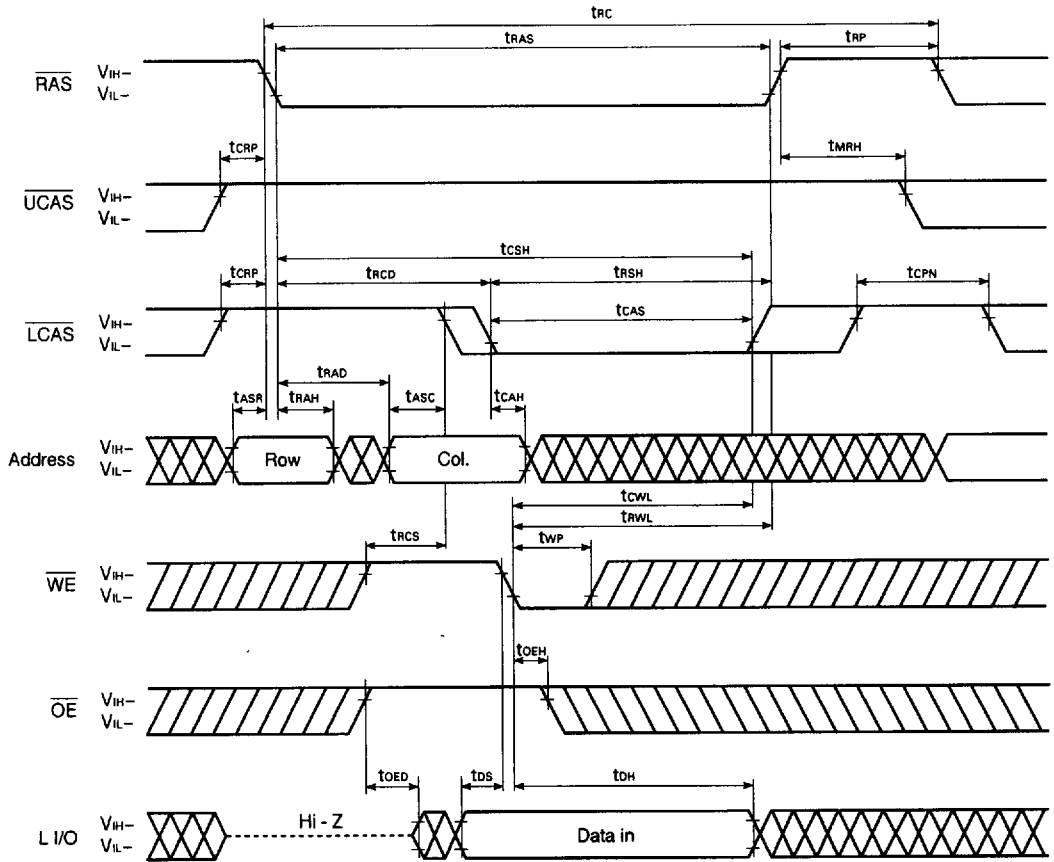


Remark \overline{OE} , U I/O: Don't care

Late Write Cycle

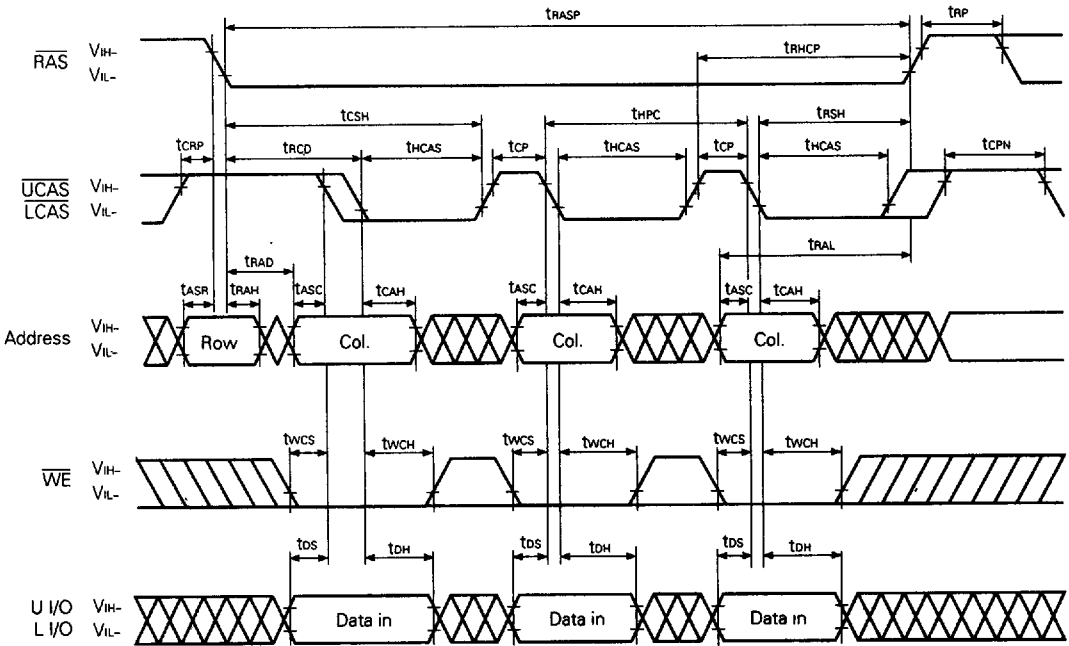


Lower Byte Late Write Cycle



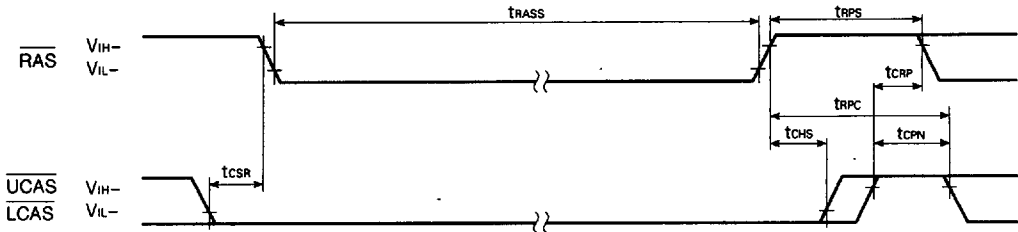
Remark U I/O: Don't care

Hyper Page Mode Early Write Cycle



- Remarks**
1. \overline{OE} : Don't care
 2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive \overline{CAS} cycles within the same \overline{RAS} cycle.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S4210AL)



Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

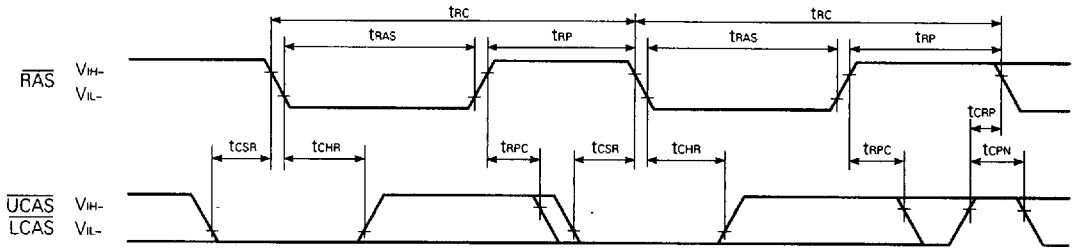
Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

- (1) **Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh**
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 512 times within an 8 ms interval just before and after setting CAS before RAS self refresh.
- (2) **Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh**
When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 512 times within an 8 ms interval just before and after setting CAS before RAS self refresh.

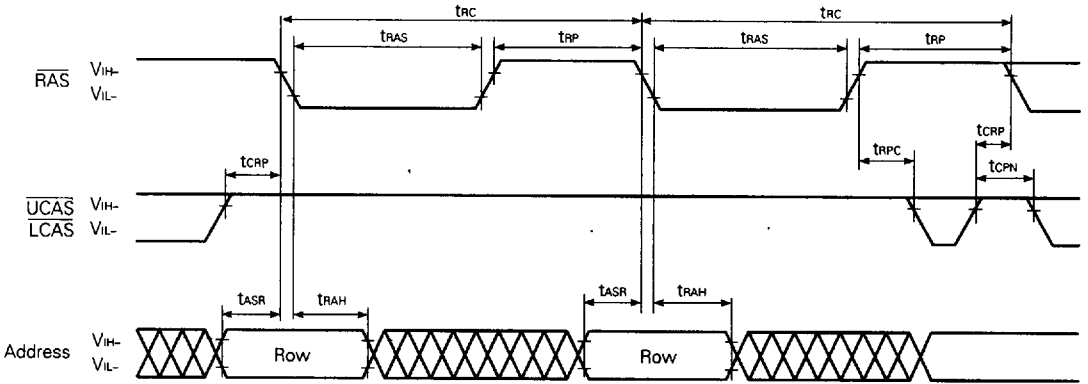
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



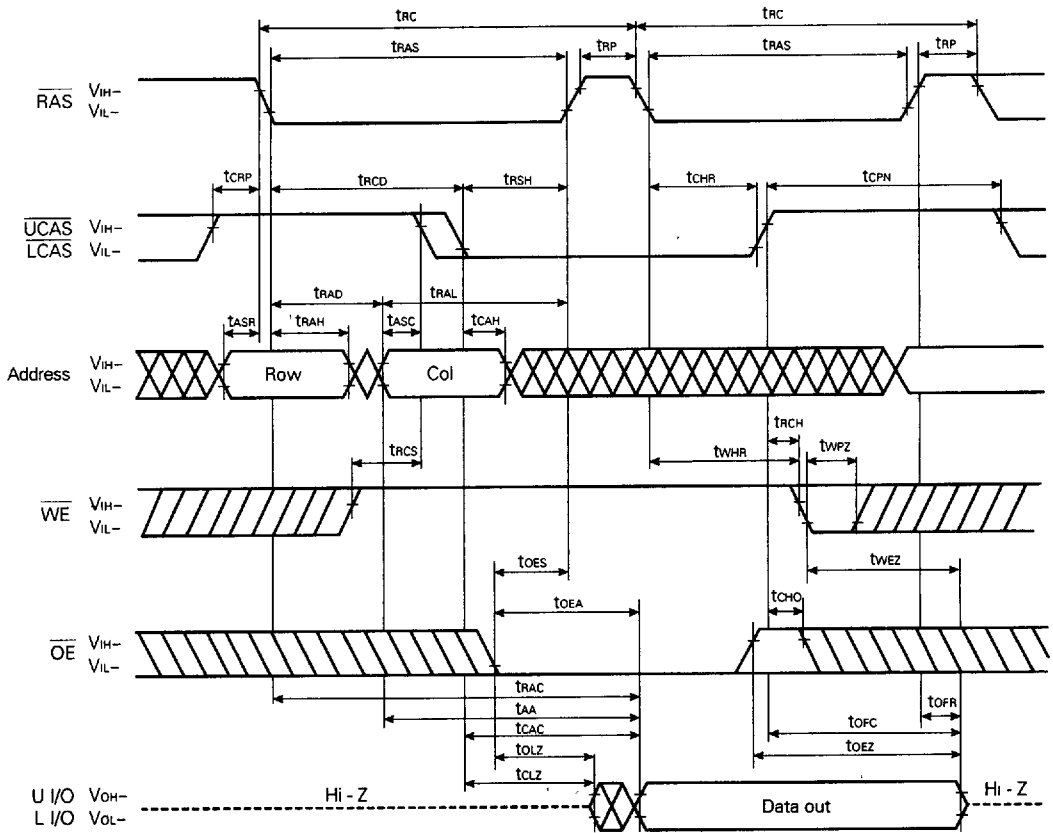
Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle



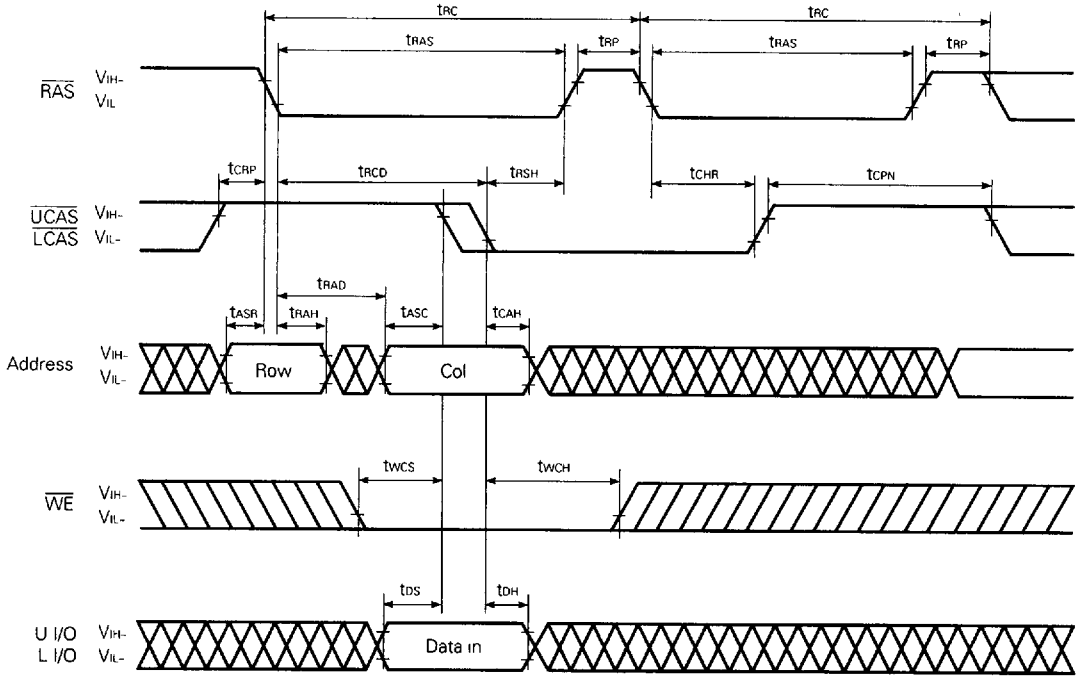
Remark \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



6427525 0061143 9T0

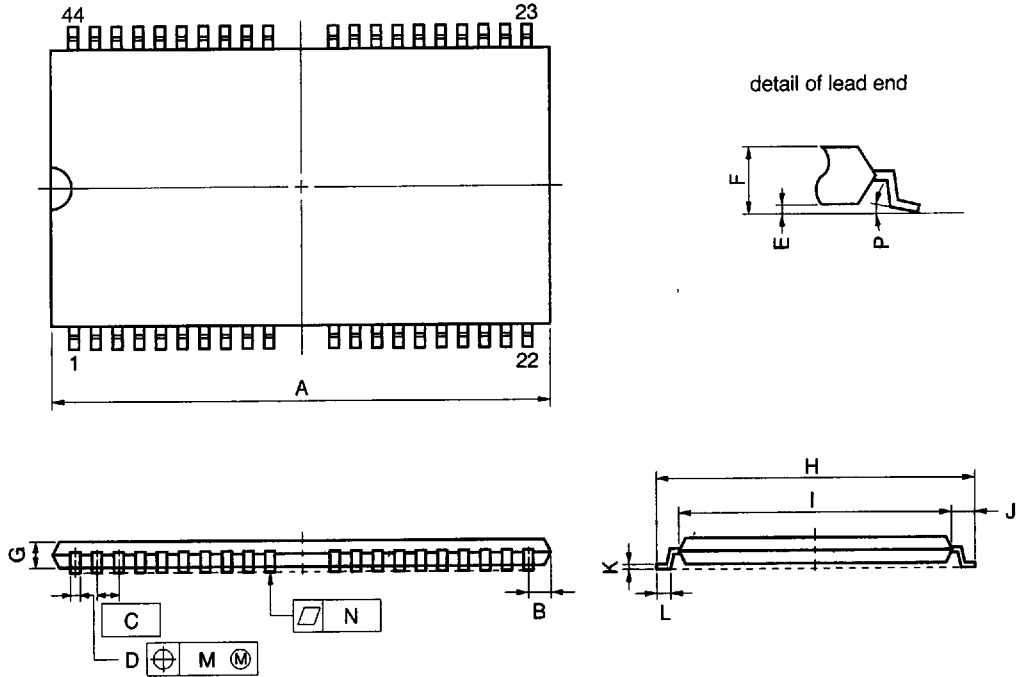
Hidden Refresh Cycle (Write)



Remark \overline{OE} : Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)

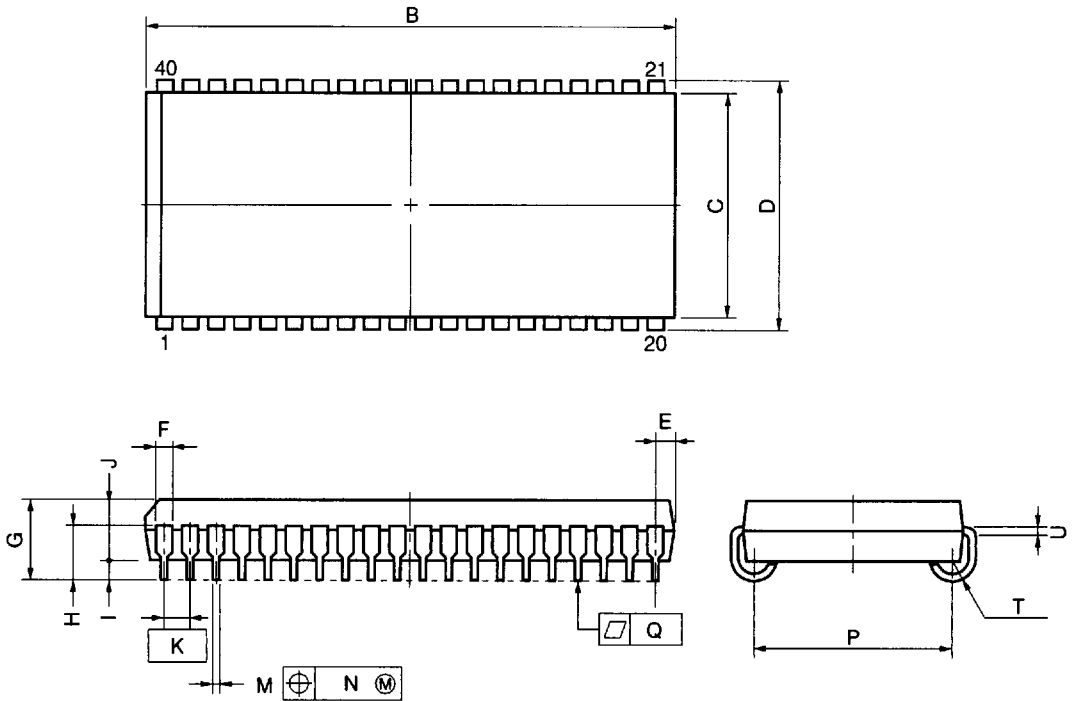


NOTE
 Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S4-G5-80-7JF4

40 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	26.29 ^{+0.2} _{-0.35}	1.035 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

P40LE-400A-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD42S4210AL, 424210AL.

Types of Surface Mount Device

μ PD42S4210ALG5, 424210ALG5: 44-pin plastic TSOP (II) (400 mil)

μ PD42S4210ALLE, 424210ALLE: 40-pin plastic SOJ (400 mil)