

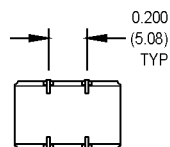
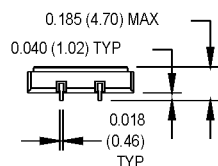
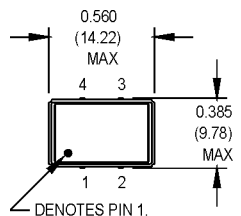
M5R Series

9x14 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillator



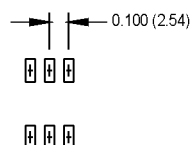
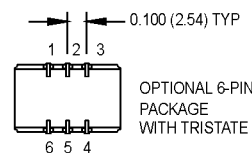
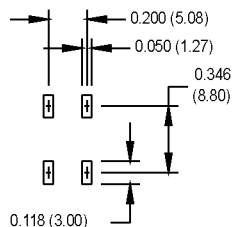
Pin Connections

FUNCTION	4 Pin	6 Pin
N/C or Output $\bar{Q}$	1	1
Tri-state		2
Ground/Cover	2	3
Output Q	3	4
N/C		5
+Vcc	4	6



All dimensions in inches (mm).

SUGGESTED SOLDER PAD LAYOUT



Ordering Information

Product Series	M5R	1	8	Z	Q	J	00.0000 MHz
Temperature Range	1: 0°C to +70°C	2: -40°C to +85°C					
	6: -20°C to +70°C	7: -0°C to +85°C					
	8: 0°C to +50°C						
Stability	3: ±100 ppm	4: ±50 ppm	5: ±35 ppm				
	6: ±25 ppm	8: ±20 ppm					
Output Type	R: Complementary Tri-state	T: Single Tri-state					
	Z: Complementary Non-Tri-state	X: Single Non-Tri-state					
Symmetry/Output Logic Type	L: 45/55% LVDS	P: 45/55% LVPECL					
	H: 40/60% LVDS	Q: 40/60% LVPECL					
Package/Lead Configurations							
J: J-lead							
Frequency (customer specified)							

	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Electrical Specifications	Frequency Range	F	0.75		800	MHz	
	Frequency Stability	$\Delta F/F$	(See Ordering Information)				See Note 1
	Operating Temperature	T _s	-40		+85	°C	See ordering information
	Storage Temperature	T _A	-55		+125	°C	
	Input Voltage	V _{cc}	3.135	3.3	3.465	V	
	PECL Input Current	I _{cc}			60	mA	
	0.75 MHz to 24 MHz				95	mA	
	24 MHz to 96 MHz				105	mA	
	LVDS Input Current	I _{cc}			30	mA	
	0.75 MHz to 24 MHz				60	mA	
	24 MHz to 800 MHz						
	Symmetry (Duty Cycle)		40	50	60	%	At V _{cc} -1.3 VDC (LVPECL)
	(Per Symmetry Code)		40	50	60	%	At 50% of waveform (LVDS)
	Load		50 Ohms to V _{cc} -2 VDC				LVPECL waveform (Note 2)
			50 Ohm differential load				LVDS waveform (Note 3)
Environmental	Rise/Fall Time	Tr/Tf		0.35	0.55	ns	At 20/80%
	LVPECL			0.35	0.55	ns	At 20/80%
	Logic "1" Level	V _{oh}	V _{cc} -1.02			V	LVPECL
	Logic "0" Level	V _{ol}			V _{cc} -1.63	V	LVPECL
	Cycle to Cycle Jitter			10	20	ps RMS	1 Sigma
	Phase Jitter	ϕ_J		3	5	ps RMS	Integrated 12 kHz - 20 MHz
	Peak to Peak Jitter (+/-)	T _J		21	35	ps	@ BER 1E-12
	Differential Voltage	V _o	250	340	450	mV	LVDS
	Tri-state Output "On"	OE	2.8			V	Pin 2 voltage
	Tri-state Output "Off"	OE			0.6	V	Pin 2 voltage
	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C					
	Vibration	Per MIL-STD-202, Method 201 & 204					
	Reflow Solder Conditions	See "Figure 2" on page 147					
	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 ⁻⁶ atm.cc/s of helium)					
	Solderability	Per EIAJ-STD-002					

1. Calibration, deviation over temperature, shock, vibration, and aging.
2. See load circuit diagram #5 on page 149.
3. See load circuit diagram #9 on page 149.

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