Advance Information

Am28F256

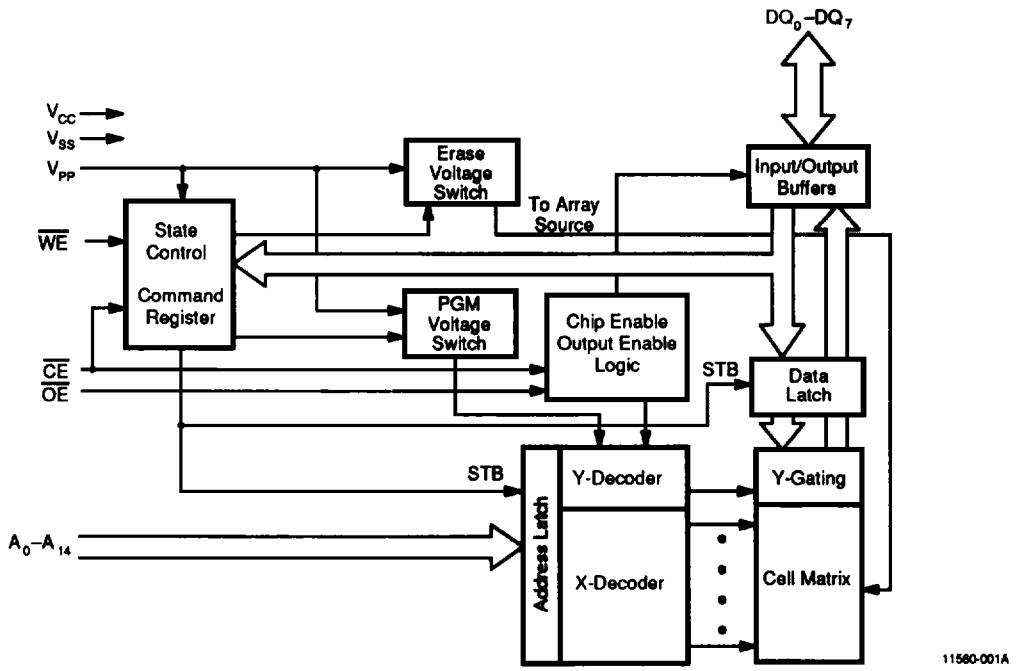
32,768 x 8-Bit Flash E²PROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  - — One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide 32-pin EEPROM Pinouts**
  - — 32-pin DIP
  - — 32-pin PLCC
- **Flashrite™ Programming**
  - — 10 µS Typical Byte-Program
  - — Less than 0.5 Second Typical Chip Program
- **Program and Erase Voltage 12.0V ± 5% V_{PP}**
- **Advanced CMOS Technology**
  - — EPROM Compatible Process
  - — Extensive Manufacturing Experience
- **Low Power Consumption**
  - — 30 mA Maximum Active Current
  - — 100 µA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **10,000 Program/Erase Cycles**
- **Provides On-Board Functionality for In-System-Write**
- **High Performance**
  - — 90 nS Maximum Access Time
- **On Board Address and Data Latches**
- **5V ±10% Single Power Supply**

BLOCK DIAGRAM



Publication # 11560 Rev. A Amendment /0
Issue Date: February, 1989

GENERAL DESCRIPTION

This device is an alternative to the full-featured EEPROM.

The 28F256 is targeted for in-system alterable code- or data-storage applications where full-feature EEPROM functionality is either not required or not cost effective. The Am28F256 CMOS Flash memory provides the highest performance and most cost-effective alternative for rewritable non-volatile memory. Flash memory adds electrical chip-erase and reprogramming to AMD's EPROM technology. The entire memory content may be Flash erased and reprogrammed OR PROM programmer, or test socket, on board during subassembly test, in-system during final test or after sale. In-system electrical erasure increases the memory's flexibility, while providing time and cost savings.

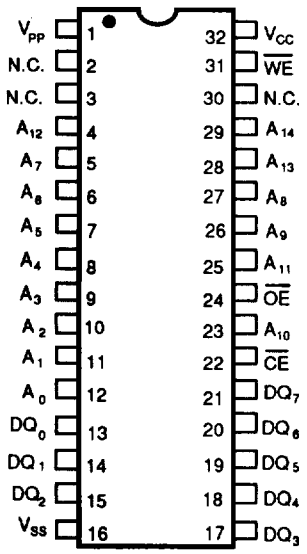
The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory array may be erased and reprogrammed on-board using AMD's Flasherase™ and Flashrite™ programming algorithms respectively.

Typical Applications

Flash memory is ideal for storing code or data-tables in embedded control applications where periodic updates or data down-loading may be required. Code updates may occur throughout the entire life of a system. Beginning with prototyping, code updates may also be necessary during subassembly or even in after-sale service. Electrical chip erasure eliminates the 15 to 20 minute ultraviolet erase and streamlines code updates. In addition both DIP or PLCC Flash devices may be soldered to the circuit board during subassembly. Test codes may be programmed into the device on board. Prior to shipment final code is downloaded to the device. Thus, Flash technology eliminates unnecessary handling and less reliable socketed connections, saves board space, and adds increased manufacturing flexibility. After-sale code updates are performed locally via an edge-connector, or remotely over a serial communication link.

CONNECTION DIAGRAMS

DIP



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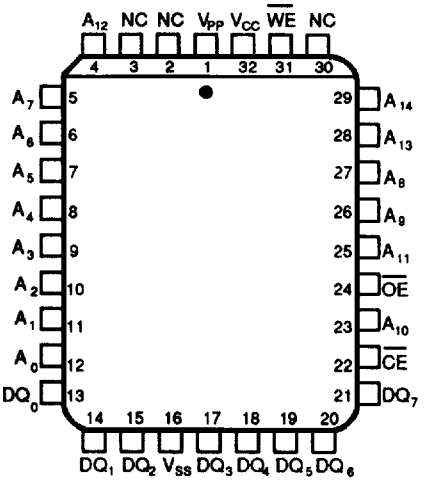
LCC/PLCC



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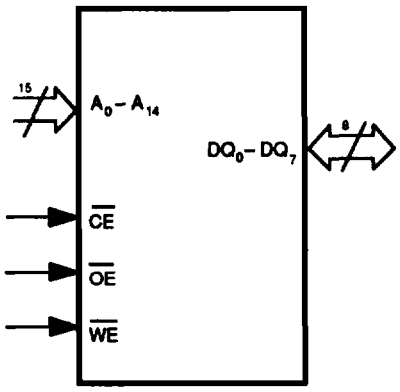
LOGIC SYMBOL



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FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming gives flash memory the flexibility of EEPROM. A command register in the Flash device manages the electrical erasure and reprogramming. The command register architecture allows for fixed power supplies during erasure and programming and does not require high voltage on control pins.

Read Mode

The Flash device functions as a read only memory when high voltage is not applied to the V_{pp} pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

Programming / Read Mode

High voltage on the V_{pp} pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the V_{pp} pin. All functions associated with altering memory contents (erase, erase-verify, program, and program-verify) are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes. As with EEPROM devices, the 28F256 uses a dedicated $\overline{WE}$ control pin for command execution.

The command register is alterable only when high voltage is applied to V_{pp}. When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory. V_{pp} may be controlled with system hardware to provide secure write protect.

Performance

AMD's Flash memories offer access times as fast as 90ns. This high performance allows operation of high-speed microprocessors and microcontrollers without wait-states. The Flash architecture supports separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls in order to eliminate bus contention.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) –40°C to +85°C

Extended Commercial (E) Devices
Case Temperature (Tc) –55°C to +125°C

Military (M) Devices
Case Temperature (Tc) –55°C to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.