

TL4810B, TL4810BI VACUUM FLUORESCENT DISPLAY DRIVERS

SLDS006C – D2716, DECEMBER 1984 – REVISED MAY 1993

- Each Device Drives Ten Lines
- 60-V Output Voltage Rating
- 40-mA Output Source Current
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs
- Improved Direct Replacement for UCN4810A and TL4810A

description

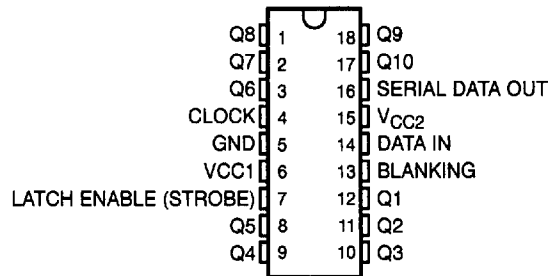
The TL4810B and TL4810BI are monolithic BIFDFT† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

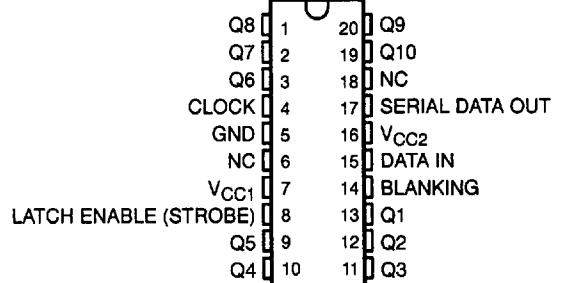
Outputs are totem-pole structures formed by npn emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and 40-mA source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pullup resistor to V_{CC1} when driven by TTL logic.

The TL4810B is characterized for operation from 0°C to 70°C. The TL4810BI is characterized for operation from -40°C to 85°C.

**N PACKAGE
(TOP VIEW)**



**DW PACKAGE
(TOP VIEW)**



NC—No internal connection

†BIFDFT – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

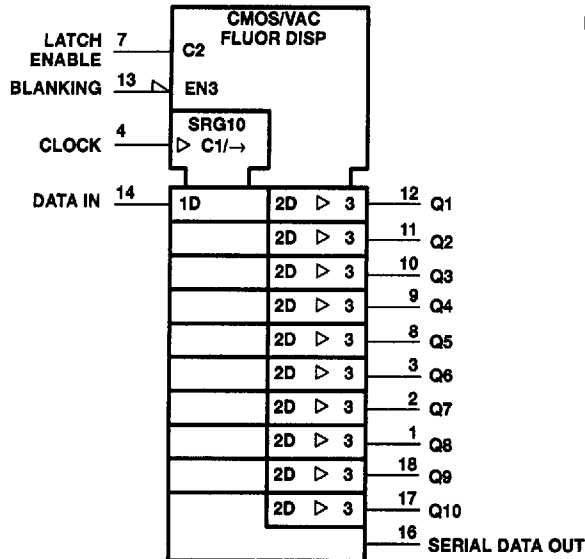
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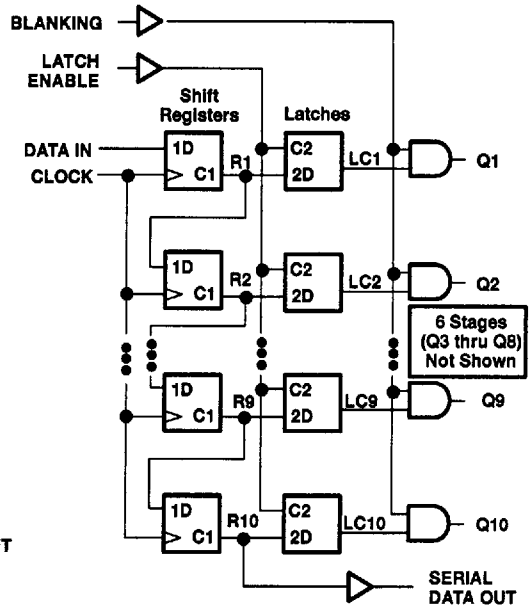
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the N package.

logic diagram (positive logic)



FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R10‡	LATCHES LC1 THRU LC10	SERIAL	OUTPUTS Q1 THRU Q10
	CLOCK	LATCH ENABLE	BLANKING				
Load	↑	X	X	Load and shift‡	Determined by LATCH ENABLE§	R10	Determined by BLANKING
	No↑	X	X	No change			
Latch	X	L	X	As determined above	Stored data New data	R10	Determined by BLANKING
	X	H	X				
Blank	X	X	H	As determined above	Determined by LATCH ENABLE§	R10	All L LC1 thru LC10, respectively
	X	X	L				

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

‡ Register R10 takes on the state of R9, R9 takes on the state of R8...R2 takes on the state of R1, and R1 takes on the state of the data input.

§ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

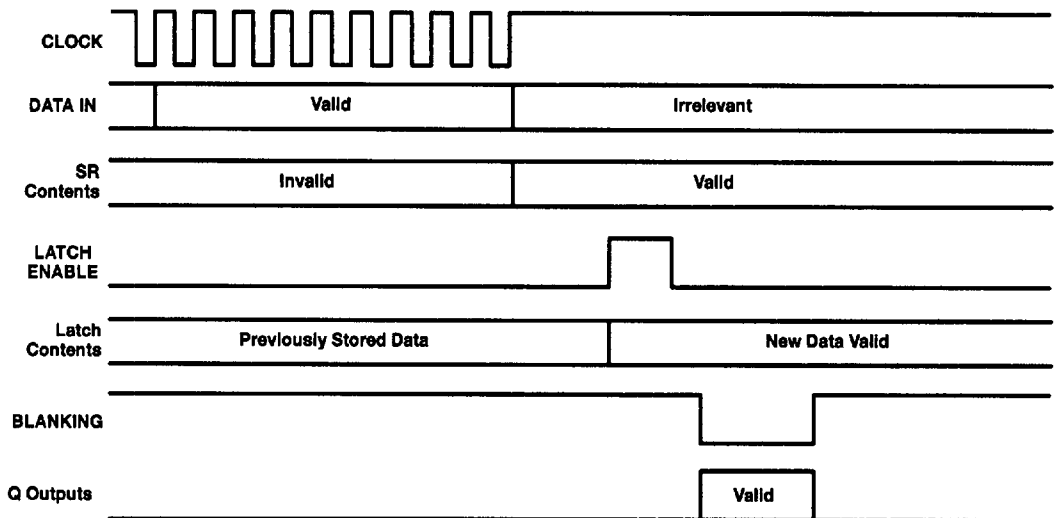
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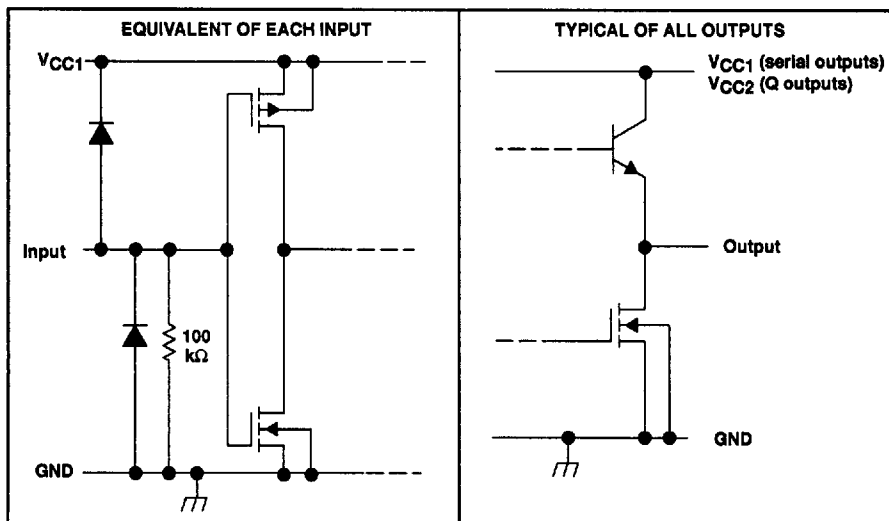
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typical operating sequence



schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1} (see Note 1)	18 V
Driver supply voltage, V_{CC2}	70 V
Output voltage, V_O	70 V
Input voltage range, V_I	-0.3 V to $V_{CC1} + 0.3$ V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: TL4810B	0°C to 70°C
TL4810BI	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

PARAMETER	TL4810B			TL4810BI			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}	4.75		15.75	4.75		15.75	V
Supply voltage, V_{CC2}	5		60	5		60	V
High-level input voltage, V_{IH}	$V_{CC1} = 5$ V		3.5	5.3	3.5	5.3	V
	$V_{CC1} = 15$ V		13.5	15.3	13.5	15.3	
Low-level input voltage, V_{IL}	-0.3†		0.8	-0.3†		0.8	V
Continuous high-level output current, I_{OH}			-25			-25	mA
Operating free-air temperature, T_A	0		70	-40		85	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltages only.



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**electrical characteristics over recommended operating free-air temperature range,
V_{CC1} = 5 V to 15 V, V_{CC2} = 60 V, GND = 0 (unless otherwise noted)**

PARAMETER		TEST CONDITIONST	TL4810B			TL4810BI			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{OH}	High-level output voltage	Q outputs	I _{OH} = -25 mA			57.5	58	57.5	58	V
		SERIAL DATA OUT	V _{CC1} = 5 V, I _{OH} = -100 μA		4	4.5	4	4.5		
		V _{CC1} = 15 V, I _{OH} = -100 μA		14	14.7	14	14.7			
V _{OL}	Low-level output voltage	Q outputs	I _{OL} = 1 μA, BLANKING at V _{CC1}			0.5	1	0.5	1	V
		SERIAL DATA OUT	V _{CC1} = 5 V, I _{OL} = 100 μA		0.05	0.1	0.05	0.1		
		V _{CC1} = 15 V, I _{OL} = 100 μA		0.02	0.1	0.02	0.1			
I _{OL}	Low-level Q output current (pulldown current)	V _O = 60 V, BLANKING at V _{CC1} , T _A = MIN to 70°C	2.5	3.7	2.5	3.7			mA	
		V _O = 60 V, BLANKING at V _{CC1} , T _A = 85°C			2					
I _{O(off)}	Off-state output current	V _O = 0, BLANKING at V _{CC1} , T _A = MAX		-1	-15		-1	-15	μA	
I _H	High-level input current	V _I = V _{CC1}		30	50		30	50	μA	
I _{CC1}	Supply current from V _{CC1}	All inputs at 0 V, One Q output high	V _{CC1} = 5 V	10	50	10	50	μA		
			V _{CC1} = 15 V	10	100	10	100			
		All inputs at 0 V, All outputs low	V _{CC1} = 5 V	10	50	10	50			
			V _{CC1} = 15 V	10	100	10	100			
I _{CC2}	Supply current from V _{CC2}	All outputs low	0.5	1	0.5	1	mA			
		All outputs high, T _A = 0°C to MAX	2.7	4	2.7	4				
		All outputs high, T _A = -40°C				5				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at T_A = 25°C, except for I_O.

timing requirements over recommended operating free-air temperature range

		V _{CC1} = 5 V		V _{CC1} = 15 V		UNIT
		MIN	MAX	MIN	MAX	
t _w (CKH)	Pulse duration, CLOCK high	250		50		ns
t _w (LEH)	Pulse duration, LATCH ENABLE high	250		50		ns
t _{su} (D)	Setup time, DATA IN before CLOCK↑	125		25		ns
t _h (D)	Hold time, DATA IN after CLOCK↑	125		25		ns
t _d (CKH-LEH)	Delay time, CLOCK↑ to LATCH ENABLE high	125		25		ns

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			UNIT
t _{pd}	Propagation delay time, LATCH ENABLE to Q outputs	V _{CC1} = 5 V		1	μs
		V _{CC1} = 15 V		0.5	



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PARAMETER MEASUREMENT INFORMATION

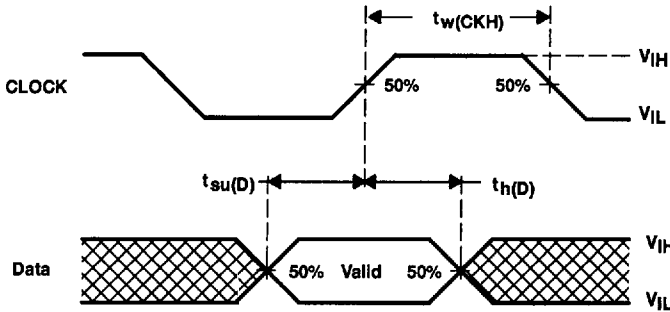


Figure 1. Input Timing

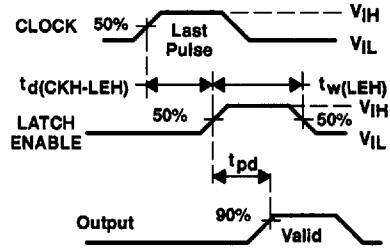


Figure 2. Output Switching Times

THERMAL INFORMATION

DW PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

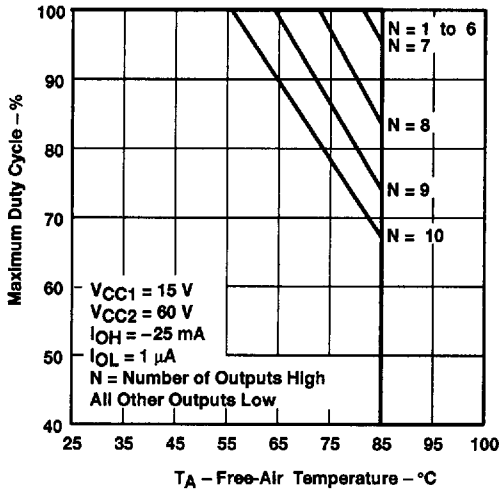


Figure 3

N PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

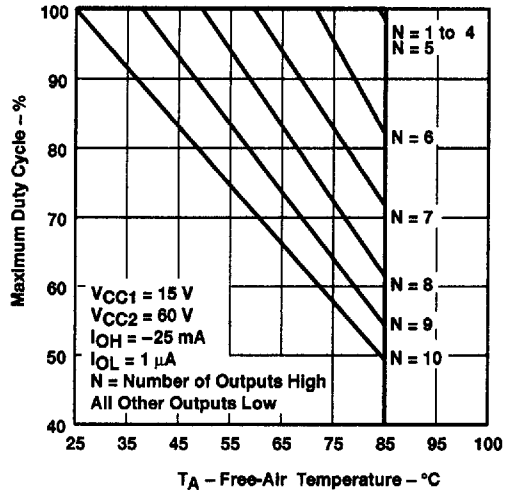


Figure 4

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