

**M1S25664DSH8C1G / M1S12864DSH4C1G
M1N25664DSH8C1G (GREEN)
256MB and 128MB
PC2700
Unbuffered DDR SO-DIMM**



200 pin Unbuffered DDR SO-DIMM

Based on DDR333 256M bit C Die device

Features

- 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- Unbuffered DDR SO-DIMM based on DDR 256Mbit die C device, organized as 16Mx16 using Nanya's 110nm technology
- Performance:

	PC2700	Unit
Speed Sort	6K	
DIMM $\overline{\text{CAS}}$ Latency	2.5	
f_{CK} Clock Frequency	166	MHz
t_{CK} Clock Cycle	6	ns
f_{DQ} DQ Burst Frequency	333	MHz

- Intended for 166 MHz applications
- Inputs and outputs are SSTL-2 compatible
- $V_{\text{DD}} = V_{\text{DDQ}} = 2.5V \pm 0.2V$ (DDR333 devices)
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions

- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
 - DIMM $\overline{\text{CAS}}$ Latency: 2/2.5(6K)
 - Burst Type: Sequential or Interleave
 - Burst Length: 2, 4, 8
 - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 7.8 μs Max. Average Periodic Refresh Interval
- Serial Presence Detect EEPROM
- Gold contacts
- SDRAMs are packaged in TSOP packages

Description

M1S25664DSH8C1G, M1S12864DSH4C1G and M1N25664DSH8C1G are unbuffered 200-Pin Double Data Rate (DDR) Synchronous DRAM Small Outline Dual In-Line Memory Modules (SO-DIMM). M1S12864DSH4C1G is 128MB module, organized as a single rank using four 16Mx16 TSOP devices. M1S25664DSH8C1G and M1N25664DSH8C1G are 256MB modules, organized as dual ranks using eight 16Mx16 TSOP devices.

Depending on the speed grade, these SO-DIMMs are intended for use in applications operating up to 166 MHz clock speeds and achieves high-speed data transfer rates of up to 333 MHz. Prior to any access operation, the device $\overline{\text{CAS}}$ latency and burst type/ length/operation type must be programmed into the SO-DIMM by address inputs and I/O inputs BA0 and BA1 using the mode register set cycle.

The DDR SO-DIMM uses a serial EEPROM and through the use of a standard IIC protocol the serial presence-detect implementation (SPD) can be accessed. The first 128 bytes of the SPD data are programmed with the module characteristics as defined by JEDEC.

Ordering Information

Part Number	Organization	Speed			Power	Leads	Note
M1S25664DSH8C1G-6K	32Mx64	DDR333	PC2700 2.5-3-3	166MHz (6ns @ CL = 2.5)	2.5V	Gold	
M1S12864DSH4C1G-6K	16Mx64						
M1N25664DSH8C1G-6K	32Mx64						Green

For the closest sales office or information, please visit: www.elixir-memory.com

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Pin Description

CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	Differential Clock Inputs.	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
\overline{RAS}	Row Address Strobe	DM0-DM7	Input Data Mask
\overline{CAS}	Column Address Strobe	V _{DD}	Power
WE	Write Enable	V _{DDQ}	Supply voltage for DQs
$\overline{S0}$, $\overline{S1}$	Chip Selects	V _{SS}	Ground
A0-A9, A11, A12	Address Inputs	NC	No Connect
A10/AP	Address Input/Auto-precharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
V _{REF}	Ref. Voltage for SSTL_2 inputs	SA0-2	Serial Presence Detect Address Inputs
V _{DDID}	V _{DD} Identification flag.	V _{DDSPD}	Serial EEPROM positive power supply

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REF}	2	V _{REF}	51	V _{SS}	52	V _{SS}	101	A9	102	A8	151	DQ42	152	DQ46
3	V _{SS}	4	V _{SS}	53	DQ19	54	DQ23	103	V _{SS}	104	V _{SS}	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	V _{DD}	156	V _{DD}
7	DQ1	8	DQ5	57	V _{DD}	58	V _{DD}	107	A5	108	A4	157	V _{DD}	158	$\overline{CK1}$
9	V _{DD}	10	V _{DD}	59	DQ25	60	DQ29	109	A3	110	A2	159	V _{SS}	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	V _{SS}	162	V _{SS}
13	DQ2	14	DQ6	63	V _{SS}	64	V _{SS}	113	V _{DD}	114	V _{DD}	163	DQ48	164	DQ52
15	V _{SS}	16	V _{SS}	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	\overline{RAS}	167	V _{DD}	168	V _{DD}
19	DQ8	20	DQ12	69	V _{DD}	70	V _{DD}	119	WE	120	\overline{CAS}	169	DQS6	170	DM6
21	V _{DD}	22	V _{DD}	71	NC	72	NC	121	$\overline{S0}$	122	$\overline{S1}$	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	NC	74	NC	123	DU	124	DU	173	V _{SS}	174	V _{SS}
25	DQS1	26	DM1	75	V _{SS}	76	V _{SS}	125	V _{SS}	126	V _{SS}	175	DQ51	176	DQ55
27	V _{SS}	28	V _{SS}	77	DQS8	78	NC	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	NC	80	NC	129	DQ33	130	DQ37	179	V _{DD}	180	V _{DD}
31	DQ11	32	DQ15	81	V _{DD}	82	V _{DD}	131	V _{DD}	132	V _{DD}	181	DQ57	182	DQ61
33	V _{DD}	34	V _{DD}	83	NC	84	NC	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	V _{DD}	85	DU	86	DU	135	DQ34	136	DQ38	185	V _{SS}	186	V _{SS}
37	$\overline{CK0}$	38	V _{SS}	87	V _{SS}	88	V _{SS}	137	V _{SS}	138	V _{SS}	187	DQ58	188	DQ62
39	V _{SS}	40	V _{SS}	89	CK2	90	V _{SS}	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	$\overline{CK2}$	92	V _{DD}	141	DQ40	142	DQ44	191	V _{DD}	192	V _{DD}
43	DQ17	44	DQ21	93	V _{DD}	94	V _{DD}	143	V _{DD}	144	V _{DD}	193	SDA	194	SA0
45	V _{DD}	46	V _{DD}	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	V _{DDSPD}	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	V _{SS}	150	V _{SS}	199	V _{DDID}	200	DU

Note: All pin assignments are consistent for all 8-byte unbuffered versions.

Input/Output Functional Description

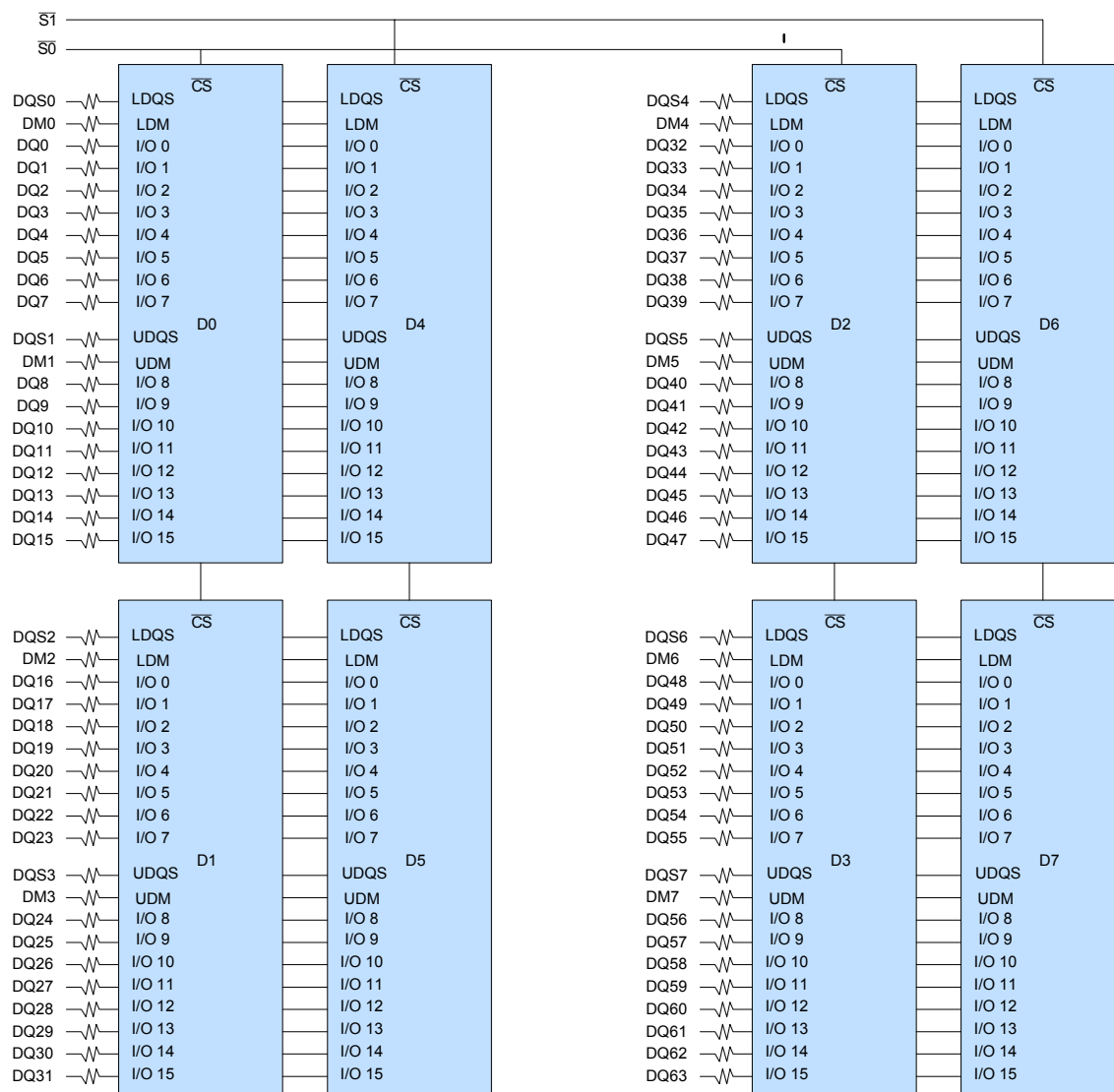
Symbol	Type	Polarity	Function
CK0, CK1, CK2, $\overline{\text{CK0}}, \overline{\text{CK1}}, \overline{\text{CK2}}$	(SSTL)	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	(SSTL)	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S0}}, \overline{\text{S1}}$	(SSTL)	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by S0; Bank 1 is selected by S1.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, these lines define the row address when sampled at the rising clock edge. During a Read or Write command cycle, these lines defines the column address when sampled at the rising clock edge. In addition to the column address, AP is used to invoke auto-precharge operation at the end of the Burst Read or Write cycle. If AP is high, auto-precharge is selected and BA0/BA1 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQS0 – DQS8	(SSTL)	Active High	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data. DQS8 is used for ECC modules (CB0-CB7) and is not used on x64 modules.
CB0 – CB7	(SSTL)	-	Data Check Bit Input/Output pins. Used on ECC modules and is not used on x64 modules.
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
$V_{\text{DD}}, V_{\text{SS}}$	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

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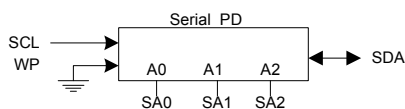
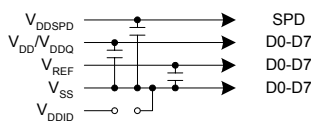


Functional Block Diagram

256MB, 2 Ranks, 8 devices, 16Mx16 DDR SDRAMs



- BA0-BA1 → BA0-BA1 : SDRAMs D0-D7
- A0-A12 → A0-A12 : SDRAMs D0-D7
- RAS → RAS : SDRAMs D0-D7
- CAS → CAS : SDRAMs D0-D7
- CKE0 → CKE : SDRAMs D0-D3
- CKE1 → CKE : SDRAMs D4-D7
- WE → WE : SDRAMs D0-D7



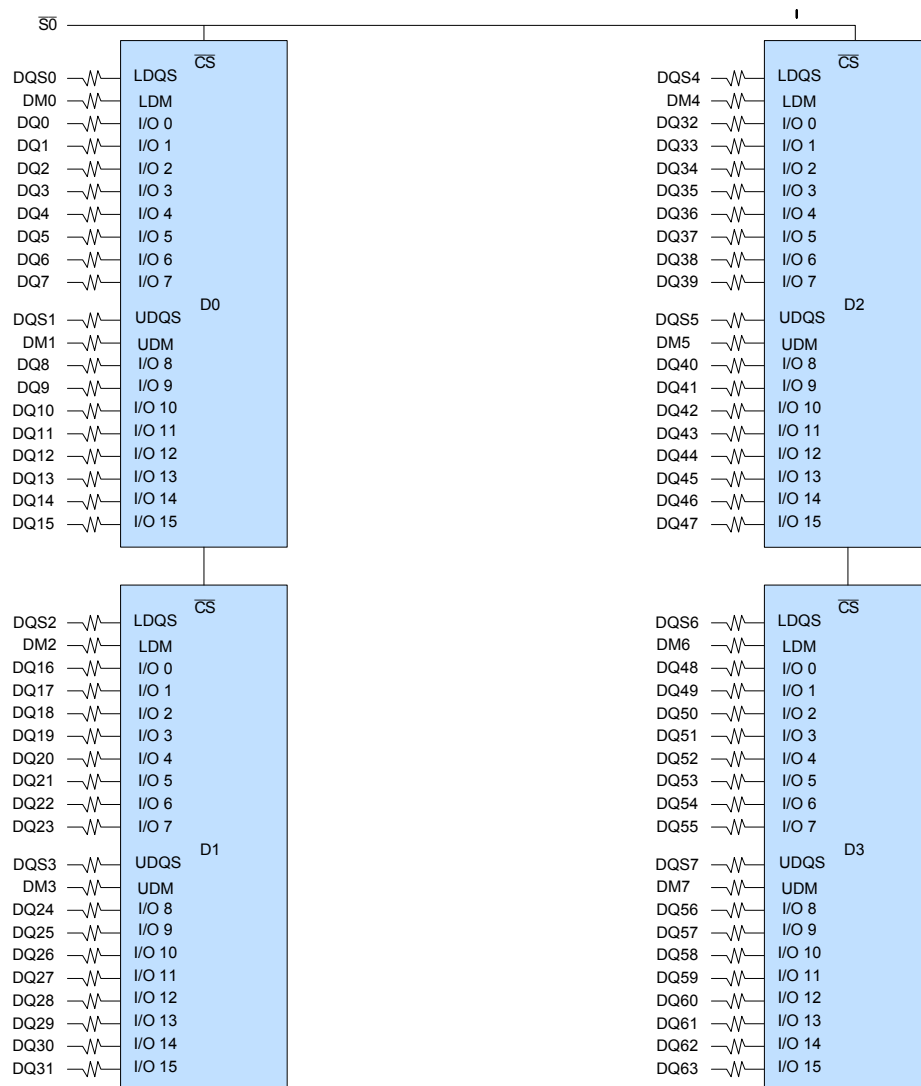
- CK0 → 4 loads
- CK0 → 4 loads
- CK1 → 4 loads
- CK1 → 4 loads
- CK2 → 0 loads
- CK2 → 0 loads

Notes :

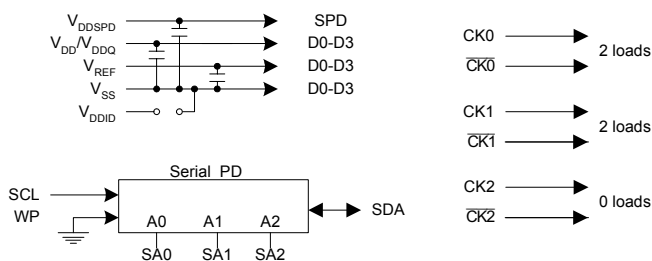
1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22+/- 5% Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD is not equal to VDDQ.

Functional Block Diagram

128MB, 1 Rank, 4 devices, 16Mx16 DDR SDRAMs



- BA0-BA1 → BA0-BA1 : SDRAMs D0-D3
- A0-A12 → A0-A12 : SDRAMs D0-D3
- RAS → RAS : SDRAMs D0-D3
- CAS → CAS : SDRAMs D0-D3
- CKE0 → CKE : SDRAMs D0-D3
- CKE1 → N.C.
- WE → WE : SDRAMs D0-D3



Notes :

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22+/- 5% Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
 STRAP OUT (OPEN): V_{DD} = V_{DDQ}
 STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

**M1S25664DSH8C1G / M1S12864DSH4C1G
M1N25664DSH8C1G (GREEN)
Unbuffered DDR SO-DIMM**



Serial Presence Detect

SPD Description

Byte	Description	Byte	Description
0	Number of Serial PD Bytes Written during Production	26	Maximum Data Access Time from Clock at CL=1
1	Total Number of Bytes in Serial PD device	27	Minimum Row Precharge Time (t_{RP})
2	Fundamental Memory Type	28	Minimum Row Active to Row Active delay (t_{RRD})
3	Number of Row Addresses on Assembly	29	Minimum RAS to CAS delay (t_{RCD})
4	Number of Column Addresses on Assembly	30	Minimum RAS Pulse Width (t_{RAS})
5	Number of DIMM Rank	31	Module Bank Density
6	Data Width of Assembly	32	Address and Command Setup Time Before Clock
7	Data Width of Assembly (cont')	33	Address and Command Hold Time After Clock
8	Voltage Interface Level of this Assembly	34	Data Input Setup Time Before Clock
9	DDR SDRAM Device Cycle Time CL=2.5	35	Data Input Hold Time After Clock
10	DDR SDRAM Device Access Time from Clock CL=2.5	36-40	Reserved
11	DIMM Configuration Type	41	Minimum Active/Auto-refresh Time (t_{RC})
12	Refresh Rate/Type	42	Auto-refresh to Active/Auto-refresh Command Period (t_{RFC})
13	Primary DDR SDRAM Width	43	Max Cycle Time ($t_{CK\ max}$)
14	Error Checking DDR SDRAM Device Width	44	Maximum DQS-DQ Skew Time ($t_{DQS\Omega}$)
15	DDR SDRAM Device Attr: Min CLK Delay, Random Col Access	45	Maximum Read Data Hold Skew Factor (t_{QHS})
16	DDR SDRAM Device Attributes: Burst Length Supported	46-61	Reserved
17	DDR SDRAM Device Attributes: Number of Device Banks	62	SPD Revision
18	DDR SDRAM Device Attributes: CAS Latencies Supported	63	Checksum Data
19	DDR SDRAM Device Attributes: CS Latency	64-71	Manufacturer's JEDEC ID Code
20	DDR SDRAM Device Attributes: WE Latency	72	Module Manufacturing Location
21	DDR SDRAM Device Attributes:	73-90	Module Part number
22	DDR SDRAM Device Attributes: General	91-92	Module Revision Code
23	Minimum Clock Cycle CL=2.5	93-94	Module Manufacturing Data yy= Binary coded decimal year code, 0-99(Decimal), 00-63(Hex) ww= Binary coded decimal year code, 01-52(Decimal), 01-34(Hex)
24	Maximum Data Access Time from Clock at CL=2	95-98	Module Serial Number
25	Minimum Clock Cycle Time at CL=1	99-127	Reserved

**M1S25664DSH8C1G / M1S12864DSH4C1G
M1N25664DSH8C1G (GREEN)
Unbuffered DDR SO-DIMM**



SPD Values for M1S25664DSH8C1G / M1N25664DSH8C1G

Byte	M1S25664DSH8C1G		M1N25664DSH8C1G	
	Value	Hex	Value	Hex
0	128	80	128	80
1	256	08	256	08
2	SDRAM DDR	07	SDRAM DDR	07
3	13	0D	13	0D
4	9	09	9	09
5	2	02	2	02
6	x64	40	x64	40
7	x64	00	x64	00
8	SSTL 2.5V	04	SSTL 2.5V	04
9	6.0ns	60	6.0ns	60
10	0.70ns	70	0.70ns	70
11	Non-Parity	00	Non-Parity	00
12	SR/1x(7.8us)	82	SR/1x(7.8us)	82
13	x16	10	x16	10
14	N/A	00	N/A	00
15	1 Clock	01	1 Clock	01
16	2,4,8	0E	2,4,8	0E
17	4	04	4	04
18	2/2.5	0C	2/2.5	0C
19	0	01	0	01
20	1	02	1	02
21	Differential Clock	20	Differential Clock	20
22	±0.2V Tolerance	C0	±0.2V Tolerance	C0
23	7.5ns	75	7.5ns	75
24	0.75ns	75	0.75ns	75
25	N/A	00	N/A	00
26	N/A	00	N/A	00
27	18ns	48	18ns	48
28	12ns	30	12ns	30
29	18ns	48	18ns	48
30	42ns	2A	42ns	2A
31	128MB	20	128MB	20
32	0.75ns	75	0.75ns	75
33	0.75ns	75	0.75ns	75
34	0.45ns	45	0.45ns	45
35	0.45ns	45	0.45ns	45
36-40	Undefined	00	Undefined	00
41	60ns	3C	60ns	3C
42	72ns	48	72ns	48
43	12ns	30	12ns	30
44	0.45ns	2D	0.45ns	2D
45	0.55ns	55	0.55ns	55
46-61	Undefined	00	Undefined	00
62	Initial	00	1.0	10
63	Checksum	ED	Checksum	FE
64-71	NANYA	7F7F7F0B00000000	NANYA	7F7F7F0B00000000
72	Assembly	--	Assembly	--
73-90	Module PN	--	Module PN	--
91-92	Revision	--	Revision	--
93-94	Year/Week Code	--	Year/Week Code	--
95-98	Serial Number	--	Serial Number	--
99-127	Reserved	--	Reserved	--

M1S25664DSH8C1G / M1S12864DSH4C1G
M1N25664DSH8C1G (GREEN)
Unbuffered DDR SO-DIMM



SPD Values for M1S12864DSH4C1G

M1S12864DSH4C1G		
Byte	Value	Hex
0	128	80
1	256	08
2	SDRAM DDR	07
3	13	0D
4	9	09
5	1	01
6	x64	40
7	x64	00
8	SSTL 2.5V	04
9	6.0ns	60
10	0.70ns	70
11	Non-Parity	00
12	SR/1x(7.8us)	82
13	x16	10
14	N/A	00
15	1 Clock	01
16	2,4,8	0E
17	4	04
18	2/2.5	0C
19	0	01
20	1	02
21	Differential Clock	20
22	±0.2V Tolerance	C0
23	7.5ns	75
24	0.75ns	75
25	N/A	00
26	N/A	00
27	18ns	48
28	12ns	30
29	18ns	48
30	42ns	2A
31	128MB	20
32	0.75ns	75
33	0.75ns	75
34	0.45ns	45
35	0.45ns	45
36-40	Undefined	00
41	60ns	3C
42	72ns	48
43	12ns	30
44	0.45ns	2D
45	0.55ns	55
46-61	Undefined	00
62	Initial	00
63	Checksum	EC
64-71	NANYA	7F7F7F0B00000000
72	Assembly	--
73-90	Module PN	--
91-92	Revision	--
93-94	Year/Week Code	--
95-98	Serial Number	--
99-127	Reserved	--

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.5 to $V_{DDQ} + 0.5$	V
V_{IN}	Voltage on Input relative to V_{SS}	-0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	-0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	-0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	-55 to +150	°C
P_D	Power Dissipation (per device component)	1	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics and Operating Conditions

$T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$; $V_{DDQ} = V_{DD} = 2.5\text{V} \pm 0.2\text{V}$ (PC2700)

Symbol	Parameter	Min	Max	Units	Notes	
V_{DD}	Supply Voltage	PC2700	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	PC2700	2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V		
V_{REF}	I/O Reference Voltage	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	1, 2	
V_{TT}	I/O Termination Voltage (System)	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	1, 3	
$V_{IH(DC)}$	Input High (Logic1) Voltage	$V_{REF} + 0.15$	$V_{DDQ} + 0.3$	V	1	
$V_{IL(DC)}$	Input Low (Logic0) Voltage	-0.3	$V_{REF} - 0.15$	V	1	
$V_{IN(DC)}$	Input Voltage Level, CK and \overline{CK} Inputs	-0.3	$V_{DDQ} + 0.3$	V	1	
$V_{ID(DC)}$	Input Differential Voltage, CK and \overline{CK} Inputs	0.30	$V_{DDQ} + 0.6$	V	1, 4	
I_I	Input Leakage Current Any input $0\text{V} \leq V_{IN} \leq V_{DD}$; All other pins not under test = 0V	-10	10	μA	1	
I_{OZ}	Output Leakage Current DQs are disabled; $0\text{V} \leq V_{out} \leq V_{DDQ}$	-10	10	μA	1	
I_{OH}	Output High Current ($V_{OUT} = V_{DDQ} - 0.373\text{V}$, min V_{REF} , min V_{TT})	-16.8	-	mA	1	
I_{OL}	Output Low Current ($V_{OUT} = 0.373$, max V_{REF} , max V_{TT})	16.8	-	mA	1	

Note:

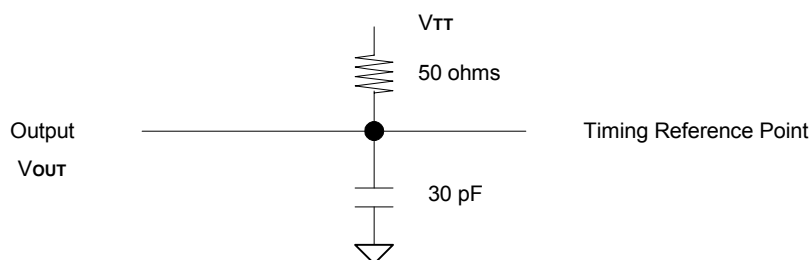
- Inputs are not recognized as valid until V_{REF} stabilizes.
- V_{REF} is expected to be equal to $0.5 V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
- V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .

AC Characteristics

Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

- All voltages referenced to V_{SS} .
- Tests for AC timing, I_{DD} , and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
- Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
- AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, \overline{CK}), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$ unless otherwise specified.
- The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuits



AC Operating Conditions

$T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 2.5V \pm 0.2V$ (PC2700)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage.	$V_{REF} + 0.31$		V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage.		$V_{REF} - 0.31$	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and \overline{CK} Inputs	0.62	$V_{DDQ} + 0.6$	V	1, 2, 3
$V_{IX(AC)}$	Input Differential Pair Cross Point Voltage, CK and \overline{CK} Inputs	$(0.5 * V_{DDQ}) - 0.2$	$(0.5 * V_{DDQ}) + 0.2$	V	1, 2, 4

Note:

- Input slew rate = 1V/ ns.
- Inputs are not recognized as valid until V_{REF} stabilizes.
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
- The value of V_{IX} is expected to equal $0.5 * V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

$T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 2.5\text{V} \pm 0.2\text{V}$ (PC2700)

Symbol	Parameter/Condition	Notes
IDD0	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1,2
IDD1	Operating Current: one bank; active/read/precharge; Burst = 2; $t_{RC} = t_{RC(MIN)}$; CL=2.5; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$; address and control inputs changing once per clock cycle	1,2
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$	1,2
IDD2N	Idle Standby Current: $CS \geq V_{IH(MIN)}$; all banks idle; $CKE \geq V_{IH(MIN)}$; $t_{CK} = t_{CK(MIN)}$; address and control inputs changing once per clock cycle	1,2
IDD3P	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$	1,2
IDD3N	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH(MIN)}$; $CKE \geq V_{IH(MIN)}$; $t_{RC} = t_{RAS(MAX)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1,2
IDD4R	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$	1,2
IDD4W	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; $t_{CK} = t_{CK(MIN)}$	1,2
IDD5	Auto-Refresh Current: $t_{RC} = t_{RFC(MIN)}$	1,2,3
IDD6	Self-Refresh Current: $CKE \leq 0.2\text{V}$	1,2
IDD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC(MIN)}$; $I_{OUT} = 0\text{mA}$.	1,2

1. IDD specifications are tested after the device is properly initialized.
 2. Input slew rate = 1V/ ns.
 3. Current at 7.8 μs is time averaged value of IDD5 at $t_{RFC(MIN)}$ and IDD2P over 7.8 μs .
- All IDD current values are calculated from device level.

Symbol	M1N25664DSH8C1G	M1S25664DSH8C1G	M1S12864DSH4C1G	Unit
	PC2700 (6K)	PC2700 (6K)	PC2700 (6K)	
IDD0	428	428	272	mA
IDD1	444	444	288	mA
IDD2P	32	32	16	mA
IDD2N	200	200	100	mA
IDD3P	80	80	40	mA
IDD3N	312	312	156	mA
IDD4R	504	504	348	mA
IDD4W	548	548	392	mA
IDD5	628	628	472	mA
IDD6	16	16	8	mA
IDD7	984	984	828	mA

* M1N25664DSH8C1G IDD was calculated from component IDD. It may differ from the actual measurement.

AC Timing Specifications for DDR SDRAM Devices Used on Module

$T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 2.5\text{V} \pm 0.2\text{V}$ (PC2100/PC2700) (Part 1 of 2)

Symbol	Parameter	6K PC2700		75B PC2100		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AC}	DQ output access time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	-0.75	+0.75	ns	1-4
t_{DQACK}	DQS output access time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	-0.75	+0.75	ns	1-4
t_{CH}	CK high-level width	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CK}	Clock cycle time CL=3	-	-	-	-		
t_{CK}	Clock cycle time CL=2.5	6	12	7.5	12	ns	1-4
t_{CK}	Clock cycle time CL=2	7.5	12	10	12	ns	1-4
t_{DH}	DQ and DM input hold time	0.45		0.5		ns	1-4, 15, 16
t_{DS}	DQ and DM input setup time	0.45		0.5		ns	1-4, 15, 16
t_{DIPW}	DQ and DM input pulse width (each input)	1.75		1.75		ns	1-4
t_{HZ}	Data-out high-impedance time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	-0.75	+0.75	ns	1-4, 5
t_{LZ}	Data-out low-impedance time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	-0.75	+0.75	ns	1-4, 5
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)		0.45		0.5	ns	1-4
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	t_{CH} or t_{CL}		t_{CH} or t_{CL}		t_{CK}	1-4
t_{QH}	Data output hold time from DQS	$t_{HP} -$ t_{QHS}		$t_{HP} -$ t_{QHS}		t_{CK}	1-4
t_{QHS}	Data hold Skew Factor		0.55		0.75	ns	1-4
t_{DQSS}	Write command to 1st DQS latching transition	0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSL} , t_{DQSH}	DQS input low (high) pulse width (write cycle)	0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time	2		2		t_{CK}	1-4
t_{WPRES}	Write preamble setup time	0		0		ns	1-4, 7
t_{WPST}	Write postamble	0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble	0.25		0.25		t_{CK}	1-4
t_{IH}	Address and control input hold time (fast slew rate)	0.75		0.9		ns	2-4, 9, 11, 12
t_{IS}	Address and control input setup time (fast slew rate)	0.75		0.9		ns	2-4, 9, 11, 12
t_{IH}	Address and control input hold time (slow slew rate)	0.8		1.0		ns	2-4, 10, 11, 12, 14

AC Timing Specifications for DDR SDRAM Devices Used on Module

$T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 2.5\text{V} \pm 0.2\text{V}$ (PC2100/PC2700) (Part 2 of 2)

Symbol	Parameter	6K PC2700		75B PC2100		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{IS}	Address and control input setup time (slow slew rate)	0.8		1.0		ns	2-4, 10-12, 14
t_{IPW}	Input pulse width	2.2		2.2		ns	2-4, 12
$t_{RP\ RE}$	Read preamble	0.9	1.1	0.9	1.1	t_{CK}	1-4
$t_{RP\ ST}$	Read postamble	0.40	0.60	0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command	42ns	120us	45ns	120us		1-4
t_{RC}	Active to Active/Auto-refresh command period	60		65		ns	1-4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	72		75		ns	1-4
t_{RCD}	Active to Read or Write delay	18		20		ns	1-4
t_{RAP}	Active to Read Command with Auto-precharge	18		20		ns	1-4
t_{RP}	Precharge command period	18		20		ns	1-4
t_{RRD}	Active bank A to Active bank B command	12		15		ns	1-4
t_{WR}	Write recovery time	15		15		ns	1-4
t_{DAL}	Auto-precharge write recovery + precharge time	$(\frac{t_{WR}}{t_{CK}}) + (\frac{t_{RP}}{t_{CK}})$		$(\frac{t_{WR}}{t_{CK}}) + (\frac{t_{RP}}{t_{CK}})$		t_{CK}	1-4, 13
t_{WTR}	Internal write to read command delay	1		1		t_{CK}	1-4
t_{PDEX}	Power down exit time	6		7.5		ns	1-4
t_{XSNR}	Exit self-refresh to non-read command	75		75		ns	1-4
t_{XSRD}	Exit self-refresh to read command	200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval		7.8		7.8	μs	1-4, 8

AC Timing Specification Notes

- Input slew rate = 1V/ns.
- The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$ is V_{REF} .
- Inputs are not recognized as valid until V_{REF} stabilizes.
- The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT} .
- t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on t_{DQSS} .
- A maximum of eight Auto refresh commands can be posted to any given DDR SDRAM device.
- For command/address input slew rate ≥ 1.0 V/ns. Slew rate is measured between $V_{\text{OH(AC)}}$ and $V_{\text{OL(AC)}}$.
- For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns. Slew rate is measured between $V_{\text{OH(AC)}}$ and $V_{\text{OL(AC)}}$.
- CK/ $\overline{\text{CK}}$ slew rates are ≥ 1.0 V/ns.
- These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
- For each of the terms in parentheses, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time. For example, for PC2100 at CL= 2.5, $t_{\text{DAL}} = (15\text{ns}/7.5\text{ns}) + (20\text{ns}/7.0\text{ns}) = 2 + 3 = 5$.
- An input setup and hold time derating table is used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (t_{IS})	Delta (t_{IH})	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+50	0	ps	1, 2
0.3 V/ns	+100	0	ps	1, 2

- Input slew rate is based on the lesser of the slew rates determined by either $V_{\text{IH(AC)}}$ to $V_{\text{IL(AC)}}$ or $V_{\text{IH(DC)}}$ to $V_{\text{IL(DC)}}$, similarly for rising transitions.
- These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

- An input setup and hold time derating table is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (t_{DS})	Delta (t_{DH})	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+75	+75	ps	1, 2
0.3 V/ns	+150	+150	ps	1, 2

- I/O slew rate is based on the lesser of the slew rates determined by either $V_{\text{IH(AC)}}$ to $V_{\text{IL(AC)}}$ or $V_{\text{IH(DC)}}$ to $V_{\text{IL(DC)}}$, similarly for rising transitions.
- These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

- An I/O Delta Rise, Fall Derating table is used to increase t_{DS} and t_{DH} in the case where DQ, DM, and DQS slew rates differ.

Delta Rise and Fall Rate	Delta (t_{DS})	Delta (t_{DH})	Unit	Note
0.0 ns/V	0	0	ps	1-4
0.25 ns/V	+50	+50	ps	1-4
0.5 ns/V	+100	+100	ps	1-4

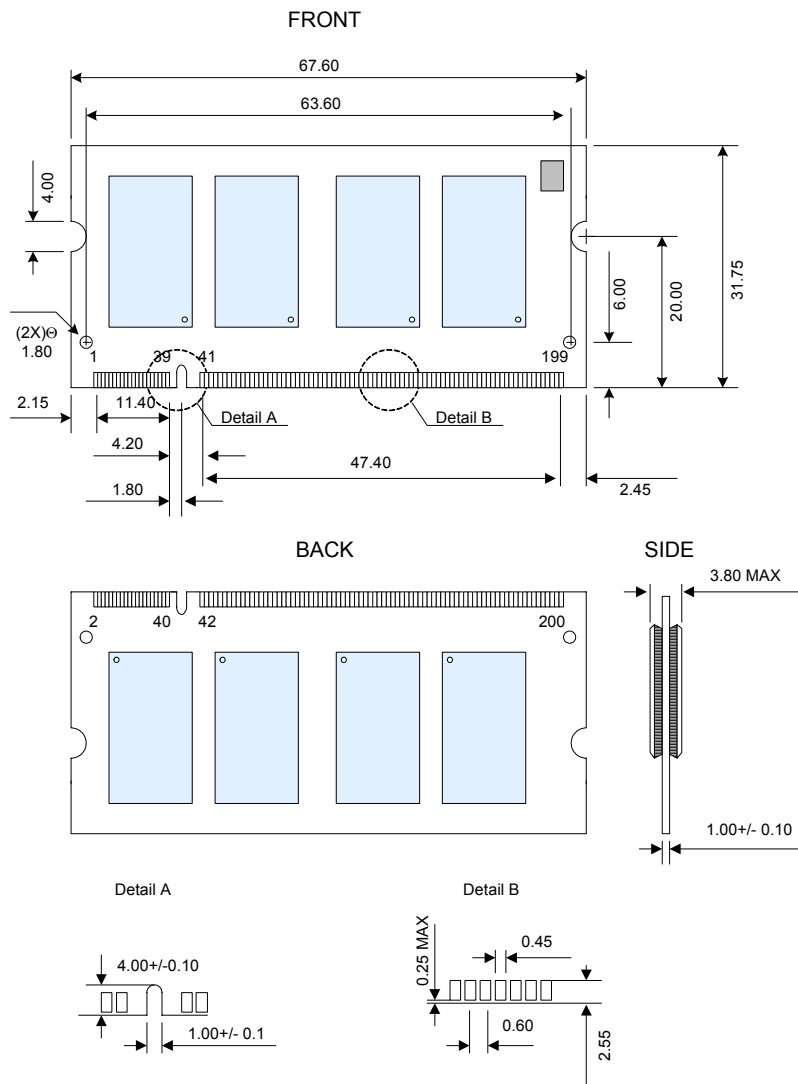
- Input slew rate is based on the lesser of the slew rates determined by either $V_{\text{IH(AC)}}$ to $V_{\text{IL(AC)}}$ or $V_{\text{IH(DC)}}$ to $V_{\text{IL(DC)}}$, similarly for rising transitions.
- Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
- The delta rise, fall rate is calculated as: $[1/(\text{slew rate 1})] - [1/(\text{slew rate 2})]$
For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns. Delta rise, fall = $(1/0.5) - (1/0.4)$ [ns/V] = -0.5 ns/V
Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
- These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

M1S25664DSH8C1G / M1S12864DSH4C1G
M1N25664DSH8C1G (GREEN)
Unbuffered DDR SO-DIMM



Package Dimensions

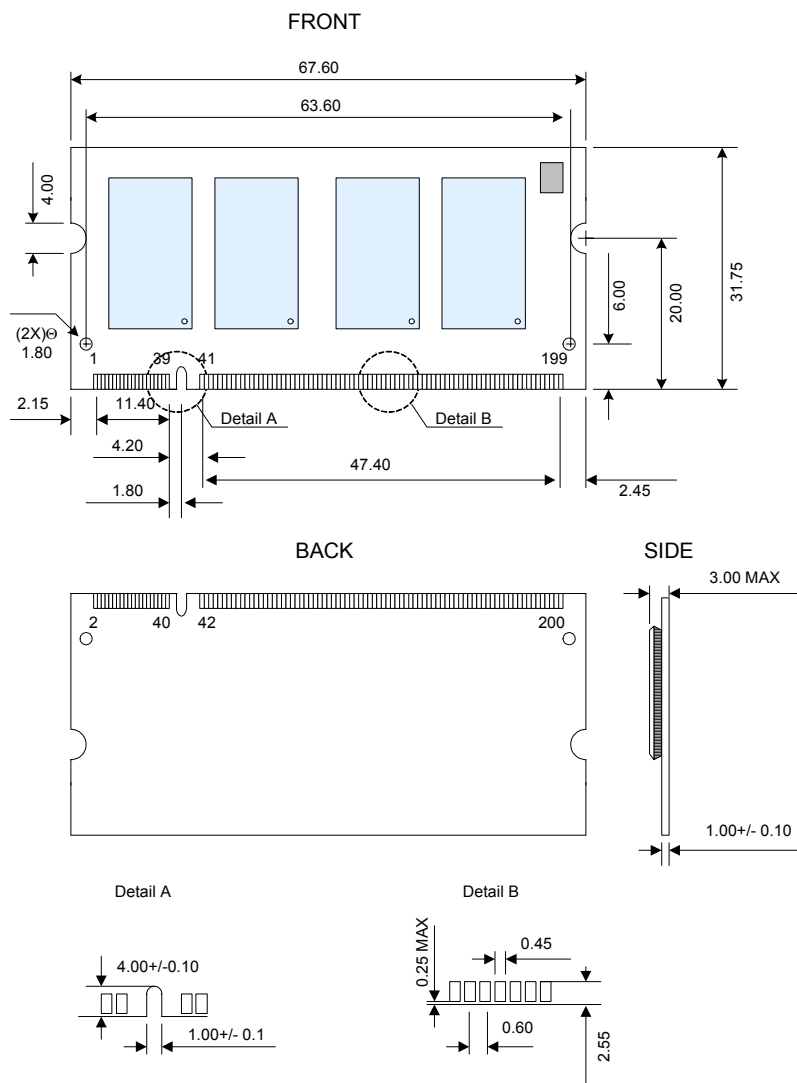
256MB, 8 TSOP devices



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.
 Units: Millimeters (Inches)

Package Dimensions

128MB, 4 TSOP devices



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

M1S25664DSH8C1G / M1S12864DSH4C1G
M1N25664DSH8C1G (GREEN)
Unbuffered DDR SO-DIMM



Revision Log

Rev	Date	Modification
0.1	April 8, 2004	Release
0.2	April 16, 2004	Speed grade update
0.3	June 1, 2005	Add green part number
1.0	July 19, 2005	Official Release for Super Elixir

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