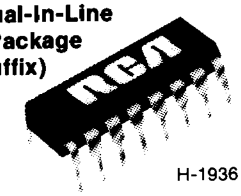
RCA Solid State

# CA3338, CA3338A

## Linear Integrated Circuits

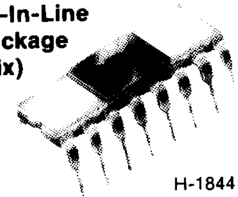
**Advance Information/ Preliminary Data**

**16-Lead Dual-In-Line Plastic Package (E Suffix)**



H-1936

**16-Lead Dual-In-Line Ceramic Package (D Suffix)**



H-1844

# CMOS Video-Speed 8-Bit R-2R Digital-to-Analog Converter

For Use in Low-Power Consumption, High-Speed Applications

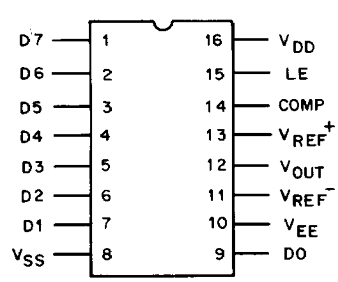
**Features:**
- *CMOS/SOS low power*
- *R-2R output, segmented for low "glitch"*
- *CMOS or TTL compatible inputs*
- *Fast settling: 20 ns (typ.) to ½ LSB*
- *Feedthrough latch for clocked or unclocked use*
- *Single or dual supplies, 4.5 to 7.5 V total*
- *½ LSB accuracy (typ.)*
- *Data complement control*
- *High update rate: 50 MHz (typ.)*
- *Unipolar or bipolar operation*

The RCA-CA3338 family are CMOS/SOS high-speed R-2R voltage output digital-to-analog converters. They operate from a single 5 volt supply at video speeds, and can produce "rail-to-rail" output swings. Internal level shifters and a pin for an optional second supply provide for an output range below the digital ground. The data complement control allows the inversion of input data while the latch enable control provides either feed-through or latched operation. Both ends of the R-2R ladder network are available externally and may be modulated for gain or offset adjustments. In addition, "glitch" energy has been kept very low by segmenting and "bar graph" decoding of the upper 3 bits.

The CA3338 is manufactured on a sapphire substrate to give low dynamic power dissipation, low output capacitance, and inherent latch-up resistance.

The CA3338 is available in a 16-lead dual-in-line plastic package (E suffix), in a 16-lead dual-in-line welded-seal ceramic package (D suffix), and in 1 LSB or 3/4 LSB (A suffix) integral linearity grades.

**Applications:**
- *TV/video display*
- *High-speed oscilloscope display*
- *Digital waveform generator*
- *Feed-forward A/D systems*




92CS-40442

**TERMINAL ASSIGNMENT**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE
($V_{DD}$-$V_{SS}$ or $V_{DD}$-$V_{EE}$, whichever is greater) ........ -0.5 to +8 V
INPUT VOLTAGE RANGE
DIGITAL INPUTS (LE, COMP, D0 - D7) ........ $V_{SS}$ -0.5 to $V_{DD}$ +0.5 V
ANALOG PINS ($V_{REF}^+$, $V_{REF}^-$, $V_{OUT}$) ........ $V_{DD}$ -8 to $V_{DD}$ +0.5 V
DC INPUT CURRENT
DIGITAL INPUTS (LE, COMP, D0 - D7) ........ ±20 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
FOR $T_A$ = -55°C to +55°C ........ 315 mW
FOR $T_A$ = +55°C to +125°C ........ Derate Linearly at 3.3 mW/°C
OPERATING-TEMPERATURE RANGE ($T_A$):
CERAMIC PACKAGE - D SUFFIX ........ -55 to +125°C
PLASTIC PACKAGE - E SUFFIX ........ -40 to +85°C
STORAGE-TEMPERATURE RANGE ($T_{stg}$) ........ -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ........ +265°C
RECOMMENDED SUPPLY VOLTAGE RANGE ........ 4.5 to 7.5 V

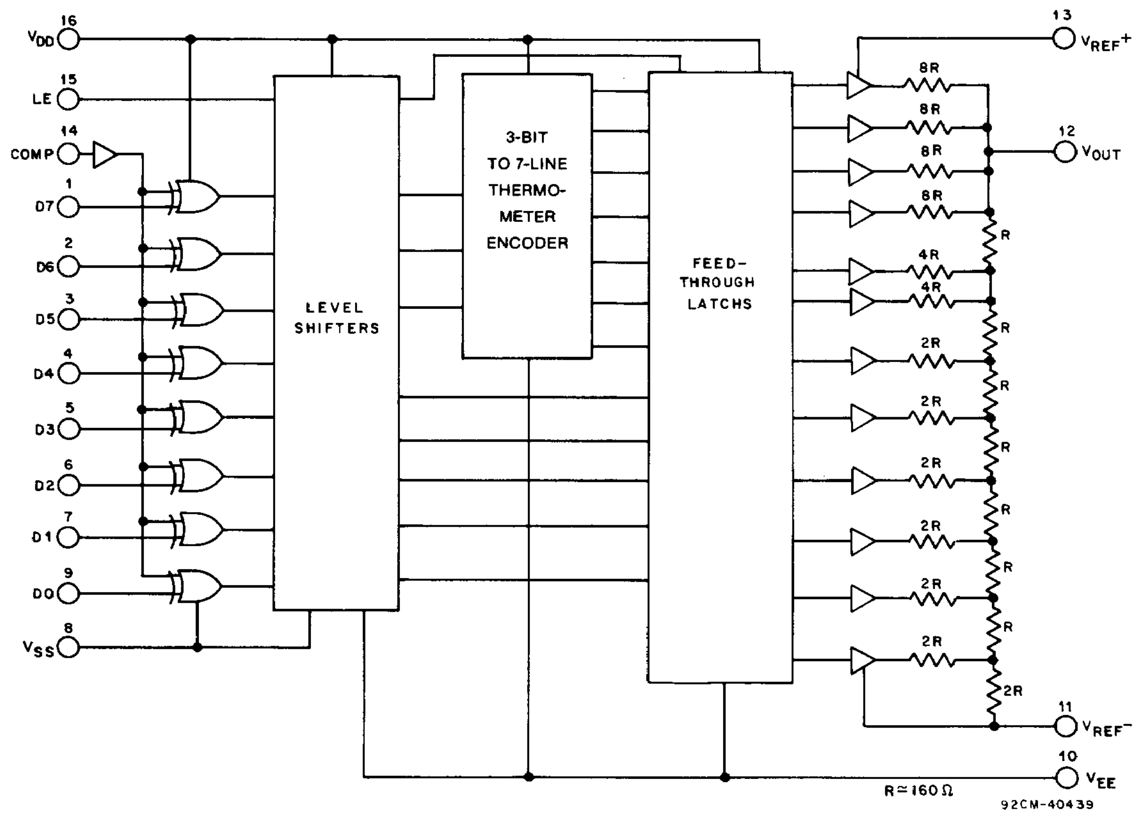



*Fig. 1 - Block diagram for the CA3338.*

**ELECTRICAL CHARACTERISTICS FOR CA3338 AND CA3338A AT $T_A$ = 25°C, $V_{DD}$ = 5 V ± 5%, $V_{REF}^+$ = 4.608 V, $V_{SS}$ = $V_{EE}$ = $V_{REF}^-$ = GND, LE CLOCKED AT 20 MHz, $R_L$ ≥ 1 M OHM (UNLESS OTHERWISE SPECIFIED)**

| CHARACTERISTIC | TEST CONDITIONS/COMMENTS | LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| Accuracy | | | | | |
| Resolution | | — | — | 8 | Bits |
| Integral Linearity Error | See Figure 5 | | | | |
| CA3338 | | — | — | 1 | LSB |
| CA3338A | | — | — | 3/4 | LSB |
| Differential Linearity Error | See Figure 5 | | | | |
| CA3338 | | — | — | 3/4 | LSB |
| CA3338A | | — | — | 1/2 | LSB |
| Gain Error | Input Code = $FF_{16}$; See Fig. 4 | | | | |
| CA3338 | | — | — | 3/4 | LSB |
| CA3338A | | — | — | 1/2 | |
| Offset Error | Input Code = $00_{16}$; See Fig. 4 | — | — | 1/4 | LSB |
| Digital Input Timing | | | | | |
| Update Rate | To Maintain 1/2 LSB Settling | DC | 50 | TBE | MHz |
| Update Rate | $V_{REF}^-$ = $V_{EE}$ = -2.5 V, $V_{REF}^+$ = +2.5 V | DC | 20 | TBE | MHz |
| Set up Time $T_{SU1}$ | For Low Glitch | TBE | -2 | — | nSEC |
| Set up Time $T_{SU2}$ | For Data Store | TBE | 8 | — | nSEC |
| Hold Time $T_H$ | For Data Store | TBE | 5 | — | nSEC |
| Latch Pulse Width $T_W$ | For Data Store | TBE | 5 | — | nSEC |
| Latch Pulse Width $T_W$ | $V_{REF}^-$ = $V_{EE}$ = -2.5 V, $V_{REF}^+$ = +2.5 V | TBE | 25 | — | nSEC |
| Output Parameters | $R_L$ Adjusted for 1 Vp-p Output | | | | |
| Output Delay $T_{D1}$ | From LE Edge | — | 25 | TBE | nSEC |
| Output Delay $T_{D2}$ | From Data Changing | — | 22 | TBE | nSEC |
| Rise Time $T_R$ | 10 to 90% of Output | — | 4 | TBE | nSEC |
| Settling Time $T_S$ | 10% to Settling to 1/2 LSB | — | 20 | TBE | nSEC |
| Output Impedance | | 120 | 160 | 200 | Ohms |
| Glitch Energy | | — | 150 | TBE | PV - SEC |
| Glitch Energy | $V_{REF}^-$ = $V_{EE}$ = -2.5 V, $V_{REF}^+$ = +2.5 V | — | 250 | TBE | PV - SEC |
| Reference Voltage | | | | | |
| $V_{REF}^+$ Range | (+) Full Scale | $V_{REF}$- +3 | — | $V_{DD}$ | Volts |
| $V_{REF}^-$ Range | (-) Full Scale | $V_{EE}$ | — | $V_{REF}$+ -3 | Volts |
| $V_{REF}^+$ Input Current | Input Code = $55_{16}$ | — | 20 | — | mA |
| Supply Voltage | | | | | |
| Static $I_{DD}$ or $I_{EE}$ | LE Low | — | 1 | — | μA |
| Dynamic $I_{DD}$ or $I_{EE}$ | $V_{OUT}$ = 10 MHz, 0 to 5 V Sq. Wave | — | 20 | — | mA |
| Dynamic $I_{DD}$ or $I_{EE}$ | $V_{OUT}$ = 10 MHz, ±2.5 V Sq. Wave | — | 25 | — | mA |
| $V_{DD}$ Rejection | 50 kHz Sine Wave Applied | — | 3 | — | mV/V |
| $V_{EE}$ Rejection | 50 kHz Sine Wave Applied | — | 1 | — | mV/V |
| Digital Inputs | D0 - D7, LE, COMP | | | | |
| High Level Input Voltage | | 2 | — | — | Volts |
| Low Level Input Voltage | | — | — | 0.8 | Volts |
| Leakage Current | | — | 1 | — | μA |
| Capacitance | | — | 5 | — | pF |
| Temperature Coefficients | | | | | |
| Gain Error | | — | TBE | — | μV/°C |
| Offset Error | | — | TBE | — | μV/°C |
| Output Impedance | | — | 200 | — | PPM/°C |

## DIGITAL SIGNAL PATH

The digital inputs (LE, COMP, and D0 - D7) are of TTL compatible RCA HCT High Speed CMOS design: the loading is essentially capacitive and the logic threshold is typically 1.5 V.

The 8 data bits, D0 (weighted $2^0$) through D7 (weighted $2^7$), are applied to Exclusive OR gates (see figure 1). The COMP (data complement) control provides the second input to the gates: if COMP is high, the data bits will be inverted as they pass through.

The input data and the LE (latch enable) signals are next applied to a level shifter. The inputs, operating between the levels of $V_{DD}$ and $V_{SS}$, are shifted to operate between $V_{DD}$ and $V_{EE}$. $V_{EE}$, optionally at ground or at a negative voltage, will be discussed under bipolar operation. All further logic elements except the output drivers operate from the $V_{DD}$ and $V_{EE}$ supplies.

The upper 3 bits of data, D5 through D7, are input to a 3-to-7 line bar graph encoder. The encoder outputs and D0 through D4 are applied to a feedthrough latch, which is controlled by LE (latch enable).

## OUTPUT STRUCTURE

The latches feed data to a row of high current CMOS drivers, which in turn feed a modified R-2R ladder network.

The "N" channel (pull down) transistor of each driver plus the bottom "2R" resistor are returned to $V_{REF}^-$; this is the (-) full-scale reference. The "P" channel (pull up) transistor of each driver is returned to $V_{REF}^+$, the (+) full-scale reference.

In unipolar operation, $V_{REF}^-$ would typically be returned to analog ground, but may be raised above ground (see specifications). There is substantial code dependent current that flows from $V_{REF}^+$ to $V_{REF}^-$ (see $V_{REF}^+$ input current in specifications), so $V_{REF}^-$ should have a low impedance path to ground.

In bipolar operation, $V_{REF}^-$ would be returned to a negative voltage (the maximum voltage rating to $V_{DD}$ must be observed). $V_{EE}$, which supplies the gate potential for the output drivers, must be returned to a point at least as negative as $V_{REF}^-$. Note that the maximum clocking speed decreases when the bipolar mode is used.

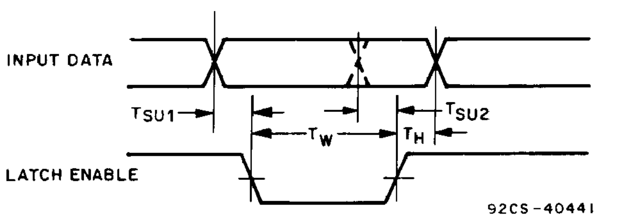



*Fig. 2 - Data to latch enable timing.*

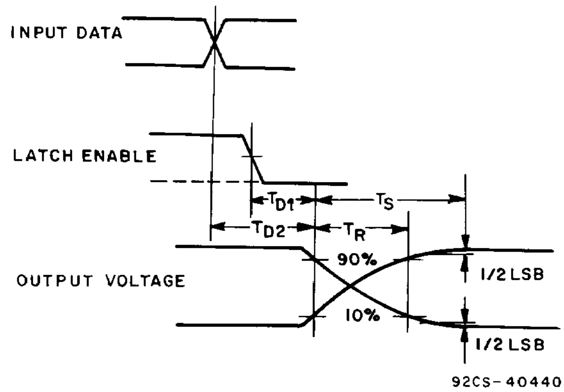



*Fig. 3 - Data and latch enable to output timing.*

## LATCH OPERATION

Data is fed from input to output while LE is low: LE should be tied low for non-clocked operation.

Non-clocked operation or changing data while LE is low is not recommended for applications requiring low output "glitch" energy: there is no guarantee of the simultaneous changing of input data or the equal propagation delay of all bits through the converter. Several parameters are given if the converter is to be used in either of these modes: $T_{D2}$ gives the delay from the input changing to the output changing (10%), while $t_{SU2}$ and $T_H$ give the set-up and hold times (referred to LE rising edge) needed to latch data. See figures 2 and 3.

Clocked operation is needed for low "glitch" energy use. Data must meet the given $T_{SU1}$ set-up time to the LE falling edge, and the $T_H$ hold time from the LE rising edge. The delay to the output changing, $T_{D1}$, is now referred to the LE falling edge.

There is no need for a square wave LE clock; LE must only meet the minimum TW pulse width for successful latch operation. Generally, output timing (desired accuracy of settling) sets the upper limit of usable clock frequency.

## STATIC CHARACTERISTICS

The ideal 8-bit D/A would have an output equal to $V_{REF}^-$ with an input code of $00_{16}$ (zero scale output), and an output equal to 255/256 of $V_{REF}^+$ (referred to $V_{REF}^-$) with an input code of $FF_{16}$ (full-scale output). The difference between the ideal and actual values of these two parameters are the OFFSET and GAIN errors respectively: see figure 4.

If the code into an 8-bit D/A is changed by 1 count, the output should change by 1/255 (full-scale output - zero-scale output). A deviation from this step-size is a differential linearity error: see figure 5. Note that the error is expressed in fractions of the ideal step size (usually called an LSB). Also note that if the (-) differential linearity error is less (in absolute numbers) than 1 LSB, the device is monotonic. (The output will always increase for increasing code or decrease for decreasing code).

If the code into an 8-bit D/A is at any value, say "N", the output voltage should be N/255 of the full-scale output (referred to the zero-scale output). Any deviation from that output is an integral linearity error, usually expressed in LSB's. See figure 5.

Note that OFFSET and GAIN errors do not affect integral linearity, as the linearity is referenced to actual zero and full-scale outputs, not ideal. Absolute accuracy would have to also take these errors into account.

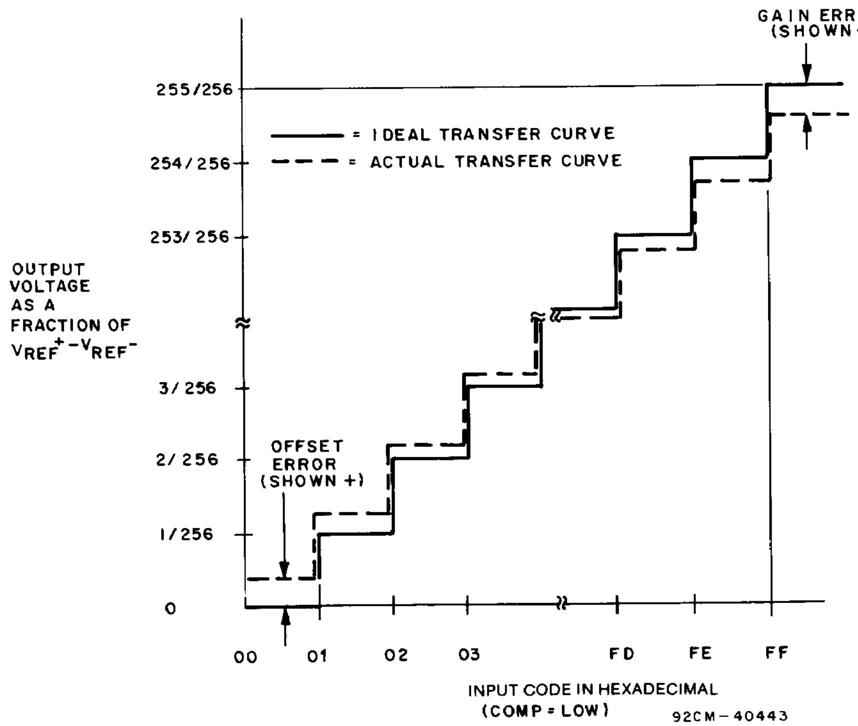



*Fig. 4 - D/A offset and gain error.*

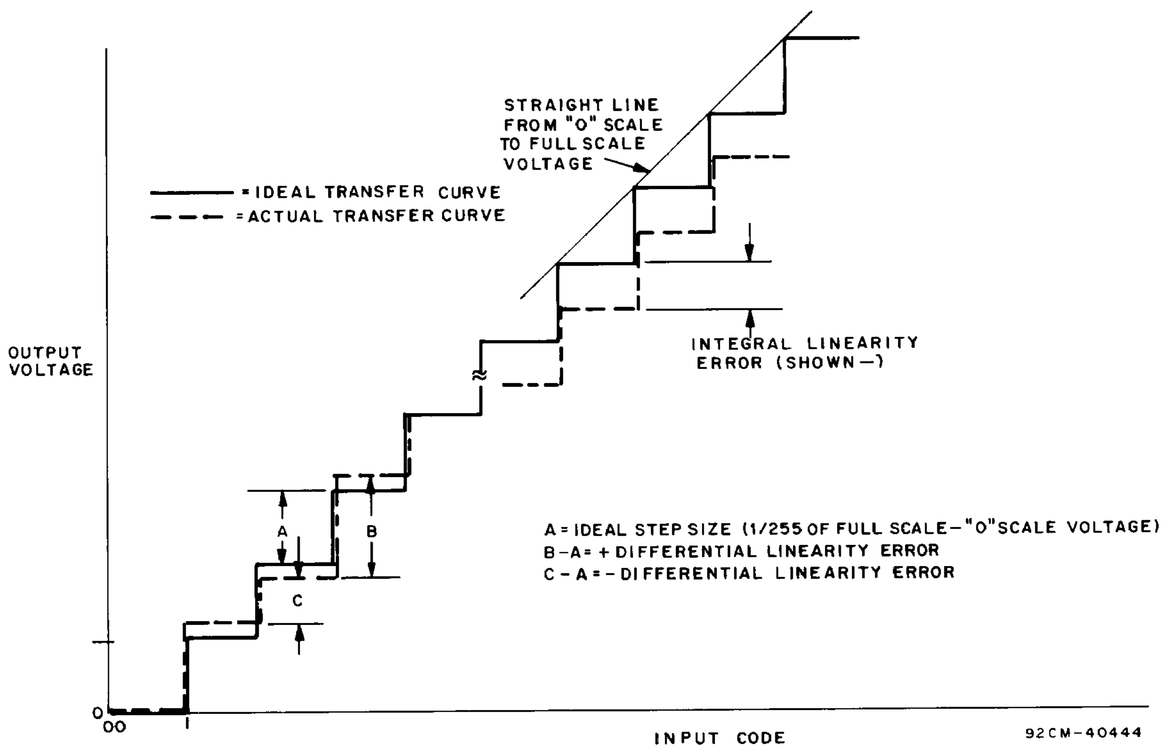



*Fig. 5 - D/A integral and differential linearity error.*

## DYNAMIC CHARACTERISTICS

Keeping the full-scale range ($V_{REF}^+$ - $V_{REF}^-$) as high as possible gives the best linearity and lowest "glitch" energy (referred to 1 volt). This provides the best "P" and "N" channel gate drives (hence saturation resistance) and propagation delays. The $V_{REF}^+$ (and $V_{REF}^-$ if bipolar) terminal should be well bypassed as near the chip as possible.

"Glitch" energy is defined as a spurious voltage that occurs as the output is changed from one voltage to another. In a binary input converter, it is usually highest at the most significant bit transition ($7F_{16}$ to $80_{16}$ for an 8 bit device), and can be measured by displaying the output as the input code alternates around that point. The "glitch" energy is the area between the actual output display and an ideal one LSB step voltage (subtracting negative area from positive), at either the positive or negative-going step. It is usually expressed in pico-volt seconds.

The CA3338 uses a modified R-2R ladder, where the 3 most significant bits drive a bar-graph decoder and 7 equally weighted resistors. This makes the "glitch" energy at each 1/8 scale transition ($1F_{16}$ to $20_{16}$, $3F_{16}$ to $40_{16}$, etc.) essentially equal, and far less than the MSB transition would otherwise display.

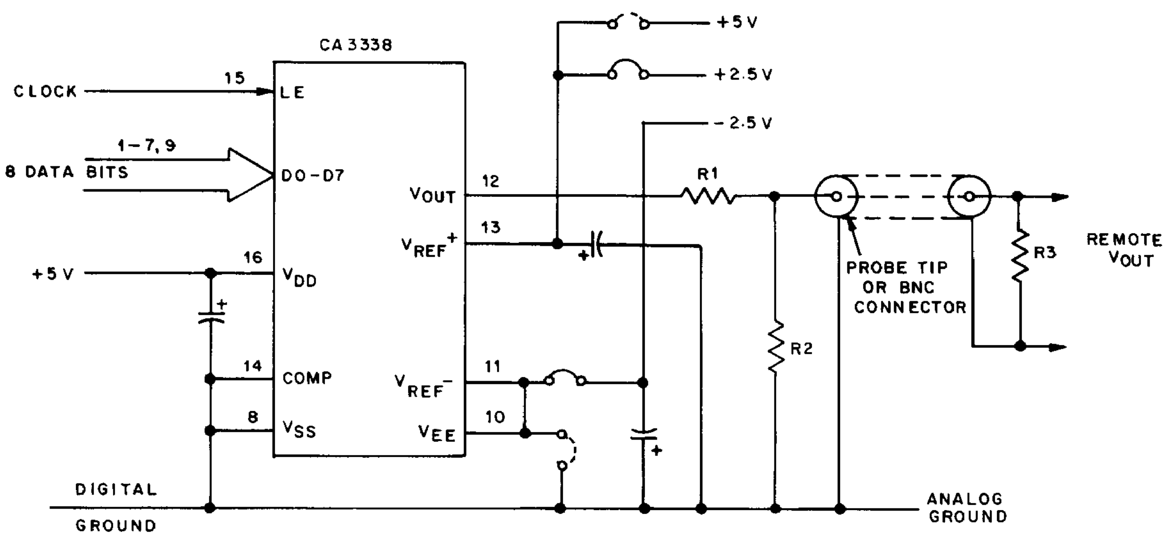
For the purpose of comparison to other converters, the output should be resistively divided to 1 volt full-scale. Figure 6 shows a typical hook-up for checking "glitch" energy or settling time.

The settling time of the A/D is mainly a function of the output resistance (approximately 160 ohms in parallel with the load resistance) and the load plus internal chip capacitance. Both "glitch" energy and settling time measurements require very good circuit and probe grounding: a probe tip connector such as Tektronix part number 131-0258-00 is recommended.

## APPLICATIONS:

The output of the CA3338 can be resistively divided to match a doubly-terminated 50 or 75 ohm line, although peak-to-peak swings of less than 1 volt may result. The output magnitude will also vary with the converter's output impedance. Figure 6 shows such an application. Note that because of the HCT input structure, the CA3338 could be operated up to +7.5 volt $V_{DD}$ and $V_{REF}^+$ supplies and still accept 0 to 5 volt CMOS input voltages.

If larger voltage swings or better accuracy is desired, a high speed output buffer, such as the CA3450, can be employed. Figure 7 shows a typical application, with the output capable of driving ±2 volts into multiple 50 ohm terminated lines.

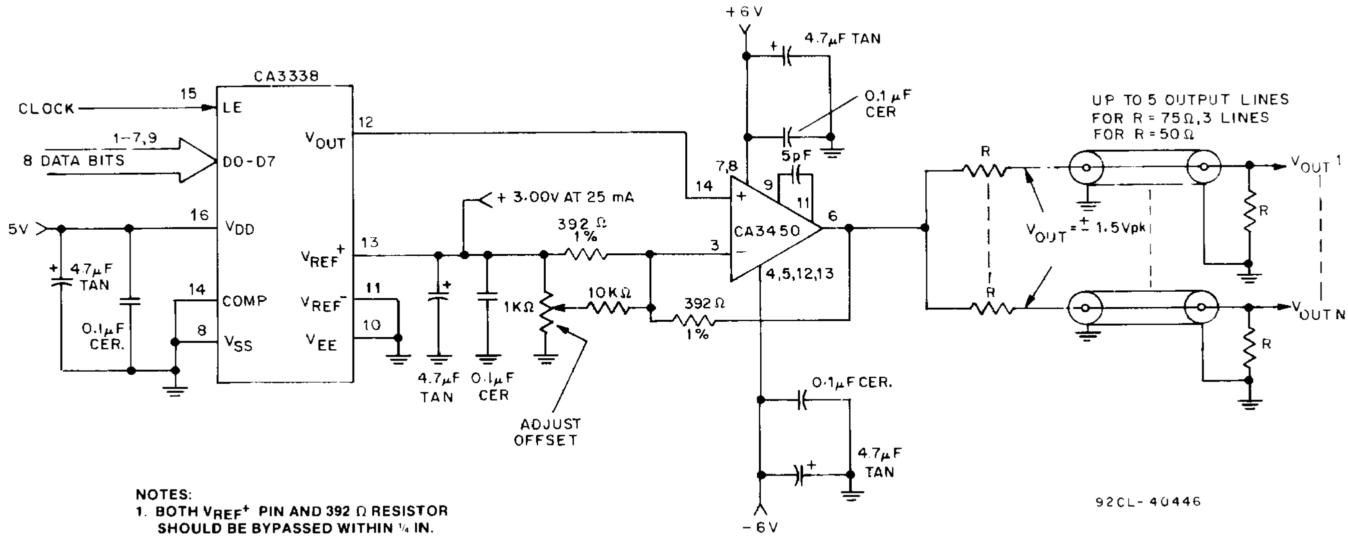



| FUNCTION: | CONNECTOR | R1 | R2 | R3 | $V_{OUT}$ (PK-PK) |
|---|---|---|---|---|---|
| OSCILLOSCOPE DISPLAY | PROBE TIP | 82 Ω | 62 Ω | N/C | 1 V |
| MATCH 93-OHM CABLE | BNC | 75 | 160 | 93 | 1 V |
| MATCH 75-OHM CABLE | BNC | 18 | 130 | 75 | 1 V |
| MATCH 50-OHM CABLE | BNC | SHORT | 75 | 50 | 0.79 V |

NOTES:
1. $V_{OUT}$(PK) IS APPROXIMATE, AND WILL VARY AS $R_{OUT}$ OF D/A VARIES.
2. ALL DRAWN CAPACITORS ARE 0.1 μF MULTILAYER CERAMIC//4.7 μF TANTALUM.
3. DASHED CONNECTIONS ARE FOR UNIPOLAR OPERATION, SOLID FOR BIPOLAR.

92CM-40445

*Fig. 6 - CA3338 dynamic test circuit.*




NOTES:
1. BOTH $V_{REF}^+$ PIN AND 392 Ω RESISTOR SHOULD BE BYPASSED WITHIN ¼ IN.
2. KEEP NODAL CAPACITANCE AT CA3450 PIN 3 AS LOW AS POSSIBLE.
3. $V_{OUT}$ RANGE ±3 V AT CA3450.

*Fig. 7 - CA3338 and CA3450 for driving multiple coaxial lines.*

## TABLE I: OUTPUT VOLTAGE VS INPUT CODE AND $V_{REF}$

| $V_{REF}+$<br>$V_{REF}-$<br>**STEP SIZE** | **5.12 V**<br>**0**<br>**0.0200 V** | **5.00 V**<br>**0**<br>**0.0195 V** | **4.608 V**<br>**0**<br>**0.0180 V** | **2.56 V**<br>**-2.56 V**<br>**0.0200 V** | **2.50 V**<br>**-2.50 V**<br>**0.0195 V** |
|---|---|---|---|---|---|
| INPUT CODE | | | | | |
| $1111\ 1111_2 = FF_{16}$ | 5.1000 V | 4.9805 V | 4.5900 V | 2.5400 V | 2.4805 V |
| $1111\ 1110_2 = FE_{16}$ | 5.0800 | 4.9610 | 4.5720 | 2.5200 | 2.4610 |
| • | | | | | |
| • | | | | | |
| • | | | | | |
| $1000\ 0001_2 = 81_{16}$ | 2.5800 | 2.5195 | 2.3220 | 0.0200 | 0.0195 |
| $1000\ 0000_2 = 80_{16}$ | 2.5600 | 2.5000 | 2.3040 | 0.0000 | 0.0000 |
| $0111\ 1111_2 = 7F_{16}$ | 2.5400 | 2.4805 | 2.2860 | -0.0200 | -0.0195 |
| • | | | | | |
| • | | | | | |
| • | | | | | |
| $0000\ 0001_2 = 01_{16}$ | 0.0200 | 0.0195 | 0.0180 | -2.5400 | -2.4805 |
| $0000\ 0000_2 = 00_{16}$ | 0.0000 | 0.0000 | 0.0000 | -2.5200 | -2.5000 |

## ORDERING INFORMATION

| **Package** | **Integral Linearity** | |
|---|---|---|
| | **1 LSB** | **3/4 LSB** |
| Ceramic | CA3338D | CA3338AD |
| Plastic | CA3338E | CA3338AE |

## OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

**Operating Voltage**

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the absolute maximum ratings to be exceeded.

**Input Signals**

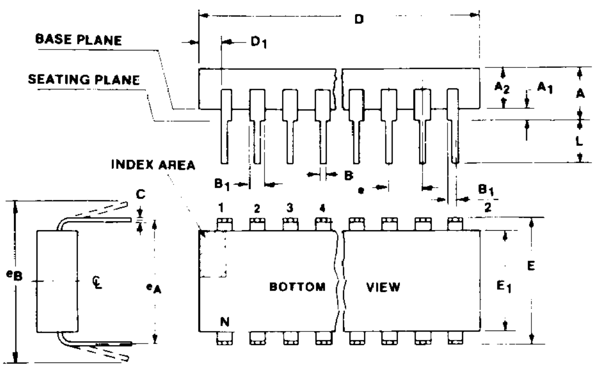
To prevent damage to the input protection circuit, input signals should never be greater than $V_{DD}$ nor less than $V_{SS}$. Input currents must not exceed 20 mA even when the power supply is off.

**Unused Inputs**

A connection must be provided at every input terminal. All unused input terminals must be connected to either $V_{CC}$ or Gnd, whichever is appropriate.

## DIMENSIONAL OUTLINES

**(E) Suffix (JEDEC MS-001-AA)**
**16-Lead Dual-In-Line Plastic Package**




| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | — | 0.210 | — | 5.33 | 9 |
| $A_1$ | 0.015 | — | 0.39 | — | 9 |
| $A_2$ | 0.115 | 0.195 | 2.93 | 4.95 | |
| B | 0.014 | 0.022 | 0.356 | 0.558 | |
| $B_1$ | 0.045 | 0.070 | 1.15 | 1.77 | 3 |
| C | 0.008 | 0.015 | 0.204 | 0.381 | |
| D | 0.745 | 0.840 | 18.93 | 21.33 | 4 |
| $D_1$ | 0.005 | — | 0.13 | — | 12 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 5 |
| $E_1$ | 0.240 | 0.280 | 6.10 | 7.11 | 6, 7 |
| e | 0.100 BSC | | 2.54 BSC | | 8 |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 9 |
| $e_B$ | — | 0.430 | — | 10.92 | 10 |
| L | 0.115 | 0.160 | 2.93 | 4.06 | 9 |
| N | 16 | | 16 | | 11 |

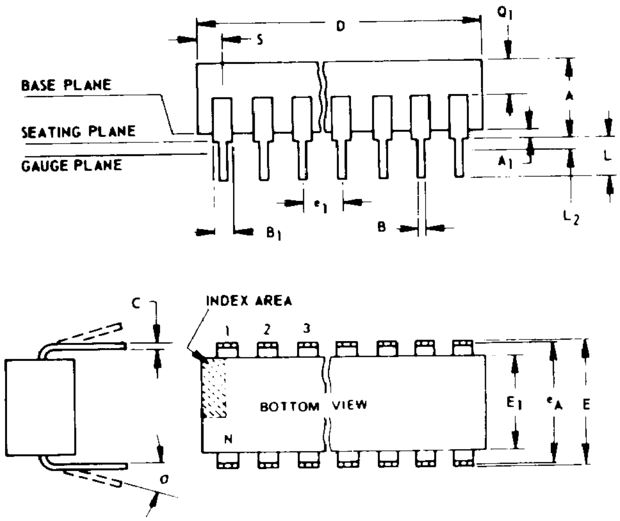
92CS-39900

**Notes:**

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions $1, N, \frac{N}{2}, \frac{N}{2}+1$.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension $E_1$ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension $e_A$.
10. $e_B$ is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension $D_1$ at the left end of the package must equal dimension $D_1$ at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

## DIMENSIONAL OUTLINES (Continued)

**(D) Suffix**
**16-Lead Dual-In-Line Welded-Seal Package**




| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 0.120 | 0.160 | 3.05 | 4.06 | |
| $A_1$ | 0.020 | 0.065 | 0.51 | 1.65 | |
| B | 0.014 | 0.020 | 0.356 | 0.508 | |
| $B_1$ | 0.050 | 0.065 | 1.27 | 1.65 | |
| C | 0.008 | 0.012 | 0.204 | 0.304 | 1 |
| D | 0.745 | 0.840 | 18.93 | 21.33 | |
| E | 0.300 | 0.325 | 7.62 | 8.25 | |
| $E_1$ | 0.240 | 0.260 | 6.10 | 6.60 | |
| $e_1$ | 0.100 TP | | 2.54 TP | | 2 |
| $e_A$ | 0.300 TP | | 7.62 TP | | 2, 3 |
| L | 0.125 | 0.150 | 3.18 | 3.81 | |
| $L_2$ | 0.000 | 0.030 | 0.000 | 0.76 | |
| $\alpha$ | 0° | 15° | 0° | 15° | 4 |
| N | 16 | | 16 | | 5 |
| $N_1$ | 0 | | 0 | | 6 |
| $Q_1$ | 0.050 | 0.085 | 1.27 | 2.15 | |
| S | 0.065 | 0.090 | 1.66 | 2.28 | |

92CS-40078

**NOTES:**

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. $e_A$ applies in zone $L_2$ when unit installed.
4. $\alpha$ applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. $N_1$ is the quantity of allowable missing leads.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices," Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.