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Status	Product Specification
ECL Products	

100984

Quad ECL–TTL Translating Transceiver with Registers

FEATURES

- **Typical propagation delay from clock to output: 3.5ns**
- **Typical ECL supply current (–IECL): 110mA**
- **Typical TTL supply current (ITTL): 25mA**
- **Low logic level of ECL output doubles as a high impedance state**
- **ECL output drives 25 Ohm loads**
- **4,000 Volt ESD protection for all pins**
- **Controlled edge rates for quieter bus operation**

DESCRIPTION

The 100984 is a four–bit, translating transceiver with registers. It allows the exchange of data between a 100K ECL bus and a TTL bus. The A data lines are 100K ECL–compatible and bidirectional. The B data lines are TTL–compatible and unidirectional (BI for input, BO for output). The control lines are 100K ECL–compatible.

There are three basic modes of operation for the device: When data flows from A to BO, an ECL–to–TTL translation occurs. When data flows from BI to A, a TTL–to–ECL translation occurs. Finally, A can be disconnected from B, preventing any data exchange between the ECL and TTL buses.

The 100984 has two storage registers, one for each direction of data flow (A to BO, BI to A). Data is stored on the rising edge of the clock pulse (CPAB, CPBA), provided that the clock enable ($\overline{CEAB}$, $\overline{CEBA}$) is Low.

Each 100K ECL output (A side) can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V). When an ECL output goes Low, its emitter–follower turns off. As a result, the Low logic level approaches the termination voltage (–2.0V) and represents a high impedance state. A High on the ECL output enable ($\overline{OEBA}$) will also cut off the emitter–follower, producing the same high impedance state.

The TTL outputs (BO) have three–state capability. A High on the TTL output enable ($\overline{OEAB}$) will put the TTL outputs into a high impedance state.

Power may be applied to the VECL and VTTL pins in any order.

All unused inputs can be left open due to integrated pull–down resistors.

ORDERING INFORMATION

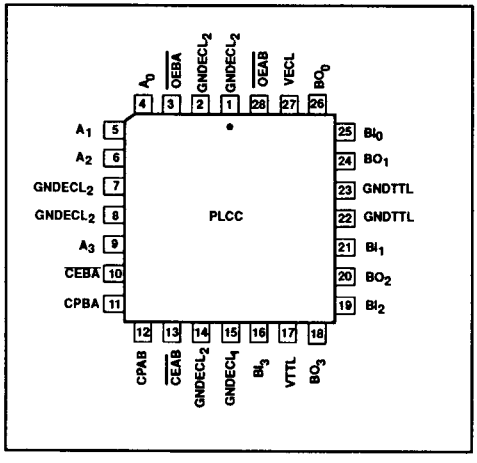
DESCRIPTION	ORDER CODE
28–Pin PLCC	100984A

Translating Transceiver 100984

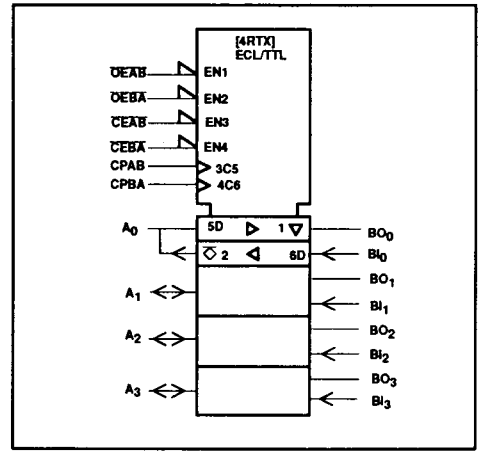
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_3$	Bidirectional data lines (100K ECL compatible)
$BI_0 - BI_3$	Data inputs (TTL compatible)
$BO_0 - BO_3$	Data outputs (TTL compatible)
$\overline{OEAB}$	BO output enable (100K ECL compatible)
$\overline{OEBA}$	A output enable (100K ECL compatible)
CPAB	Clock pulse input for A–to–BO data flow (100K ECL compatible)
CPBA	Clock pulse input for BI–to–A data flow (100K ECL compatible)
$\overline{CEAB}$	Clock enable input for A–to–BO data flow (100K ECL compatible)
$\overline{CEBA}$	Clock enable input for BI–to–A data flow (100K ECL compatible)
VECL	ECL supply voltage
VTTL	TTL supply voltage
$GNDECL_1$	Ground for ECL internal logic and reference generator
$GNDECL_2$	Ground for ECL outputs
GNDTTL	TTL ground

PIN CONFIGURATION

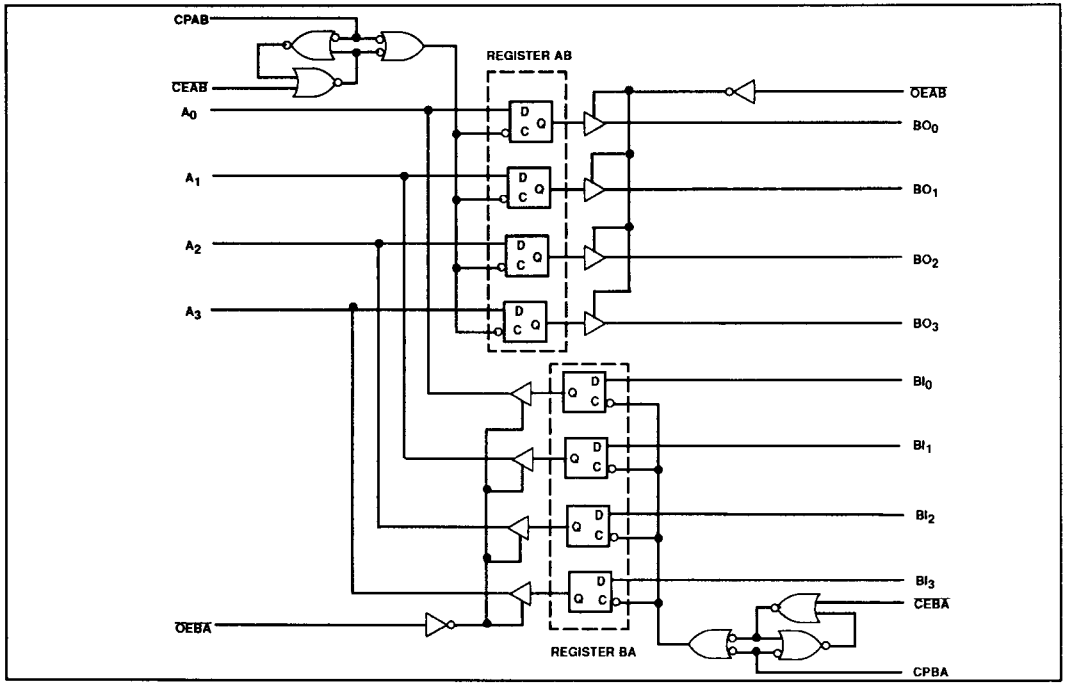


IEC/IEEE SYMBOL



Translating Transceiver 100984

LOGIC DIAGRAM



NOTE:
Pins BI_0 through BI_3 and BO_0 through BO_3 are TTL–compatible. Pins CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$, and A_0 through A_3 are ECL–compatible.

FUNCTION TABLE

ENABLES		CLOCK	INPUT	REGISTER	OUTPUT	OPERATING MODE
$\overline{OEAB}$	$\overline{CEAB}$	CPAB	A_n	AB	BO_n	A–TO–BO DATA PATH (ECL–TO–TTL TRANSLATION)
$\overline{OEBA}$	$\overline{CEBA}$	CPBA	BI_n	BA	A_n	BI–TO–A DATA PATH (TTL–TO–ECL TRANSLATION)
L	L	↑	L	L	L	Load data into register and present at outputs
L	L	↑	H	H	H	
L	L	↕	X	L	L	Hold data in register and present at outputs
L	L	↕	X	H	H	
L	H	X	X	L	L	
L	H	X	X	H	H	
H	L	↑	L	L	Z	Load data in register with outputs in high impedance state
H	L	↑	H	H	Z	
H	L	↕	X	NC	Z	Hold data in register with outputs in high impedance state
H	H	X	X	NC	Z	

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
NC = No change
Z = High impedance state
↑ = Low–to–High transition
↕ = No Low–to–High transition

Any combination of A–to–B and B–to–A operations may be carried out concurrently, provided that no signal is driven into an active (enabled) output.

ABSOLUTE MAXIMUM RATINGS FOR ECL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground

T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
VECL	ECL supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than VECL)	VECL to +0.5	V
I_O	Output source current (continuous)	–100	mA

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

ABSOLUTE MAXIMUM RATINGS FOR TTL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground,

T_A =0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
VTTL	TTL supply voltage range	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to VTTL	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High state	–0.5 to VTTL	V
I_{OUT}	Current applied to output in Low state	+96	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS FOR ECL–COMPATIBLE LINES

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
$GNDECL_1$	Ground for ECL internal logic and reference generator		0	0	0	V
$GNDECL_2$	Ground for ECL outputs		0	0	0	V
VECL	ECL supply voltage		–4.8	–4.5	–4.2	V
VECL	ECL supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	VECL = –4.2V	–1150		–880	mV
		VECL = –4.5V	–1165			
		VECL = –4.8V	–1165			
V_{IL}	Low level input voltage	VECL = –4.2V	–1810		–1475	mV
		VECL = –4.5V			–1475	mV
		VECL = –4.8V			–1490	mV

NOTE:
When operating at other than the specified VECL voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC OPERATING CONDITIONS FOR TTL–COMPATIBLE LINES

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
GNDTTL	TTL ground	0	0	0	V
VTTL	TTL supply voltage	+4.5	+5.0	+5.5	V
V_{IH}	High level input voltage	+2.0			V
V_{IL}	Low level input voltage			+0.8	V
$-I_{OH}$	High level output current			15	mA
I_{OL}	Low level output current			48	mA
T_A	Operating ambient temperature range	0	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS FOR ECL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –4.8V to –4.2V, VTTL = +4.5V to +5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Store High state in register BA.	VECL = –4.2V	–1020		–870	mV
			A_n is tested with a 25Ω load terminated to V_T = –2.0V ± 0.010V.	VECL = –4.5V	–1025	–955	–880	mV
			$\overline{OEBA}$ at V_{ILMIN}.	VECL = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Store High state in register BA.	VECL = –4.2V	–1030			mV
			A_n is tested with a 25Ω load terminated to V_T = –2.0V ± 0.010V.	VECL = –4.5V	–1035			mV
			$\overline{OEBA}$ at V_{ILMAX}.	VECL = –4.8V	–1045			mV
I_{OZ}	Off–state output current[5]		Store High state in register BA. $\overline{OEBA}$ and $\overline{OEAB}$ at V_{IHMAX}. Apply –2.1V to A_n under test.				90	µA
I_{IH}	High level input current[5]	A_n	A_n under test at V_{IHMAX}, other A_n at V_{ILMIN}. $\overline{OEBA}$ at V_{IHMAX}.				120	µA
		$\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$, CPAB, CPBA	One control line under test at V_{IHMAX}, all other control lines at V_{ILMIN}, All BI_n at V_{ILMIN}. All A_n and BO_n open.				140	µA
I_{IL}	Low level input current[5]	A_n	A_n under test at V_{ILMIN}, other A_n at V_{IHMAX}. $\overline{OEBA}$ at V_{IHMAX}.		10			µA
		$\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$, CPAB, CPBA	One control line under test at V_{ILMIN}, all other control lines at V_{IHMAX}. All BI_n at V_{IHMAX}. All A_n and BO_n open.		10			µA
–IECL	ECL supply current		All A_n at V_{IHMAX}. $\overline{OEBA}$ at V_{IHMAX}.		64	110	150	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to VECL = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended VECL range. For more information, see Chapter 10, Section 4.
5. For bidirectional lines, this parameter includes currents due to output leakage and input pull–down resistors.

DC ELECTRICAL CHARACTERISTICS FOR TTL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –4.8V to –4.2V, VTTL = 4.5V to 5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Store High state in register AB. $\overline{OEAB}$ at V_{ILMIN}.	I_{OH} = –3mA	2.4			V
			I_{OH} = –15mA	2.0			V
V_{OL}	Low level output voltage	Store Low state in register AB. $\overline{OEAB}$ at V_{ILMIN}.	I_{OL} = +24mA		0.35	0.50	V
			I_{OL} = +48mA		0.40	0.55	V
V_{IK}	Input clamp voltage	Apply –18mA to BI_n under test with other BI_n open.		–1.2	–0.73		V
I_I	Input current at maximum input voltage	BI_n under test at +5.5V, other BI_n at ground. VTTL at +5.5V.				500	µA
I_{IH}	High level input current	BI_n under test at +2.4V, other BI_n at ground.				70	µA
$-I_{IL}$	Low level input current	BI_n under test at +0.4V, other BI_n at +2.4V.				70	µA
I_{OZH}	Off–state output current, High level voltage applied	Store Low state in register AB. $\overline{OEAB}$ and $\overline{OEBA}$ at V_{IHMAX}. Apply 2.4V to BO_n under test.				80	µA
I_{OZL}	Off–state output current, Low level voltage applied	Store High state in register AB. $\overline{OEAB}$ and $\overline{OEBA}$ at V_{IHMAX}. Apply 0.5V to BO_n under test.				40	µA
$-I_{OS}$	Short circuit output current[4]	Store High state in register AB. One BO_n under test at ground. $\overline{OEAB}$ at V_{ILMIN}.		60	95	225	mA
ITTLH	TTL supply current with outputs High	Store High state in register AB. $\overline{OEAB}$ at V_{ILMIN}. All BO_n open. VTTL at +5.5V.			20	30	mA
ITTLL	TTL supply current with outputs Low	Store Low state in register AB. $\overline{OEAB}$ at V_{ILMIN}. All BO_n open. VTTL at +5.5V.			25	35	mA
ITTLZ	TTL supply current with outputs in the high impedance state	$\overline{OEAB}$ at V_{IHMAX}. All BO_n open. VTTL at +5.5V.			30	40	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I_{OS}, the use of a high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR TTL–TO–ECL DATA FLOW

PLCC $GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –5.7V to –4.2V, VTTL = 4.5V to 5.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency CPBA	Waveform 1	350		350		350		MHz
t_{PZH} t_{PHZ}	Propagation delay CPBA to A_n	Waveform 1	2.0 0.5	4.5 3.0	2.0 0.5	4.5 3.0	2.0 0.5	4.5 3.0	ns ns
t_{PZH}	Output enable time $\overline{OEBA}$ to A_n	Waveform 3	2.0	4.5	2.0	4.5	2.0	4.5	ns
t_{PHZ}	Output disable time $\overline{OEBA}$ to A_n	Waveform 3	0.5	2.5	0.5	2.5	0.5	2.5	ns
t_{TZH} t_{THZ}	Transition time for A_n	Waveform 1	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time BI_n to CPBA	Waveform 1	3.5 4.0		3.5 4.0		3.5 4.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time BI_n to CPBA	Waveform 1	0 0		0 0		0 0		ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time $\overline{CEBA}$ to CPBA	Waveform 2	1.0 1.5		1.0 1.5		1.0 1.5		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time $\overline{CEBA}$ to CPBA	Waveform 2	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width CPBA	Waveform 1	1.0 1.0		1.0 1.0		1.0 1.0		ns ns

NOTE: For AC test setup information, see AC Testing, Chapter 2, Section 3.

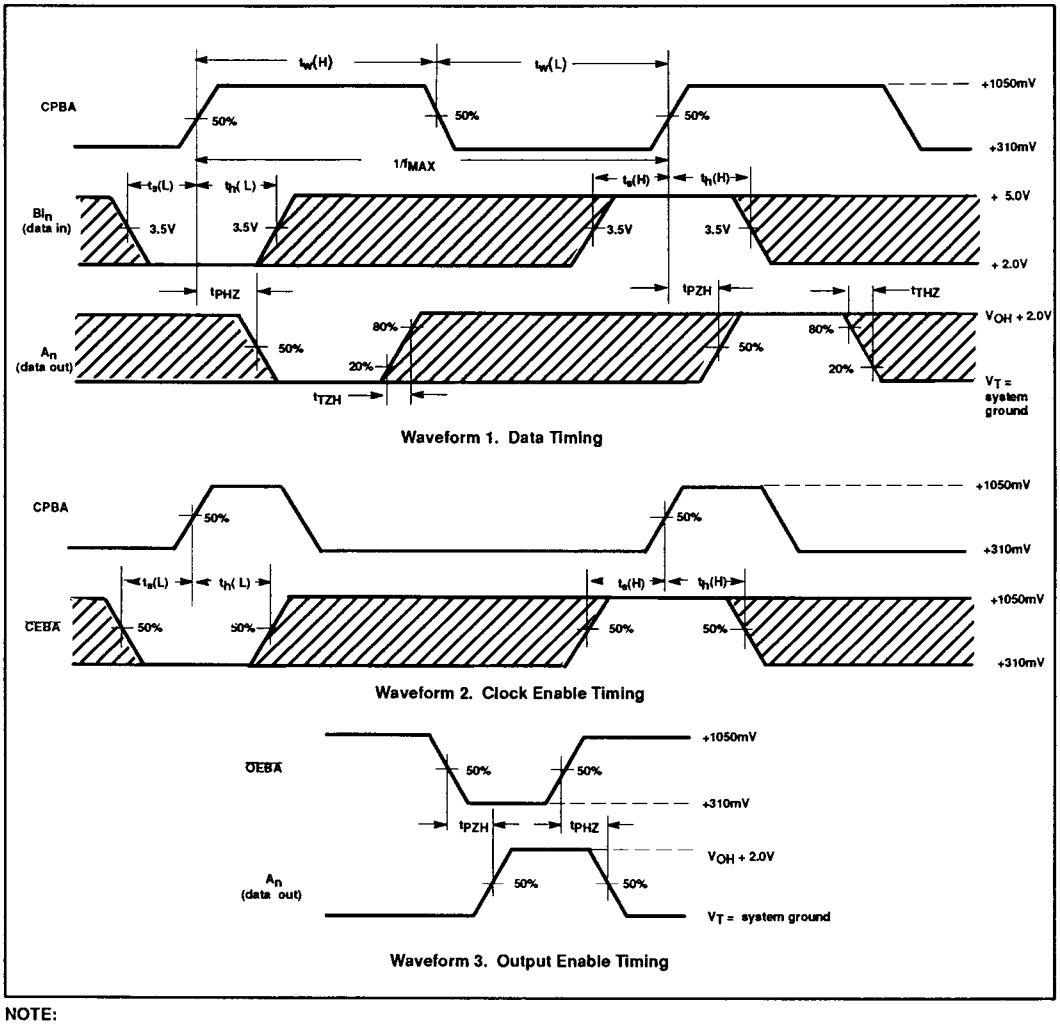
AC ELECTRICAL CHARACTERISTICS FOR ECL–TO–TTL DATA FLOW

PLCC $GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –5.7V to –4.2V, VTTL = 4.5V to 5.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency CPAB	Waveform 4	300		300		300		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to BO_n	Waveform 4	1.5 2.0	4.0 4.5	1.5 2.0	4.0 4.5	1.5 2.0	4.0 4.5	ns ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEAB}$ to BO_n	Waveform 6	1.5 2.0	4.0 5.0	1.5 2.0	4.0 5.0	1.5 2.0	4.0 5.0	ns ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEAB}$ to BO_n	Waveform 6	2.0 4.0	5.0 7.0	2.0 4.0	5.0 7.0	2.0 4.0	5.0 7.0	ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time A_n to CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time A_n to CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time $\overline{CEAB}$ to CPAB	Waveform 5	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time $\overline{CEAB}$ to CPAB	Waveform 5	1.0 1.5		1.0 1.5		1.0 1.5		ns ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns

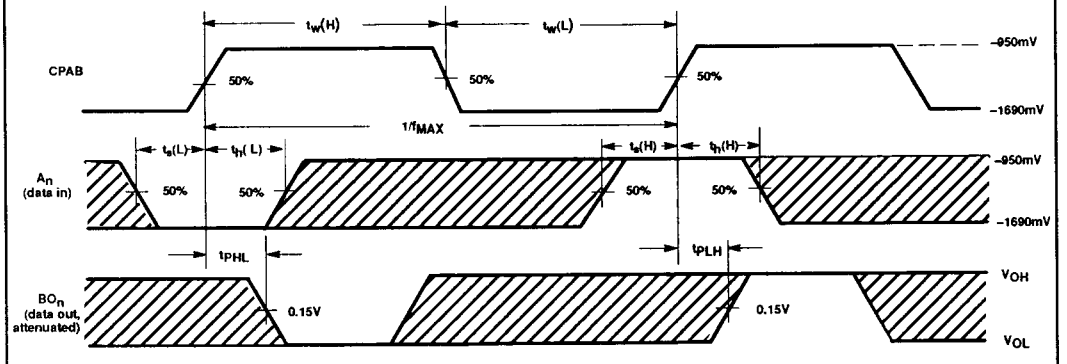
NOTE: For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS FOR TTL–TO–ECL DATA FLOW

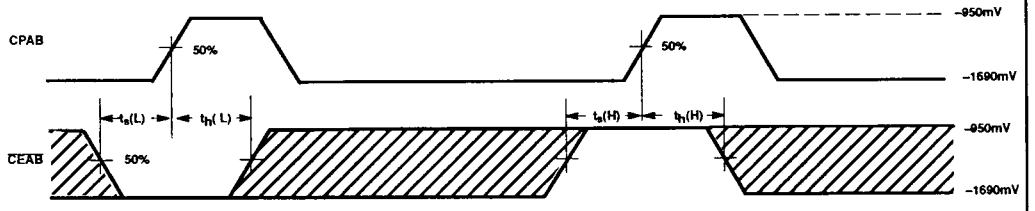


NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

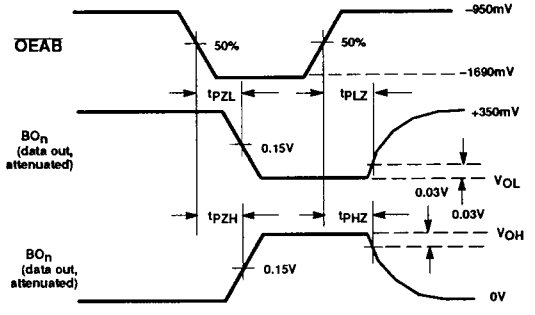
AC WAVEFORMS FOR ECL–TO–TTL DATA FLOW



Waveform 4. Data Timing



Waveform 5. Clock Enable Timing



Waveform 6. Output Enable and Disable Timing

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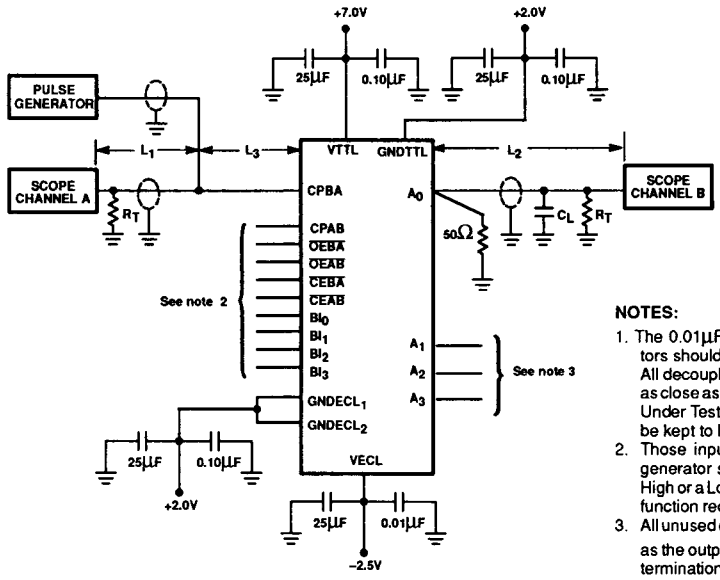
AC TEST CIRCUIT FOR TTL–TO ECL DATA FLOW



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

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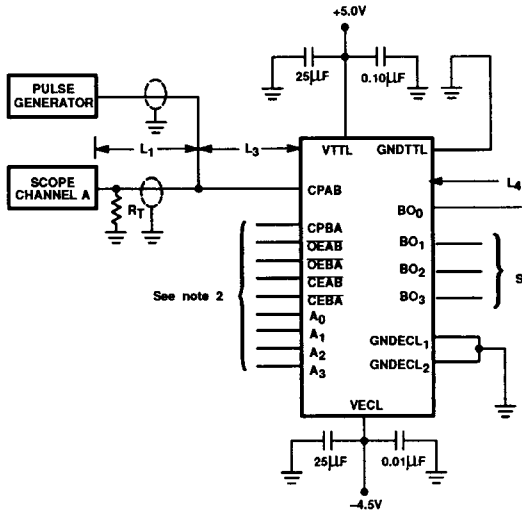
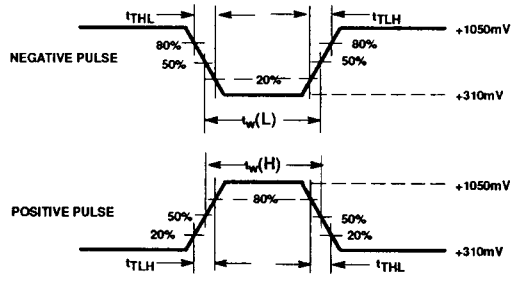
AC TEST CIRCUIT FOR ECL–TO TTL DATA FLOW



NOTES:

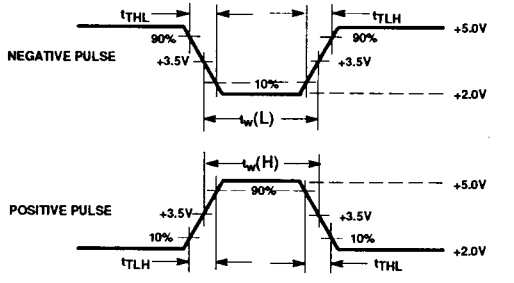
1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and R_L, should not exceed 1/4 inch.
5. R_T = 50Ω termination internal to scope. R_1 = 450Ω. R_L = 500Ω.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L = 50pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. Measure t_{PLZ} and t_{PZL} with the switch closed. Other AC parameters are tested with the switch open.

INPUT PULSE DEFINITION FOR TTL–TO–ECL DATA FLOW



INPUT PULSE REQUIREMENTS FOR
CPAB, CPBA, CEAB, CEBA, OEAB, OEBA
$GNDECL_1 = GNDECL_2 = GNDTTL = +2.0V \pm 0.010V$,
VECL = –2.8V to –2.2V, VTTL = +6.5V to +7.5V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

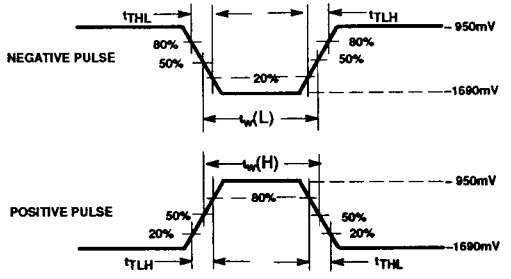


INPUT PULSE REQUIREMENTS FOR BI_n
$GNDECL_1 = GNDECL_2 = GNDTTL = +2.0V \pm 0.010V$,
VECL = –2.8V to –2.2V, VTTL = +6.5V to +7.5V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
TTL	$3.0V_{p-p}$	1MHz	500ns	2.5 ± 0.2ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION FOR ECL–TO–TTL DATA FLOW



INPUT PULSE REQUIREMENTS FOR
A_n, CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$
$GNDECL_1 = GNDECL_2 = GNDTTL = 0V$ (system ground),
VECL = –4.8V to –4.2V, VTTL = +4.5V to +5.5V

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns