MC68440
MC68442

Technical Summary

Dual-Channel Direct Memory Access Controllers

M68000 microprocessors utilize state-of-the-art MOS technology to maximize performance and throughput. The MC68440 dual-channel direct memory access controller (DDMA) is designed to complement the performance and architectural capabilities of M68000 Family microprocessors by moving blocks of data in a quick, efficient manner with minimum intervention from a processor.

The MC68442 extended dual-channel direct memory access controller (EDMA) implements an expanded addressing range over that of the MC68440 with the addition of eight address lines and one function code line (A24-A31 and FC3). This allows the EDMA to linearly access four giagbytes in any of 16 address spaces.

NOTE

Information contained in this document applies to both the DDMA and the EDMA. Reference is primarily given to the DDMA where the descriptions are identical. When applicable, difference data for the EDMA will be highlighted.

The DDMA and EDMA perform memory-to-memory, peripheral-to-memory, and memory-to-peripheral data transfers by utilizing the following features:

- Two Independent DMA Channels with Programmable Priority
- Asynchronous M68000 Bus Structure with
  - DDMA — 24-Bit Address and a 16-Bit Data Bus
  - EDMA — 32-Bit Address and a 16-Bit Data Bus
- Fast Transfer Rates: Up to 5 Megabytes per Second at 10 MHz, No Wait States
- Fully Supports all M68000 Bus Options such as Halt, Bus Error, and Retry
- FIFO Locked Step Support with Device Transfer Complete Signal
- Can Operate on an 8-Bit Data Bus with the MC68008
- Flexible Request Generation:
  - Internal, Maximum Rate
  - Internal, Limited Rate
  - External, Cycle Steal
  - External, Burst
- Programmable 8-Bit or 16-Bit Peripheral Device Types:
  - Explicitly Addressed, M68000 Type
  - Implicitly Addressed:
    - Device with Request and Acknowledge
    - Device with Request, Acknowledge, and Ready
- Non-Contiguous Block Transfer Operation (Continue Mode)
- Block Transfer Restart Operation (Reload Mode)
- Pin and Register Compatible Functional Subset of the MC68450 DMAC

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

INTRODUCTION

The main purpose of a direct memory access (DMA) controller in any system is to transfer data at very high rates, usually much faster than a microprocessor under software control can handle. The term DMA is used to refer to the ability of a peripheral device to access memory in a system in the same manner as a microprocessor does. DMA operations can occur concurrently with other operations that the system processor needs to perform, thus greatly boosting overall system performance. Figure 1 illustrates a typical system configuration using a DMA interface to a high speed disk storage device. In a system such as this, the DDMA will move blocks of data between the disk and memory at rates approaching the limits of the memory bus since the simple function of data movement is implemented in high speed MOS hardware. A block of data consists of a sequence of byte or word operands starting at a specific address in memory with the length of the block determined by a transfer count as shown in Figure 2. A single channel operation may involve the transfer of several blocks of data between the memory and a device.

Any operation involving the DDMA will follow the same basic steps: channel initialization by the system processor, data transfer, and block termination. In the initialization phase, the host processor loads the registers of the DDMA with control information, address pointers, and transfer counts and then starts the channel. During the transfer phase, the DDMA accepts requests for operand transfers and provides addressing and bus control for the transfers. The termination phase occurs after the operation is complete, when the DDMA indicates the status of the operation in a status register. During all phases of a data transfer operation, the DDMA will be in one of three operating modes:

IDLE This is the state that the DDMA assumes when it is reset by an external device and waiting for initialization by the system processor or an operand transfer request from a peripheral.

MPU This is the state that the DDMA enters when it is chip selected by another bus master in the system (usually the main system processor). In this mode, the DDMA internal registers are written or read, to control channel operation or check the status of a block transfer.

DMA This is the state that the DDMA enters when it is acting as a bus master to perform an operand transfer.

TRANSFER MODES

The DDMA can perform implicit address or explicit address data transfers. Implicitly addressed devices do not require the generation of a device data register address

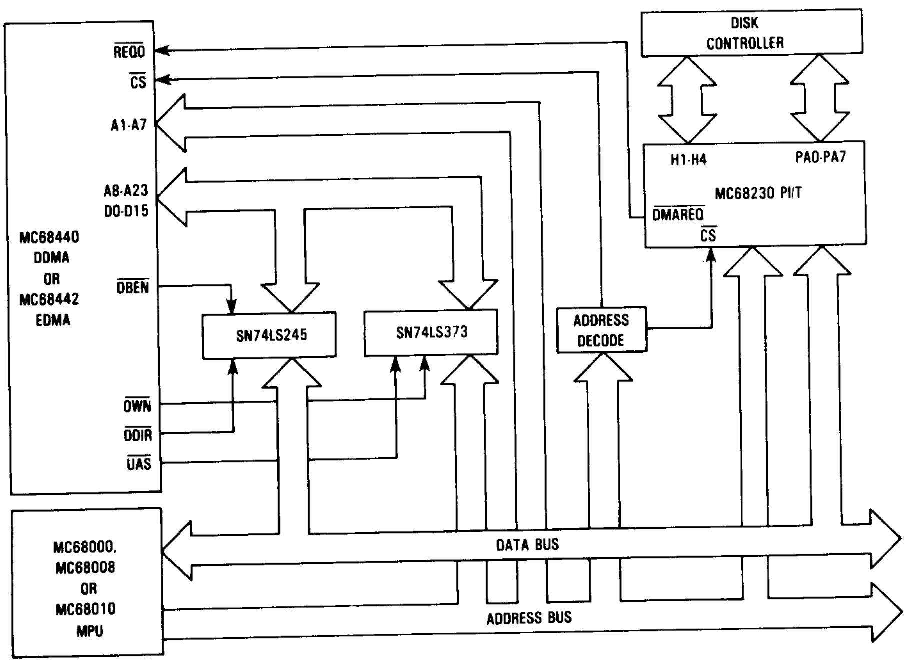

Figure 1. Typical System Configuration

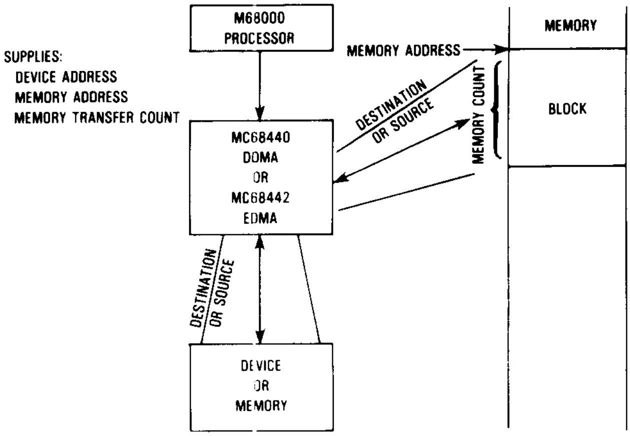

Figure 2. Data Block Format

for a data transfer. Such a device is controlled by a five signal device control interface on the DDMA during implicit address transfers as shown in Figure 3. Since only memory is addressed during such a data transfer, this method is called the single-address method.

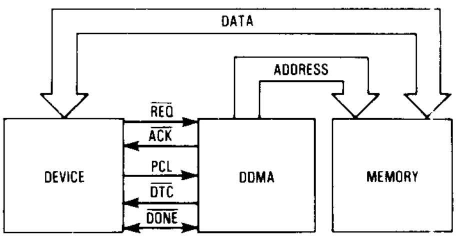

Figure 3. Implicitly Addressed Device Interface

Explicitly addressed devices require that a data register within the peripheral device be addressed. No signals other than the M68000 asynchronous bus control signals are needed to interface with such a device, although any of the five device control signals may also be used. Because the address bus is used to access the peripheral, the data cannot be directly transferred to/from memory since memory also requires addressing. Therefore, data is transferred from the source to an internal holding register in the DDMA and then transferred to the destination during a second bus transfer as shown in Figure 4. Since both memory and the device are addressed during such a data transfer, this method is called the dual-address method.

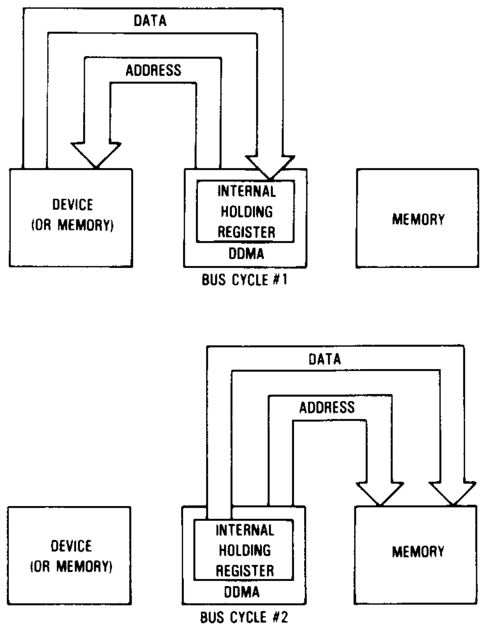

Figure 4. Dual-Address Transfer Sequence

REQUEST MODES

Requests may be externally generated by a device or internally generated by the auto-request mechanism of the DDMA. Auto-requests may be generated either at the maximum rate, where the channel always has a request pending, or at a limited rate determined by selecting a portion of the bus bandwidth to be available for DMA activity. External requests can be either burst requests or cycle steal requests that are generated by the request signal associated with each channel.

REGISTERS

The DDMA contains 17 on-chip registers for each of the two channels plus one general control register, all of which are under complete software control. The user programmer's model of the registers is shown in Figure 5.

The DDMA registers contain information about the data transfer such as the source and destination address and function codes, transfer count, operand size, device port size, channel priority, continuation address and transfer count, and the function of the peripheral control line. One register also provides status and error information on channel activity, peripheral inputs, and various events which may have occurred during a DMA transfer. A general control register selects the bus utilization factor to be used in limited rate auto-request DMA operations.

SIGNAL DESCRIPTION

The following paragraphs contain a brief description of the input and output signals. Included at the end of the functional description of the signals is a table describing the electrical characteristics of each pin (i.e., the type of driver used).

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NOTE

The terms **assertion** and **negation** will be used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or false.

SIGNAL ORGANIZATION

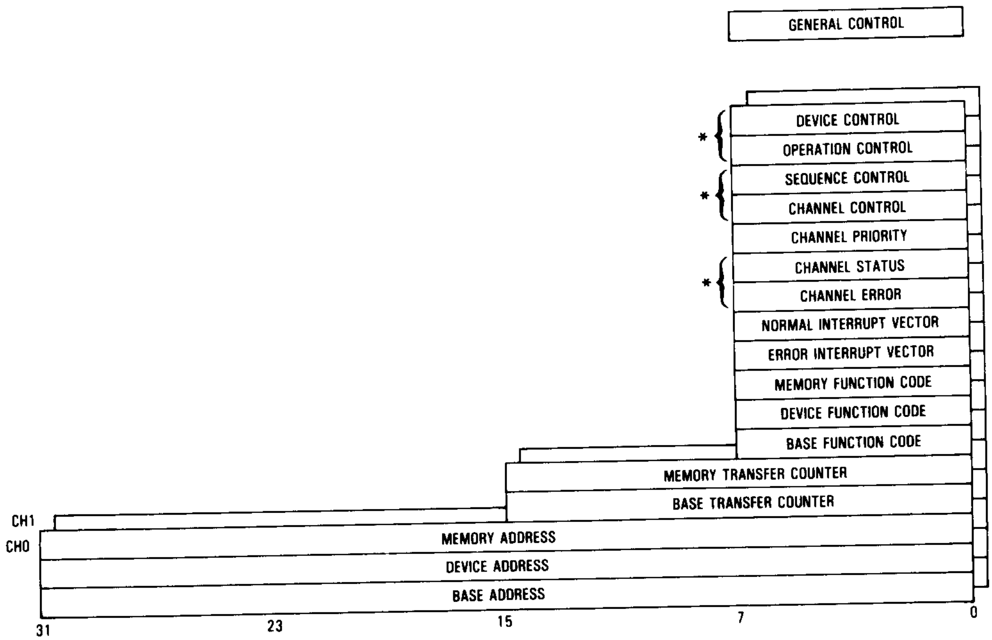
The input and output signals can be functionally organized into the groups shown in Figures 6 and 7. The function of each signal or group of signals is discussed in the following paragraphs.

Address/Data Bus (A8/D0 through A23/D15)

This 16-bit bus is time multiplexed to provide address outputs during the DMA mode of operation and is used as a bidirectional data bus to input data from an external device (during an MPU write or DMA read) or to output data to an external device (during an MPU read or a DMA write). This is a three-state bus and is demultiplexed using external latches and buffers controlled by the multiplex control lines.

Lower Address Bus (A1 through A7)

These bidirectional three-state lines are used to address the DDMA internal registers in the MPU mode and



*Word aligned register pairs.

Figure 5. DDMA Programmer's Model

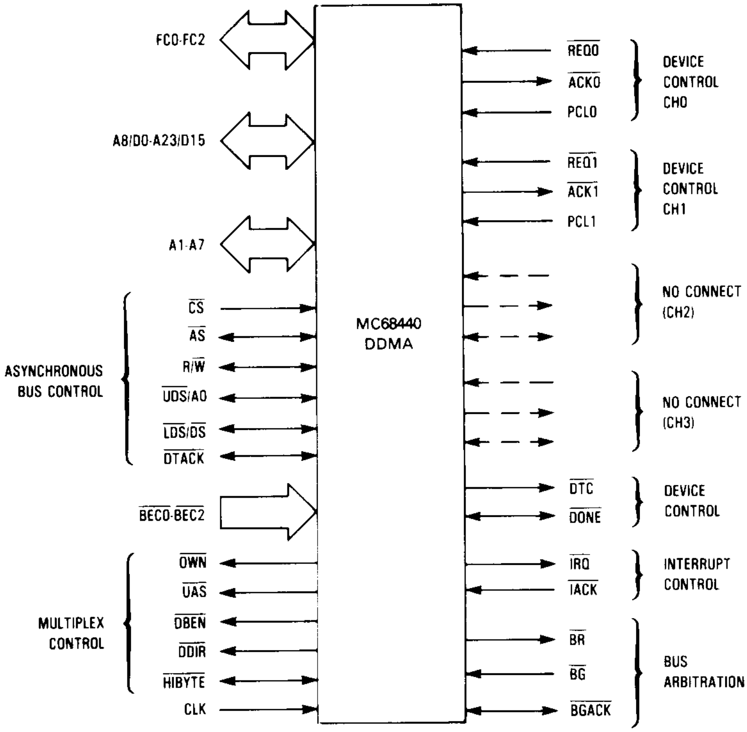


Figure 6. MC68440 Signal Organization

to provide the lower seven address outputs in the DMA mode.

EDMA Upper Address Bus (A24 through A31)

The EDMA implements an expanded addressing range over that of the DDMA with the addition of eight address lines. This allows the EDMA to linearly access four gigabytes in any of 16 address spaces. A24-A31 are non-multiplexed, with timing characteristics identical to address lines A1-A7.

Function Codes (DDMA — FC0 through FC2, EDMA — FC0 through FC3)

These three-state output lines are used in the DMA mode to further qualify the value on the address bus to provide eight separate address spaces that may be defined by the user. The value placed on these lines is taken from one of the internal function code registers, depending on the source register for the address used during a DMA bus cycle.

Asynchronous Bus Control

Asynchronous data transfers are handled using the following control signals: chip select, address strobe, read/write, upper and lower data strobes (or A0 and data strobe when using an 8-bit bus), and data transfer acknowledge. These signals are described in the following paragraphs.

CHIP SELECT ($\overline{CS}$). This input signal is used to select the DDMA for an MPU bus cycle. When $\overline{CS}$ is asserted, the address on A1-A7 and the data strobes (or A0 when using an 8-bit bus) select the internal DDMA register that will be involed in the transfer. $\overline{CS}$ should be generated by qualifying an address decode signal with the address and data strobes.

ADDRESS STROBE ($\overline{AS}$). This bidirectional signal is used as an output in the DMA mode to indicate that a valid address is present on the address bus. In the MPU or IDLE modes, it is used as an input to determine when the DDMA can take control of the bus (if the DDMA has requested and been granted use of the bus).

READ/WRITE (R/$\overline{W}$). This bidirectional signal is used to indicate the direction of a data transfer during a bus cycle. In the MPU mode, a high level indicates that a transfer is from the DDMA to the data bus and a low level indicates a transfer from the data bus to the DDMA. In the DMA mode, a high level indicates a transfer from the addressed memory or device to the data bus, and a low level indicates a transfer from the data bus to the addressed memory or device.

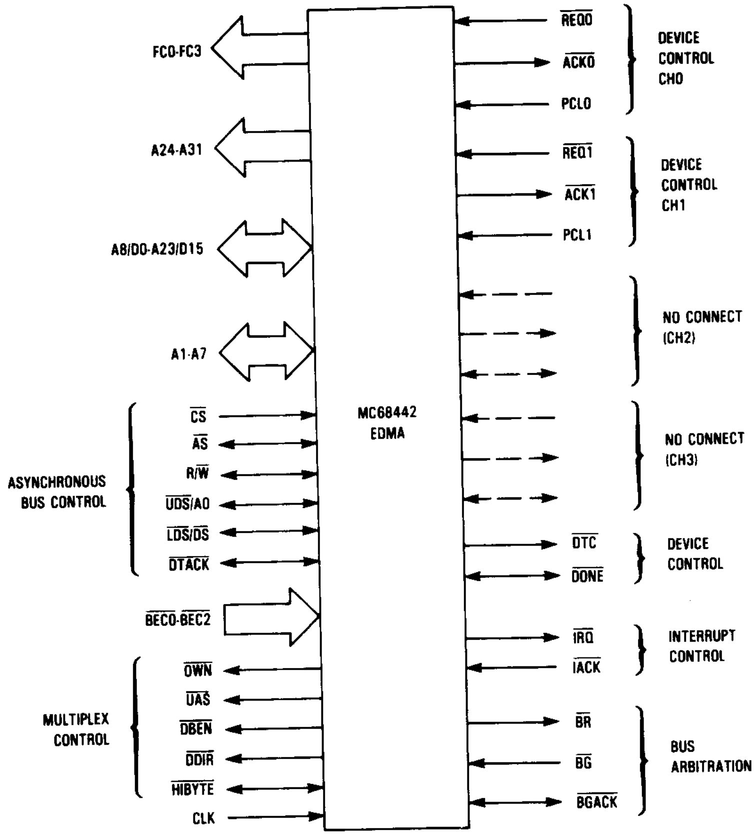


Figure 7. MC68442 Signal Organization

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UPPER AND LOWER DATA STROBES (UDS/A0 AND LDS/DS). These bidirectional lines are used for different purposes depending on whether the DDMA is operating on an 8-bit or a 16-bit bus.

When using a 16-bit bus, these pins function as UDS and LDS. During any bus cycle, UDS is asserted if data is to be transferred over data lines D8-D15 and LDS is asserted if data is to be transferred over data lines D0-D7. UDS/LDS are asserted by the DDMA when operating in the DMA mode and by another bus master when in the MPU mode.

When using an 8-bit bus, these pins function as A0 and DS. A0 is an extension to the lower address lines to provide the address of a byte in the 16 megabyte address map and is valid when A1-A7 are valid. DS is used as a data strobe to enable external data buffers and to indicate that valid data is on the bus during a write cycle.

DATA TRANSFER ACKNOWLEDGE (DTACK). This bidirectional line is used to signal that an asynchronous bus cycle may be terminated. In the MPU mode, this output indicates that the DDMA has accepted data from the MPU or placed data on the bus for the MPU. In the DMA mode, this input is monitored by the DDMA to determine when to terminate a bus cycle. As long as DTACK remains negated, the DDMA will insert wait cycles into a bus cycle and when DTACK is asserted, the bus cycle will be terminated (except when PCL is used as a ready signal, in which case both signals must be asserted before the cycle is terminated).

BUS EXCEPTION CONTROL (BEC0 THROUGH BEC2). These input lines provide an encoded signal that indicates an abnormal bus condition such as a bus error or reset. Refer to **4.4.2 Bus Exception Control Functions** for a detailed description of the function of these pins.

Multiplex Control

These signals are used to control external multiplex/demultiplex devices to separate the address and data information on the A8/D0-A23/D15 lines and to transfer data between the upper and lower halves of the data bus during certain DMA bus cycles.

Figure 8 shows the five external devices needed to demultiplex the address/data pins and the interconnection of the multiplex control signals. The SN74LS245 that may connect the upper and lower halves of the data bus is needed only if an 8-bit device is used to transfer data to or from a 16-bit system data bus during single address transfers. When the DDMA is used on an 8-bit system data bus with 8-bit devices, only the SN74LS245 buffer for D0-D7 is needed.

OWN (OWN). This output indicates that the DDMA is controlling the bus. It is used as the enable signal to turn on the external address latch drivers and control signal buffers.

UPPER ADDRESS STROBE (UAS). This output is used as the gate signal to the transparent latches that capture the value of A8-A23 on the multiplexed address/data bus.

DATA BUFFER ENABLE (DBEN). This output is used as the enable signal to the external bidirectional data buffers.

DATA DIRECTION (DDIR). This output controls the direction of the external bidirectional data buffers. If DDIR is high, the data transfer is from the DDMA to the data bus. If DDIR is low, the data transfer is from the data bus to the DDMA.

HIGH BYTE (HIBYTE). This bidirectional signal determines the size of the bus used by the DDMA during a reset operation. If this signal is asserted (tied to ground) during reset, the data bus size is eight bits and HIBYTE

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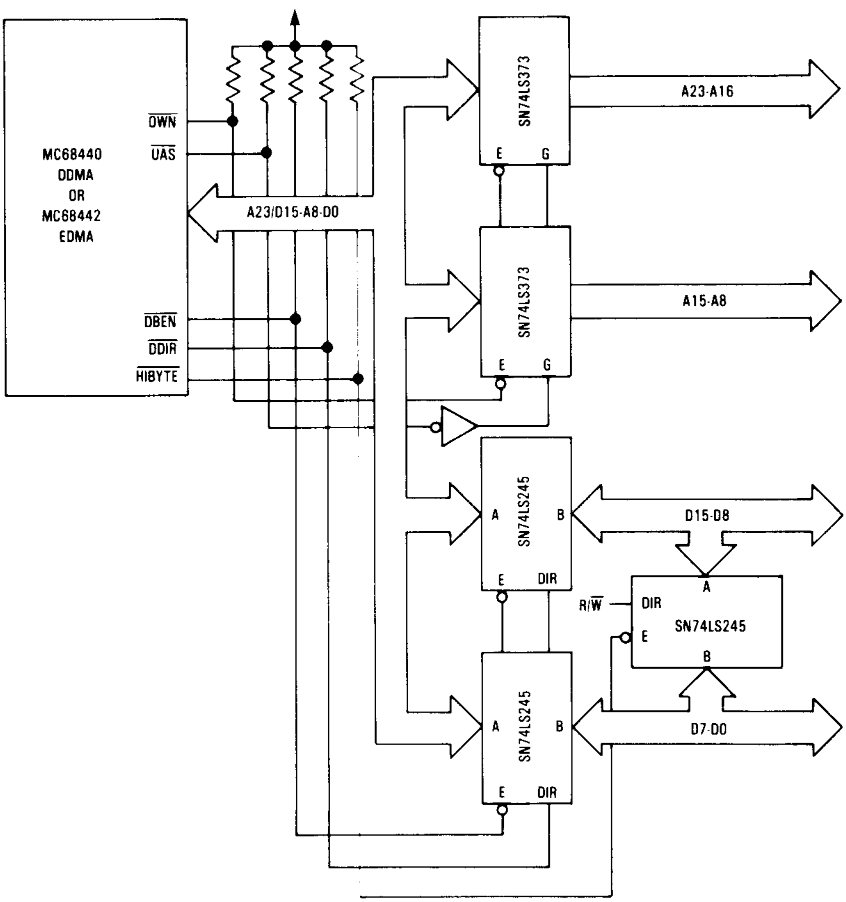

Figure 8. Demultiplex Logic

will not be used as an output. If it is negated (pulled high by a resistor) during reset, the data bus size is assumed to be 16 bits and HIBYTE will be used as an output during single-address DMA transfers between an 8-bit device and a 16-bit memory. As an output, HIBYTE indicates that data will be present on data lines D8-D15 that must be transferred to data lines D0-D7 or vice versa through an external buffer during a single address transfer between an 8-bit device and a 16-bit memory.

Bus Arbitration Control

These three signals form a bus arbitration circuit used to determine which device in a system will be the current bus master.

BUS REQUEST (BR). This output is asserted by the DDMA to request control of the bus.

BUS GRANT (BG). This input is asserted by an external bus arbiter to inform the DDMA that it may assume bus mastership as soon as the current bus cycle is completed. The DDMA will not take control of the bus until CS, IACK, AS, and BGACK are all negated.

BUS GRANT ACKNOWLEDGE (BGACK). This bidirectional signal is asserted by the DDMA to indicate that it is the current bus master. BGACK is monitored as an input to determine when the DDMA can become bus master and if a bus master other than the system MPU is a master during limited rate auto-request operation.

Interrupt Control

These two signals form an interrupt request/acknowledge handshake circuit with an MPU.

INTERRUPT REQUEST (IRQ). This output is asserted by the DDMA to request service from the MPU.

INTERRUPT ACKNOWLEDGE (IACK). This input is asserted by the MPU to acknowledge that it has received an interrupt from the DDMA. In response to the assertion of IACK, the DDMA will place a vector on D0-D7 that will be used by the MPU to fetch the address of the proper DDMA interrupt handler routine.

Device Control

These eight lines perform the interface between the DDMA and two peripheral devices. Two sets of three lines are dedicated to a single DDMA channel and its associated peripheral; the remaining two lines are global signals shared by both channels.

REQUEST (REQ0, REQ1). These inputs are asserted by a peripheral device to request an operand transfer between that peripheral device and memory. In the cycle steal request generation mode, these inputs are edge sensitive; in burst mode, they are level sensitive.

ACKNOWLEDGE (ACK0, ACK1). These outputs are asserted by the DDMA to signal to a peripheral that an operand is being transferred in response to a previous transfer request.

PERIPHERAL CONTROL LINE (PCL0, PCL1). These inputs are multi-purpose signals that may be programmed to function as ready, abort, reload, status, or interrupt inputs.

DATA TRANSFER COMPLETE (DTC). This output is asserted by the DDMA during any DDMA bus cycle to indicate that the data has been successfully transferred (i.e., the bus cycle was not terminated abnormally).

DONE (DONE). This bidirectional signal is asserted by the DDMA or a peripheral device during any DMA bus cycle to indicate that the data being transferred is the last item in a block. The DDMA will assert this signal during a bus cycle when the memory transfer count register is decremented to zero and the continue bit in the channel control register is not set.

Clock (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the DDMA. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times.

No Connection (NC)

Six pins are not connected in order to maintain pin compatibility with the MC68450 DMAC; these pins are in the positions of the device control signals for channels two and three (REQ2, ACK2, PCL2, REQ3, ACK3, and PCL3) on the DMAC. It is suggested that these pins be left unconnected to allow future expansion; however, if a DDMA is placed into a socket designed to also accommodate a DMAC, the four input signals will be ignored and the two output signals will be allowed to float.

SIGNAL SUMMARY

Table 1 is a summary of all the signals discussed in the previous paragraphs.

REGISTER DESCRIPTION

Figure 9 shows the memory mapped locations of the registers for each channel on a 16-bit bus. Figure 10 shows the register summary and may be used for a quick reference to the bit definitions within each register. The register locations defined as 'Null Register' may be read or written; however, a write access will not affect any DDMA channel operation and a read access will always return all ones. In the descriptions of each register, some bits are defined as 'not used', in which case writes to those bits will have no affect and they will always read as zeros.

Table 1. Signal Summary

Signal Name	Direction	Active State	Driver Type
A8/D0-A23/D15	In/Out	High	Three State
A1-A7	In/Out	High	Three State
A24-A31 — EDMA Only	In/Out	High	Three State
FC0-FC2	Out	High	Three State
FC3 — EDMA Only	Out	High	Three State
$\overline{\text{CS}}$	In	Low	—
$\overline{\text{AS}}$	In/Out	Low	Three State*
R/$\overline{\text{W}}$	In/Out	High/Low	Three State*
$\overline{\text{UDS}}$/A0	In/Out	Low/High	Three State*
$\overline{\text{LDS}}$/$\overline{\text{DS}}$	In/Out	Low	Three State*
$\overline{\text{DTACK}}$	In/Out	Low	Open Drain*
$\overline{\text{OWN}}$	Out	Low	Open Drain*
$\overline{\text{UAS}}$	Out	Low	Three State*
$\overline{\text{DBEN}}$	Out	Low	Three State*
$\overline{\text{DDIR}}$	Out	High/Low	Three State*
$\overline{\text{HIBYTE}}$	In/Out	Low	Three State*
$\overline{\text{BEC0}}$-$\overline{\text{BEC2}}$	In	Low	—
$\overline{\text{BR}}$	Out	Low	Open Drain
$\overline{\text{BG}}$	In	Low	—
$\overline{\text{BGACK}}$	In/Out	Low	Open Drain*
$\overline{\text{IRQ}}$	Out	Low	Open Drain
$\overline{\text{IACK}}$	In	Low	—
$\overline{\text{REQ0}}$, $\overline{\text{REQ1}}$	In	Low	—
$\overline{\text{ACK0}}$, $\overline{\text{ACK1}}$	Out	Low	Three State*
PCL0, PCL1	In	Programmed	—
$\overline{\text{DTC}}$	Out	Low	Three State*
$\overline{\text{DONE}}$	In/Out	Low	Open Drain
CLK	In	—	—

*These signals require a pull resistor to maintain a high voltage when in the high-impedance or negated state. However, when these signals go to the high-impedance or negated state, they will first drive the pin high momentarily to reduce the signal rise time.

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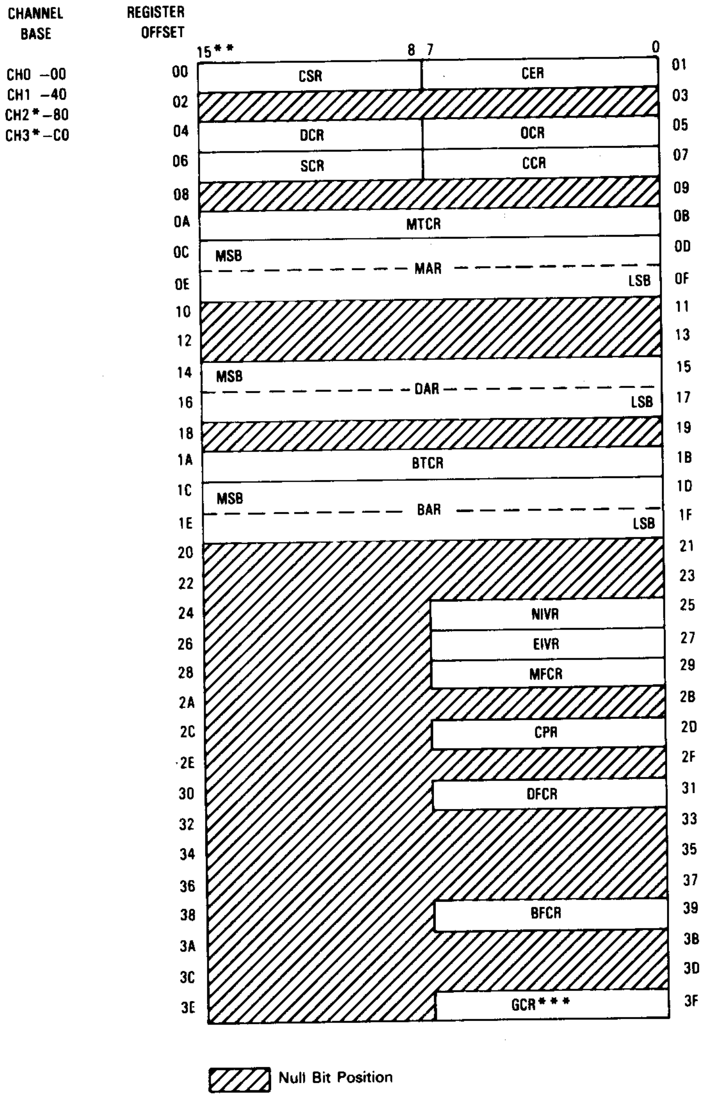

*All accesses to channel 2 and 3 registers will be treated as null accesses.

**When operated on an 8-bit bus, all register data is transferred over D0-D7, the word and long word registers are then accessed as a contiguous set of bytes.

***The GCR is located at FF only.

Figure 9. Register Memory Map

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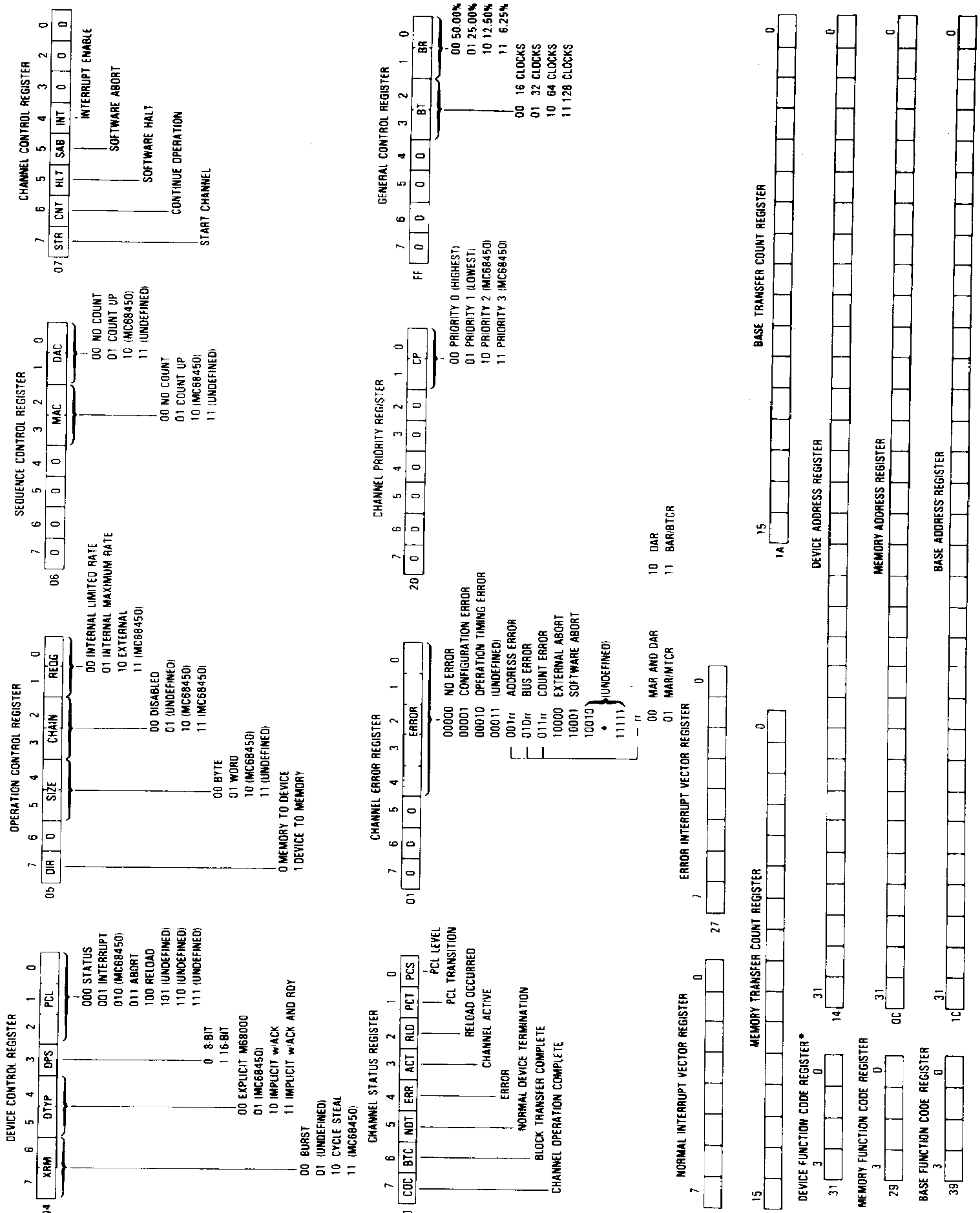

Figure 10. Register Summary

The register memory map is identical to the register memory map for the MC68450 DMAC, including the individual bit assignments within the registers. However, not all functional options available on the DMAC are available on the DDMA and vice versa, and the channel 2 and 3 registers on the DMAC are treated as null registers on the DDMA. If any programmable options labeled 'MC68450 Reserved' or 'Undefined, Reserved' are programmed into a DDMA channel, a configuration error will occur when the MPU attempts to start that channel.

All registers within the DDMA are always accessible as bytes or words by the MPU (assuming that the MPU can gain control of the DMA bus); however, some registers may not or should not be modified while a channel is actively transferring data. If a register may not be modified during operation and an attempt is made to write to it, an operation timing error will be signaled and the channel operation aborted.

RESET OPERATION RESULTS

When the DDMA is reset, either during a system power-up sequence or to re-initialize the DDMA, many of the registers will be affected and will be set to known values. Table 2 shows the hexadecimal value that will be placed in each register by a reset operation.

Table 2. Reset Operation Results

Register	Value	Comments
MARc	XXXXXXXX	
DARc	XXXXXXXX	
BARc	XXXXXXXX	
MFCRc	X	
DFCRc	X	
BFCRc	X	
MTCRc	XXXX	
BTCRc	XXXX	
NIVRc	0F	Uninitialized Vector
EIVRc	0F	Uninitialized Vector
CPRc	00	
DCRc	00	
OCRc	00	
SCRc	00	
CCRc	00	Channel Not Active, Interrupts Disabled
CSRc	00 or 01	(Depending on the Level of PCLc)
CERc	00	No Errors
GCR	00	

X r Indicates an unknown value or the previous value of the register.
c r Is the channel number (i.e., 0 or 1).

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	0.3 to +7.0	V
Input Voltage	V_{in}	0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Symbol	Value	Unit
Thermal Resistance	θ_{JA}		θ_{JC}		°C/W
Ceramic (L Suffix)		30		15*	
Plastic (P Suffix)		30		15*	
Pin Grid Array (R/RC Suffix)		33		15	

*Estimated

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \qquad (1)$$

where:

- T_A = Ambient Temperature, °C
- θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
- P_D = $P_{INT} + P_{I/O}$
- P_{INT} = $I_{CC} \times V_{CC}$, Watts – Chip Internal Power
- $P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected):

$$P_D = K \div (T_J + 273°C) \qquad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \qquad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JA} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} aproximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices," and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

Figure 11 illustrates the graphic solution to the equations, given above, for the specification power dissipation of 1.50 watts over the ambient temperature range of –55°C to 125°C using an average θ_{JA} of 40°C/watt to represent the various MC68440/MC68442 packages. However, actual θ_{JA}'s in the range of 30°C to 50°C/watt only change the curve slightly.

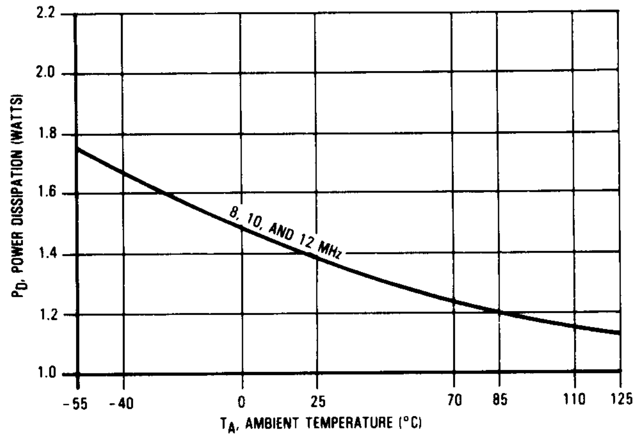

Figure 11. MC68440/MC68442 Power Dissipation vs Ambient Temperature

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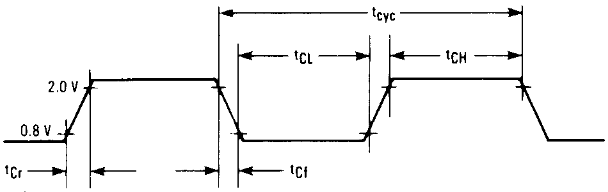
DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 V to 5.25 V, GND = 0 V, T_A = 0°C to 70°C, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage	All Inputs	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	GND − 0.3	0.8	V
Input Leakage Current @ 5.25 V	All Inputs	I_{in}	—	10	μA
Input Capacitance (V_{in} = 0 V, T_A = 25°C, Frequency = 1 MHz)	All Inputs	C_{in}	—	13	pF
Three-State (Off-State) Input Current @ 2.4V/0.4V	AS, A1-A7, BGACK, DTACK, A8/D0-A23/D15, HIBYTE, LDS/DS, UDS/A0, R/W	I_{TSI}	—	20	μA
Open-Drain (Off-State) Input Current @ 5.25 V	IRQ, DONE	I_{DD}	—	20	μA
Output High Voltage (I_{OH} = −400 μA Minimum)	AS, A1-A7, A8/D0-A23/D15, ACK0, ACK1, BR, BGACK, DBEN, DDIR, DTACK, OWN, LDS/DS, UDS/A0, R/W, UAS, DTC, FC0-FC2, IRQ, DONE, HIBYTE	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 3.2 mA Minimum) (I_{OL} = 5.3 mA Minimum) (I_{OL} = 8.9 mA Minimum)	 A1-A7, FC0-FC2 A8/D0-A23/D15, ACK0, ACK1, AS, BGACK, BR, DBEN, DDIR, DTACK, DTC, HIBYTE, LDS/DS, UDS/A0, OWN, R/W, UAS IRQ, DONE	V_{OL}	—	0.5	V
Power Dissipation at 0°C (Frequency = 8 MHz)		P_D	—	1.5	W
Output Load Capacitance		C_L	—	130	pF

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (see Figure 12)

Characteristic	Symbol	8 MHz		10 MHz		12 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	F	2.0	8.0	2.0	10.0	2.0	12.5	MHz
Cycle Period	t_{cyc}	125	500	100	500	80	500	ns
Clock Width Low	t_{CL}	55	250	45	250	35	250	ns
Clock Width High	t_{CH}	55	250	45	250	35	250	ns
Clock Fall Time	t_{Cf}	—	10	—	10	—	5	ns
Clock Rise Time	t_{Cr}	—	10	—	10	—	5	ns



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volts and 2.0 volts.

Figure 12. Clock Input Timing Diagram

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AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (V_{CC} = 4.75 V to 5.25 V, GND = 0 V, T_A = 0°C to 70°C, unless otherwise noted) (see Figures 13 through 19)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	125	500	100	500	80	500	ns
2	Clock Width Low	t_{CL}	55	250	45	250	35	250	ns
3	Clock Width High	t_{CH}	55	250	45	250	35		ns
4	Clock Fall Time	t_{Cf}	—	10	—	10	—	5	ns
5	Clock Rise Time	t_{Cr}	—	10	—	10	—	5	ns
6	MPU Address Valid to $\overline{\text{CS}}$ Low	t_{ADVCSL}	0	—	0	—	0	—	ns
7	MPU $\overline{\text{AS}}$ High to Address Invalid	t_{ASHADI}	0	—	0	—	0	—	ns
8	Asynchronous Input Setup Time	t_{ASI}	20	—	20	—	20	—	ns
9	Data Strobe(s) Low to $\overline{\text{CS}}$ Low	t_{DSLCSL}	0	—	0	—	0	—	ns
10[1]	$\overline{\text{CS}}$ Low to $\overline{\text{DDIR}}$ High (MPU Read)	$t_{CSLDDHR}$	2 Clks + 20	3 Clks + 80	2 Clks + 20	3 Clks + 70	2 Clks + 20	3 Clks + 60	ns
11[1]	$\overline{\text{CS}}$ Low to $\overline{\text{DBEN}}$ Low (MPU Read)	$t_{CSLENLR}$	2.5 Clks + 20	3.5 Clks + 80	2.5 Clks + 20	3.5 Clks + 70	2.5 Clks + 20	3.5 Clks + 60	ns
12[1]	$\overline{\text{CS}}$ Low to Data Out Valid (MPU Read)	t_{CSLDOV}	2 Clks + 20	3 Clks + 110	2 Clks + 20	3 Clks + 95	2 Clks + 20	3 Clks + 80	ns
13[1]	$\overline{\text{CS}}$ Low to $\overline{\text{DTACK}}$ Low (MPU Read)	$t_{CSLDTLR}$	3.5 Clks + 20	4.5 Clks + 80	3.5 Clks + 20	4.5 Clks + 70	3.5 Clks + 20	4.5 Clks + 60	ns
14	Clock High to Data Out Valid	t_{CHDOV}	—	90	—	75	—	65	ns
15	$\overline{\text{CS}}$ High to $\overline{\text{DDIR}}$ High Impedance	t_{CSHDOZ}	—	60	—	50	—	40	ns
16	$\overline{\text{CS}}$ High to $\overline{\text{DBEN}}$ High Impedance	t_{CSHENZ}	—	60	—	50	—	40	ns
17	$\overline{\text{CS}}$ High to Data High Impedance	t_{CSHDZ}	—	60	—	50	—	40	ns
18	Clock Low to $\overline{\text{DTACK}}$ Low	t_{CLDTL}	—	60	—	50	—	40	ns
19	$\overline{\text{DTACK}}$ Low to $\overline{\text{CS}}$ High	t_{DTLSCH}	0	—	0	—	0	—	ns
20	$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High	t_{CSHDTH}	—	50	—	45	—	35	ns
21	$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High Impedance	t_{CSHDTZ}	—	60	—	50	—	40	ns
22	$\overline{\text{CS}}$ Width High	t_{CSWH}	1	—	1	—	1	—	Clk Per
23	R/$\overline{\text{W}}$ Low to $\overline{\text{CS}}$ Low	t_{RWLCSL}	0	—	0	—	0	—	ns
24[1]	$\overline{\text{CS}}$ Low to $\overline{\text{DDIR}}$ Low (MPU Write)	$t_{CSLDDLW}$	1 Clk + 20	2 Clks + 80	1 Clk + 20	2 Clks + 70	1 Clk + 20	2 Clks + 60	ns
25[1]	$\overline{\text{CS}}$ Low to $\overline{\text{DBEN}}$ Low (MPU Write)	$t_{CSLENLW}$	1.5 Clks + 20	2.5 Clks + 80	1.5 Clks + 20	2.5 Clks + 70	1.5 Clks + 20	2.5 Clks + 60	ns
26	$\overline{\text{CS}}$ Low to Data In Valid (MPU Write)	t_{CSLDIV}	—	3	—	3	—	3	Clk Per
27[1]	$\overline{\text{CS}}$ Low to $\overline{\text{DTACK}}$ Low (MPU Write)	$t_{CSLDTLW}$	2.5 Clks + 20	3.5 Clks + 80	2.5 Clks + 20	3.5 Clks + 70	2.5 Clks + 20	3.5 Clks + 60	ns
28[8]	$\overline{\text{DDIR}}$ Low to $\overline{\text{DBEN}}$ Low	t_{DDLENL}	30	—	20	—	20	—	ns
29	$\overline{\text{DBEN}}$ Low to Data In Valid	t_{ENLDIV}	—	105	—	80	—	60	ns
30	Data In Valid to Clock High (Setup Time)	t_{DIVCH}	15	—	15	—	10	—	ns
31[8]	$\overline{\text{DTACK}}$ Low to $\overline{\text{DDIR}}$ High	t_{DTLDDH}	125	—	100	—	80	—	ns
32[8]	$\overline{\text{DTACK}}$ Low to $\overline{\text{DBEN}}$ High	t_{DTLENH}	65	—	50	—	40	—	ns

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Continued)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12 MHz		Unit
			Min	Max	Min	Max	Min	Max	
33[8]	$\overline{DBEN}$ High to $\overline{DDIR}$ High (Read)	t_{ENHDDH}	30	—	20	—	20	—	ns
34	$\overline{CS}$ High to Data Not Valid	t_{CSHDNV}	0	—	0	—	0	—	ns
34a	Clock Low to Data Not Valid	t_{CLDNV}	0	—	0	—	0	—	ns
35	$\overline{REQ}$ Width Low	t_{REQL}	2	—	2	—	2	—	Clk Per
36	$\overline{REQ}$ Low to $\overline{BR}$ Low	$t_{REQLBRL}$	2 Clks +20	3 Clks +80	2 Clks +20	3 Clks +70	2 Clks +70	3 Clks +60	ns
37[2]	$\overline{REQ}$ Low to $\overline{BGACK}$ Low	$t_{REQLBKL}$	4	—	4	—	4	—	Clk Per
38	Clock High to $\overline{BR}$ Low	t_{CHBRL}	—	60	—	50	—	40	ns
39[3]	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLBGL}	1	—	−1	—	−1	—	Clk Per
40[3]	$\overline{BR}$ Low to $\overline{AS}$ In High	t_{BRLASH}	1	—	1	—	−1	—	Clk Per
41	Clock High to $\overline{BR}$ High Impedance	t_{CHBRZ}	—	60	—	50	—	40	ns
42	Clock Low to $\overline{OWN}$ Low	t_{CLOL}	—	60	—	50	—	40	ns
43	Clock High to $\overline{BGACK}$ Low	t_{CHBKL}	—	60	—	50	—	40	ns
44[8]	$\overline{BGACK}$ Low to $\overline{BR}$ High Impedance	t_{BKLBRZ}	60	1 Clk +60	50	1 Clk +50	40	1 Clk +40	ns
45	$\overline{BGACK}$ to $\overline{BG}$ High	t_{BKLBGH}	0	—	0	—	0	—	ns
46[2]	$\overline{AS}$, $\overline{CS}$ In High to $\overline{BGACK}$ Low	t_{ASHBKL}	2	—	2	—	2	—	Clk Per
47[2]	Clock Low on which $\overline{OWN}$ Asserted to Clock High on which $\overline{AS}$ Asserted	t_{OLASL}	—	1.5	—	1.5	—	1.5	Clk Per
48	Clock High to $\overline{BGACK}$ High	t_{CHBKH}	—	60	—	50	—	40	ns
49	Clock High to $\overline{BGACK}$ High Impedance	t_{CHBKZ}	—	65	—	55	—	45	ns
50	Clock Low to $\overline{OWN}$ High	t_{CLOH}	—	60	—	50	—	40	ns
51	Clock Low to $\overline{OWN}$ High Impedance	t_{CHOZ}	—	65	—	55	—	45	ns
52[4,8]	$\overline{BGACK}$ High to $\overline{OWN}$ High	t_{BKHOH}	30	—	20	—	20	—	ns
53[8]	$\overline{DTC}$ High Impedance to $\overline{BGACK}$ High	t_{TCZBKH}	—	1 Clk +60	—	1 Clk +50	—	1 Clk +40	ns
54	Clock High to Address/FC Valid	t_{CHAV}	—	90	—	75	—	65	ns
55	Clock High to Control and Non-Muxed Bus Lines High Impedance	t_{CHNXZ}	—	60	—	50	—	40	ns
56	CLK Low to Muxed Address Bus High Impedance	t_{CLMXAZ}	—	60	—	50	—	40	ns
57	Data In Valid to Clock High (Setup Time)	t_{DIVCH}	15	—	15	—	10	—	ns
58	Clock High to $\overline{UAS}$ Low	t_{CHUL}	—	90	—	75	—	54	ns
59	Clock High to $\overline{UAS}$ High	t_{CHUH}	—	60	—	50	—	40	ns
60[8]	$\overline{UAS}$ High to Address Invalid	t_{UHAI}	20	—	20	—	20	—	ns
61[8]	Address/FC Valid to $\overline{AS}$/$\overline{DS}$ (Read), $\overline{AS}$ (Write) Low	t_{AVSL}	60	—	50	—	40	—	ns
62	$\overline{AS}$, $\overline{DS}$ Width Low (Read)	t_{ASLR}	125	—	100	—	80	—	ns
63	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	—	60	—	50	—	40	ns
64[8]	$\overline{AS}$, $\overline{DS}$ High to Address/FC/Data Invalid	t_{SHAI}	40	—	20	—	20	—	ns

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AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Continued)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12 MHz		Unit
			Min	Max	Min	Max	Min	Max	
65[8]	$\overline{AS}$ High to $\overline{UAS}$ Low	t_{ASHUL}	20	—	20	—	20	—	ns
66[5]	Clock High to $\overline{AS}$ Low	t_{CHASL}	—	50	—	40	—	40	ns
67[8]	$\overline{AS}$ Low to $\overline{DBEN}$ Low	t_{ASLENL}	—	120	—	100	—	80	ns
68	Clock High to $\overline{DS}$ Low (Read)	t_{CHDSLR}	—	60	—	50	—	40	ns
69	Clock High to $\overline{DDIR}$ Low	t_{CHDDL}	—	60	—	50	—	40	ns
70	Clock High to $\overline{DDIR}$ High	t_{CHDDH}	—	60	—	50	—	40	ns
71	Clock Low to $\overline{DBEN}$ Low	t_{CLENL}	—	60	—	50	—	50	ns
72	Clock Low to $\overline{DBEN}$ High (Read)	t_{CLENH}	—	60	—	50	—	40	ns
73	$\overline{DTACK}$ Low to Data In Valid	t_{DTLDIV}	—	105	—	80	—	60	ns
74	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{DSHDTH}	0	100	0	80	0	80	ns
75	$\overline{BEC}$ Valid to $\overline{DTACK}$ Low	$t_{BECVDTL}$	0	—	0	—	0	—	ns
76	$\overline{AS}$ High to $\overline{BEC}$ Negated	$t_{ASHBECN}$	10	—	10	—	—	0	ns
77	$\overline{BEC}$ Width Low	t_{BECL}	2	—	2	—	2	—	Clk Per
78	Clock High to $\overline{ACK}$ Low (Read)	t_{CHAKLR}	—	60	—	50	—	40	ns
79	Clock High to $\overline{ACK}$ High	t_{CHAKH}	—	60	—	50	—	40	ns
80	Clock High to $\overline{DTC}$ Low	t_{CHTCL}	—	50	—	40	—	35	ns
81[4,8]	$\overline{DTC}$ Low to $\overline{DS}$ High	t_{TCLDSH}	30	—	20	—	20	—	ns
82	Clock High to $\overline{DTC}$ High	t_{CHTCH}	—	60	—	50	—	40	ns
83	$\overline{DONE}$ Input Low to Clock on which $\overline{DTC}$ Asserted	t_{DNLTCL}	20	—	20	—	20	—	ns
84	$\overline{DTC}$ Width Low	t_{DTCL}	1	—	1	—	1	—	Clk Per
85	Clock High to $\overline{DONE}$ Low (Read)	t_{CHDNL}	—	60	—	50	—	40	ns
86	Clock High to $\overline{DONE}$ High Impedance	t_{CHDNZ}	—	60	—	50	—	40	ns
87	Clock High to $\overline{IRQ}$ Low	t_{CHIRL}	—	60	—	50	—	40	ns
88	Clock High to $\overline{IRQ}$ High Impedance	t_{CHIRZ}	—	60	—	50	—	40	ns
89	Data Out Valid to $\overline{DS}$ Low	t_{DOVDSL}	70	—	50	—	45	—	ns
90	Clock High to Muxed Data Bus High Impedance	t_{CHMXDZ}	—	60	—	50	—	40	ns
91[8]	$\overline{UAS}$ Low to $\overline{AS}$ Low	t_{ULASL}	60	—	50	—	40	—	ns
92	$\overline{AS}$ Width Low (Write)	t_{ASLW}	250	—	200	—	160	—	ns
93	Clock Low to $\overline{DS}$ Low (Write)	t_{CLDSLW}	—	60	—	50	—	40	ns
94[8]	$\overline{DBEN}$ Low to $\overline{DS}$ Low (Write)	t_{ENLDSL}	60	—	50	—	40	—	ns
95	$\overline{DS}$ Width Low (Write)	t_{DSLW}	70	—	55	—	50	—	ns
96[8]	Address/FC Valid to R/$\overline{W}$ Low	t_{AVRL}	60	—	50	—	40	—	ns
97[8]	R/$\overline{W}$ Low to $\overline{DS}$ Low (Write)	t_{RLDSL}	125	—	100	—	80	—	ns
98[8]	$\overline{DS}$ High to R/$\overline{W}$ High	t_{DSHRH}	20	—	20	—	20	—	ns
99	Clock High to R/$\overline{W}$ High	t_{CHRH}	—	60	—	50	—	40	ns
100[5]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	—	60	—	50	—	40	ns

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AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Concluded)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12 MHz		Unit
			Min	Max	Min	Max	Min	Max	
101	Clock High to DBEN High (Write)	t_{CHENH}	—	60	—	50	—	40	ns
102	DTACK Width High	t_{DTWH}	0	—	0	—	0	—	ns
103	Clock Low to ACK Low (Write)	t_{CLAKLW}	—	60	—	50	—	40	ns
104	Clock Low to DONE Low (Write)	t_{CLDNL}	—	60	—	50	—	40	ns
105	Clock High to HIBYTE Low (Read)	t_{CHHBLR}	—	60	—	50	—	40	ns
106	Clock High to HIBYTE High	t_{CHHBH}	—	60	—	50	—	40	ns
107	DTACK and PCL Low to AS High (Single Address Read)	t_{DTLASH}	190	—	150	—	120	—	ns
108	Clock High to HIBYTE Low (Write)	t_{CLHBLW}	—	60	—	50	—	40	ns
109[8]	ACK Low to DS Low (Single Address Write)	t_{AKLDSL}	80	—	60	—	45	—	ns
110	PCL Low to DS Low (ACK with Ready Write)	t_{PCLDSL}	190	—	150	—	120	—	ns

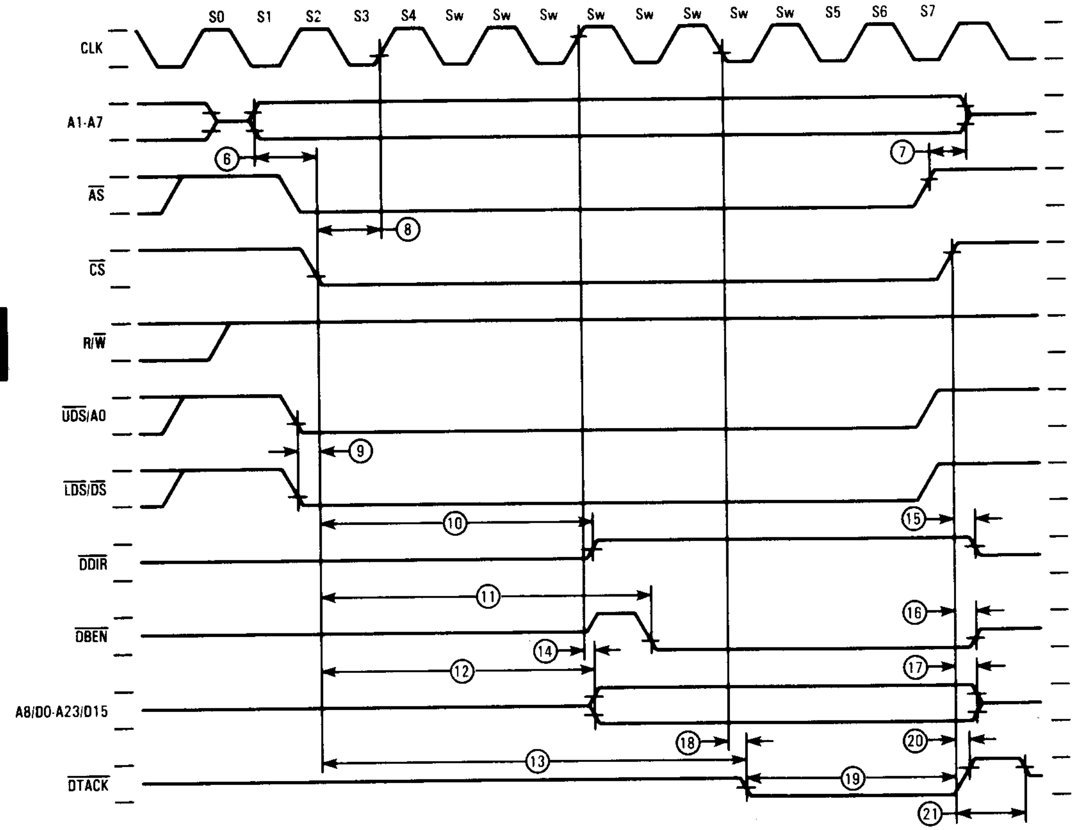
NOTES:
1. These specifications assume that the input setup time for CS is zero, which violates #8, but it is still recognized as asserted.
2. With both channels active these numbers increase by one clock.
3. AS and BG from the MPU are first sampled on the rising clock edge on which BR is asserted. Therefore, if AS is negated and BG is asserted for at least one asynchronous input setup time prior to that clock edge, then the minimum arbitration times will be achieved.
4. These minimum times assume that the two signals have equal resistive and capacitive loading (±20%).
5. When AS and R/W are equally loaded (±10%) AS will be asserted no more than 20 ns before R/W.
6. Minimum timing for single address write cycles occurs with ACK only or with ACK and PCL as READY when PCL is asserted for more than one synchronization delay before the clock edge on which ACK is asserted.
7. Specifications that include a number of clock periods refer to the actual input clock used and not the specified clock minimum or maximum values.
8. These specifications refer to the skew between two output signals that change following different edges of the clock; therefore, the actual value depends on the clock signal that is used. The minimum times are guaranteed for a minimum clock timing (high or low and period).

NOTE

For clarity, specification numbers are shown only once in Figures 16 through 19. However, many specifications apply equally to all four diagrams. For example, specification numbers 54 and 56 are shown only in Figure 16, but apply to Figures 17 through 19 as well. As a guideline, Figure 16 includes all necessary specifications for a dual-address read cycle and Figure 18 includes additional specifications for a single-address read cycle, the same relationship is true for Figures 17 and 19. Thus, the specifications shown in Figure 17 through 19 can be considered to be additions to or substitutions for the specifications shown in Figure 16.

When referring to the timing specifications shown in Figure 13 through 19, it is helpful to remember that all output signals will change states only in response to a specific transition on the CLK input and that all input signals are latched and synchronized on rising edges of the CLK input.

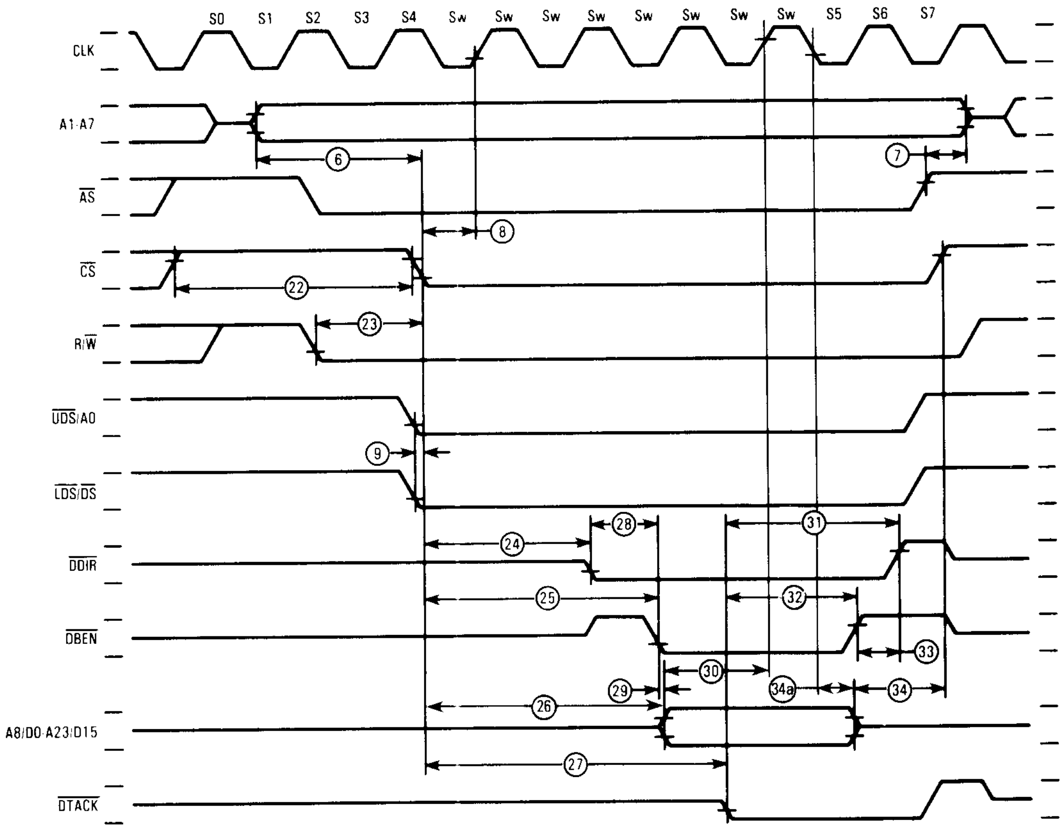
These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 13. MPU Read Cycle Timing Diagram

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 14. MPU Write Cycle Timing Diagram

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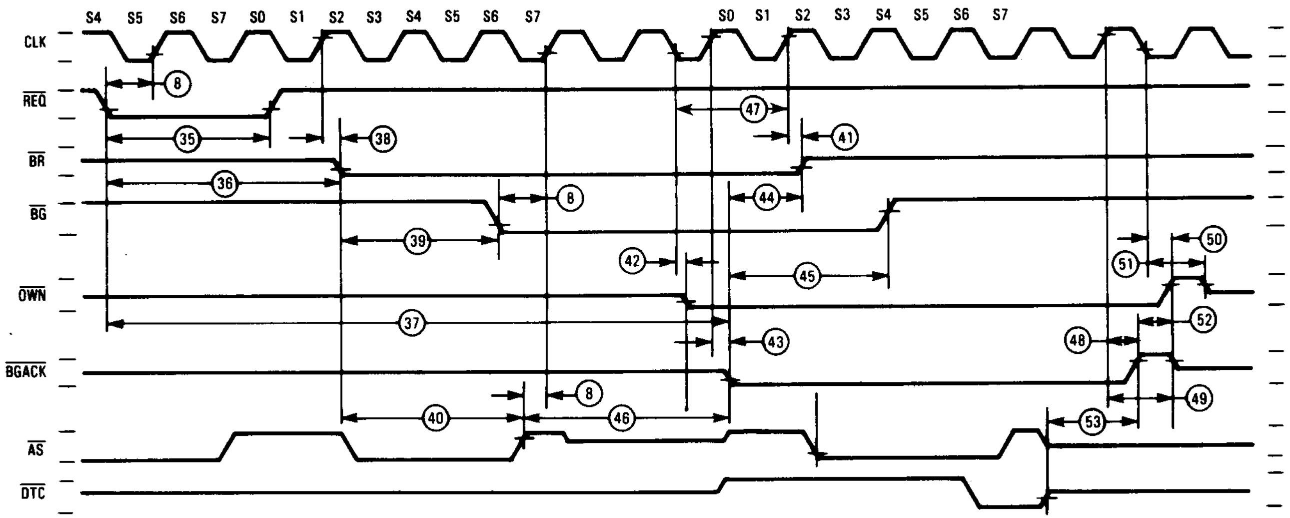
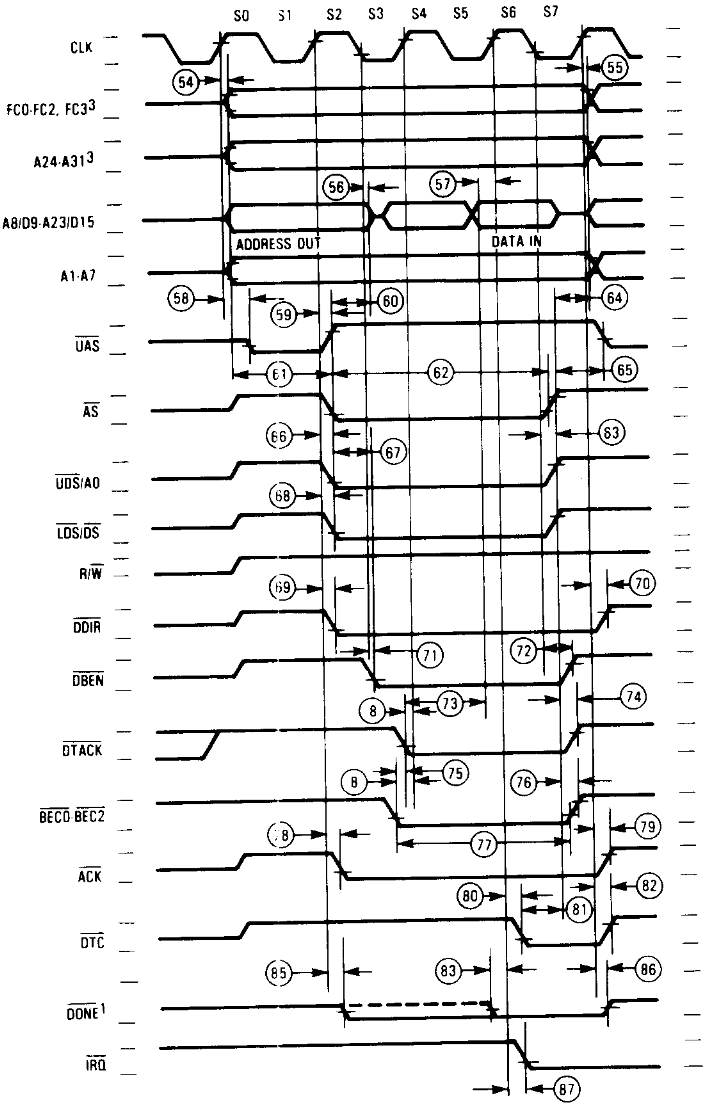
These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 15. Bus Arbitration Timing Diagram

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTES:

1. The solid line illustrates $\overline{DONE}$ as an output, and the dotted line illustrates $\overline{DONE}$ as an input.
2. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.
3. MC68442 only.

Figure 16. Dual Address Read Cycle Timing Diagram

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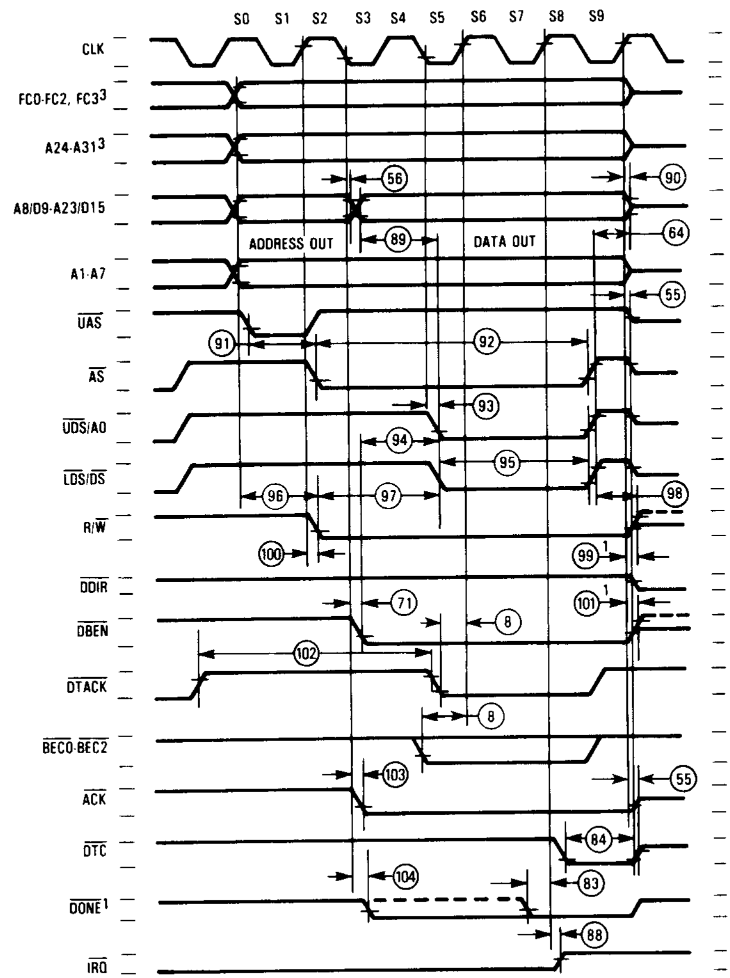
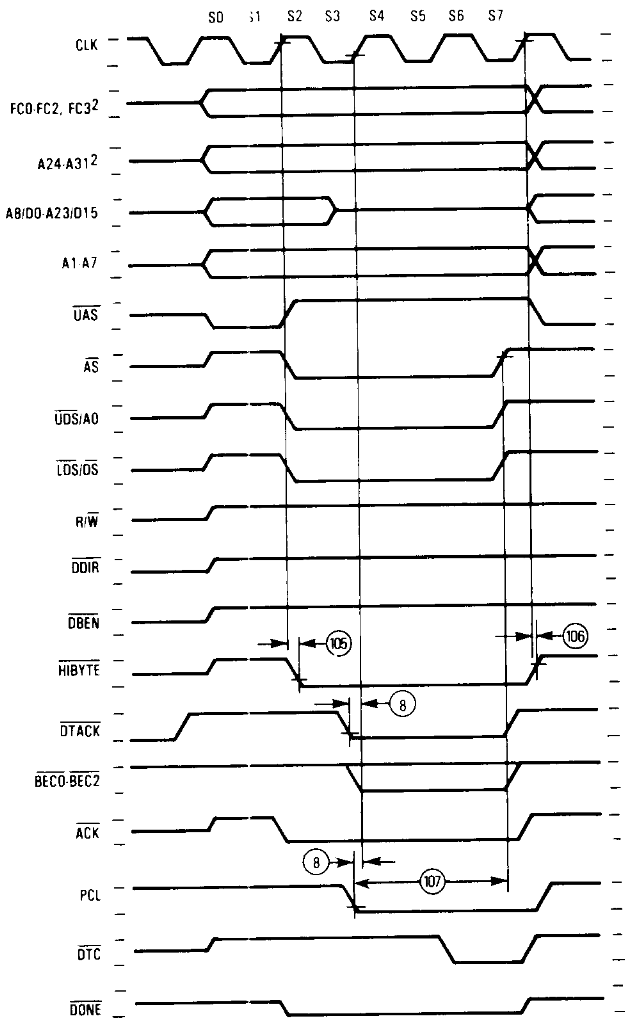
These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTES:
1. Timing specifications #99 and #101 are only applicable when another DDMA bus cycle immediatley follows this one.
2. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.
3. MC68442 only.

Figure 17. Dual Address Write Cycle Timing Diagram

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTES:
1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.
2. MC68442 only.

Figure 18. Single Address Read Cycle Timing Diagram

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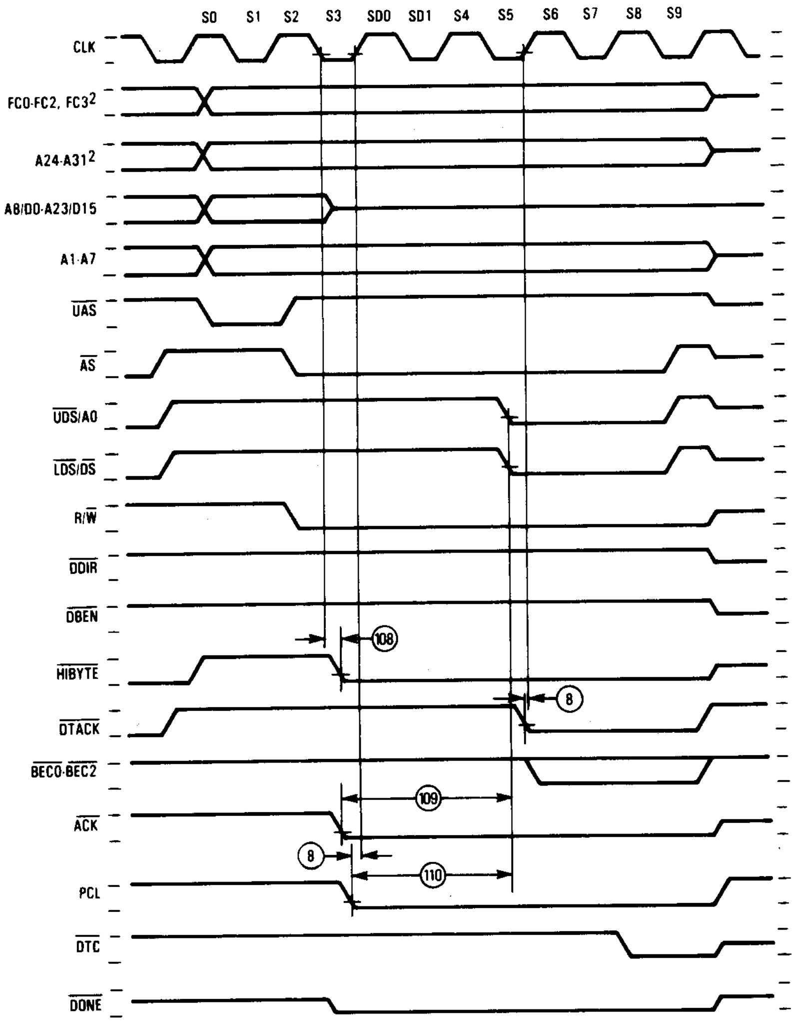
These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



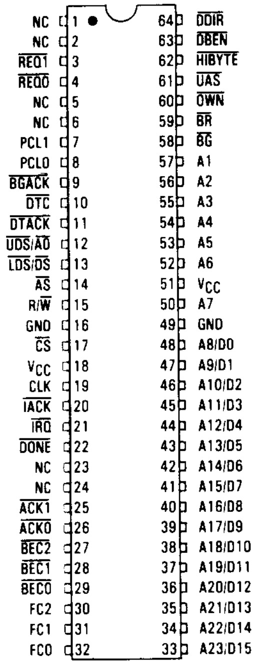
NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.
2. MC68442 only.

Figure 19. Single Address Write Cycle Timing Diagram

PIN ASSIGNMENTS

64-Pin Dual-in-Line Package
MC68440 Only



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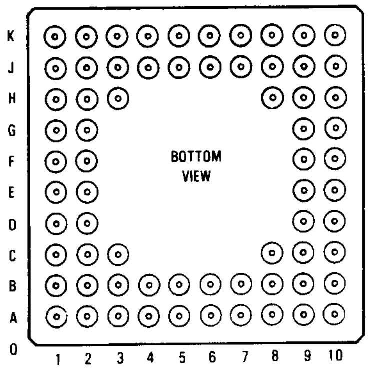
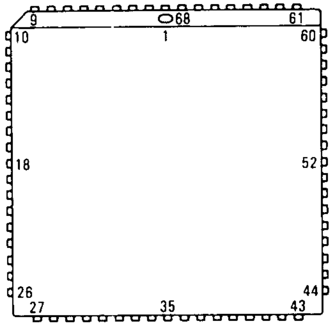
68-Terminal Pin Grid Array
MC68440 and MC68442



Pin Number	Function	
	MC68440	MC68442
A1	NC	FC3
B1	A13/D5	
C1	A11/D3	
D1	A10/D2	
E1	A8/D0	
F1	A7	
G1	A6	
H1	A5	
J1	A3	
K1	NC	A25
K2	$\overline{BR}$	
K3	$\overline{UAS}$	
K4	$\overline{DBEN}$	
K5	NC	A24
K6	NC	A26
K7	$\overline{REQ0}$	
K8	NC	A28
K9	PCL1	
K10	$\overline{DTACK}$	
J10	$\overline{UDS}$/A0	
H10	$\overline{AS}$	
G10	R/$\overline{W}$	
F10	NC	
E10	$\overline{CS}$	
D10	CLK	
C10	$\overline{IACK}$	
B10	NC	A30
A10	$\overline{ACK0}$	
A9	$\overline{BEC1}$	
A8	FC2	
A7	FC1	
A6	A23/D15	
A5	A22/D14	
A4	A20/D12	

Pin Number	Function	
	MC68440	MC68442
A3	A19/D11	
A2	A17/D9	
B2	A15/D7	
C2	A12/D4	
D2	A9/D1	
E2	GND	
F2	V_{CC}	
G2	A4	
H2	A2	
J2	$\overline{BG}$	
J3	$\overline{OWN}$	
J4	$\overline{HIBYTE}$	
J5	$\overline{DDIR}$	
J6	$\overline{REQ1}$	
J7	NC	A29
J8	PCL0	
J9	NC	A27
H9	$\overline{BGACK}$	
G9	$\overline{LDS}/\overline{DS}$	
F9	GND	
E9	V_{CC}	
D9	$\overline{DONE}$	
C9	$\overline{IRQ}$	
B9	NC	A31
B8	$\overline{BEC2}$	
B7	$\overline{BEC0}$	
B6	FC0	
B5	A21/D13	
B4	A18/D10	
B3	A16/D8	
C3	A14/D6	
H3	A1	
H8	$\overline{DTC}$	
C8	$\overline{ACK1}$	

**68-Lead Pastic Leaded
Chip Carrier
MC68440 and MC68442**



Pin Number	Function	
	MC68440	MC68442
1	$\overline{DDIR}$	
2	NC	A25
3	NC	A26
4	NC	A27
5	$\overline{REQ1}$	
6	$\overline{REQ0}$	
7	NC	A28
8	NC	A29
9	$\overline{PCL1}$	
10	$\overline{PCL0}$	
11	$\overline{BGACK}$	
12	$\overline{DTC}$	
13	$\overline{DTACK}$	
14	$\overline{UDS}$/A0	
15	$\overline{LDS}$/$\overline{DS}$	
16	$\overline{AS}$	
17	R/$\overline{W}$	
18	GND	
19	$\overline{CS}$	
20	V_{CC}	
21	CLK	
22	$\overline{IACK}$	
23	$\overline{IRQ}$	
24	$\overline{DONE}$	
25	NC	A30
26	NC	A31
27	$\overline{ACK1}$	
28	$\overline{ACK0}$	
29	$\overline{BEC2}$	
30	$\overline{BEC1}$	
31	$\overline{BEC0}$	
32	NC	FC3
33	FC2	
34	FC1	

Pin Number	Function	
	MC68440	MC68442
35	FC0	
36	A23/D15	
37	A22/D14	
38	A21/D13	
39	A20/D12	
40	A19/D11	
41	A18/D10	
42	A17/D9	
43	A16/D8	
44	A15/D7	
45	A14/D6	
46	A13/D5	
47	A12/D4	
48	A11/D3	
49	A10/D2	
50	A9/D1	
51	A8/D0	
52	NC	
53	GND	
54	A7	
55	V_{CC}	
56	A6	
57	A5	
58	A4	
59	A3	
60	A2	
61	A1	
62	$\overline{BG}$	
63	$\overline{BR}$	
64	$\overline{OWN}$	
65	$\overline{UAS}$	
66	$\overline{HIBYTE}$	
67	$\overline{DBEN}$	
68	NC	A24