TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

8,388,608 WORD × 64 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THL64V8035BTG is a 8,388,608 word by 64 bit dynamic RAM module which assembled 8 pcs of TC5164805BFT/BFTS on the printed circuit board. This module is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

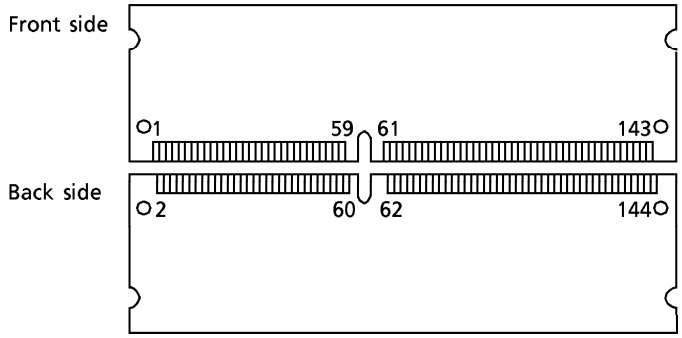
FEATURES

- 8,388,608 word by 64 bit organization
- Fast access time and cycle time

		-4/4S	-5/5S
t_{RAC}	RAS Access Time	40 ns	50 ns
t_{AA}	Column Address Access Time	20 ns	25 ns
t_{CAC}	CAS Access Time	11 ns	13 ns
t_{RC}	Cycle Time	69 ns	84 ns
t_{HPC}	Hyper Page Mode Cycle Time	16 ns	20 ns

- Single power supply of 3.3V±5%
- Low Power
  - 3332mW MAX. Operating (THLxxxxxx−4/4S)
  - 2776mW MAX. Operating (THLxxxxxx−5/5S)
  - 13.9mW MAX. Standby (THLxxxxxx−x)
  - 5.6mW MAX. Standby (THLxxxxxx−xS)
- CAS before RAS refresh, Hidden refresh, EDO (Hyper Page Mode) capability.
- Self Refresh Mode capability (THLxxxxxx−xS)
- All inputs and outputs LVTTL compatible
- 4,096 refresh cycles / 64ms (THLxxxxxx−x)
- 4,096 refresh cycles / 128ms (THLxxxxxx−xS)
- Package THL64V8035ATG : 144 pin 8 byte Small Outline DIMM (Gold Contact, 3.3 V Keying)

PIN CONNECTION



1	V_{SS}	2	V_{SS}	37	DQ8	38	DQ40	73	/OE	74	NC	109	A9	110	A12R
3	DQ0	4	DQ32	39	DQ9	40	DQ41	75	V_{SS}	76	V_{SS}	111	A10R	112	NC
5	DQ1	6	DQ33	41	DQ10	42	DQ42	77	NC	78	NC	113	V_{CC}	114	V_{CC}
7	DQ2	8	DQ34	43	DQ11	44	DQ43	79	NC	80	NC	115	/CAS2	116	/CAS6
9	DQ3	10	DQ35	45	V_{CC}	46	V_{CC}	81	V_{CC}	82	V_{CC}	117	/CAS3	118	/CAS7
11	V_{CC}	12	V_{CC}	47	DQ12	48	DQ44	83	DQ16	84	DQ48	119	V_{SS}	120	V_{SS}
13	DQ4	14	DQ36	49	DQ13	50	DQ45	85	DQ17	86	DQ49	121	DQ24	122	DQ56
15	DQ5	16	DQ37	51	DQ14	52	DQ46	87	DQ18	88	DQ50	123	DQ25	124	DQ57
17	DQ6	18	DQ38	53	DQ15	54	DQ47	89	DQ19	90	DQ51	125	DQ26	126	DQ58
19	DQ7	20	DQ39	55	V_{SS}	56	V_{SS}	91	V_{SS}	92	V_{SS}	127	DQ27	128	DQ59
21	V_{SS}	22	V_{SS}	57	NC	58	NC	93	DQ20	94	DQ52	129	V_{CC}	130	V_{CC}
23	/CAS0	24	/CAS4	59	NC	60	NC	95	DQ21	96	DQ53	131	DQ28	132	DQ60
25	/CAS1	26	/CAS5	61	NC	62	NC	97	DQ22	98	DQ54	133	DQ29	134	DQ61
27	V_{CC}	28	V_{CC}	63	V_{CC}	64	V_{CC}	99	DQ23	100	DQ55	135	DQ30	136	DQ62
29	A0	30	A3	65	NC	66	NC	101	V_{CC}	102	V_{CC}	137	DQ31	138	DQ63
31	A1	32	A4	67	/WE	68	NC	103	A6	104	A7	139	V_{SS}	140	V_{SS}
33	A2	34	A5	69	/RAS0	70	NC	105	A8	106	A11R	141	SDA	142	SCL
35	V_{SS}	36	V_{SS}	71	NC	72	NC	107	V_{SS}	108	V_{SS}	143	V_{CC}	144	V_{CC}

PIN NAMES

A0 to 9, A10R to A12R	Address Inputs
DQ0 to 63	Data Input / Outputs
/RAS0	Row Address Strobe
/CAS0 to 7	Column Address Strobe
/WE	Read / Write Input
/OE	Output Enable
V_{CC}	Power(+ 3.3 V)
V_{SS}	Ground
SCL	Presence Detect Clock
SDA	Serial Data-out
NC	No Connection

SERIAL PRESENCE DETECT

	-4/4S (hex)	-5/5S (hex)	Note
Byte-0	10	10	128 bytes
Byte-1	01	01	256 bytes
Byte-2	02	02	EDO
Byte-3	0D	0D	A_R
Byte-4	0A	0A	A_C
Byte-5	01	01	DIMM Bank
Byte-6	40	40	x64
Byte-7	00	00	—
Byte-8	01	01	LVTTL
Byte-9	28	32	tRAC
Byte-10	0B	0D	tCAC
Byte-11	00	00	Non - Parity
Byte-12	00	00	15.625 μs (Normal)
	83	83	Self Refresh
Byte-13	08	08	x8
Byte-14	00	00	Non - Parity

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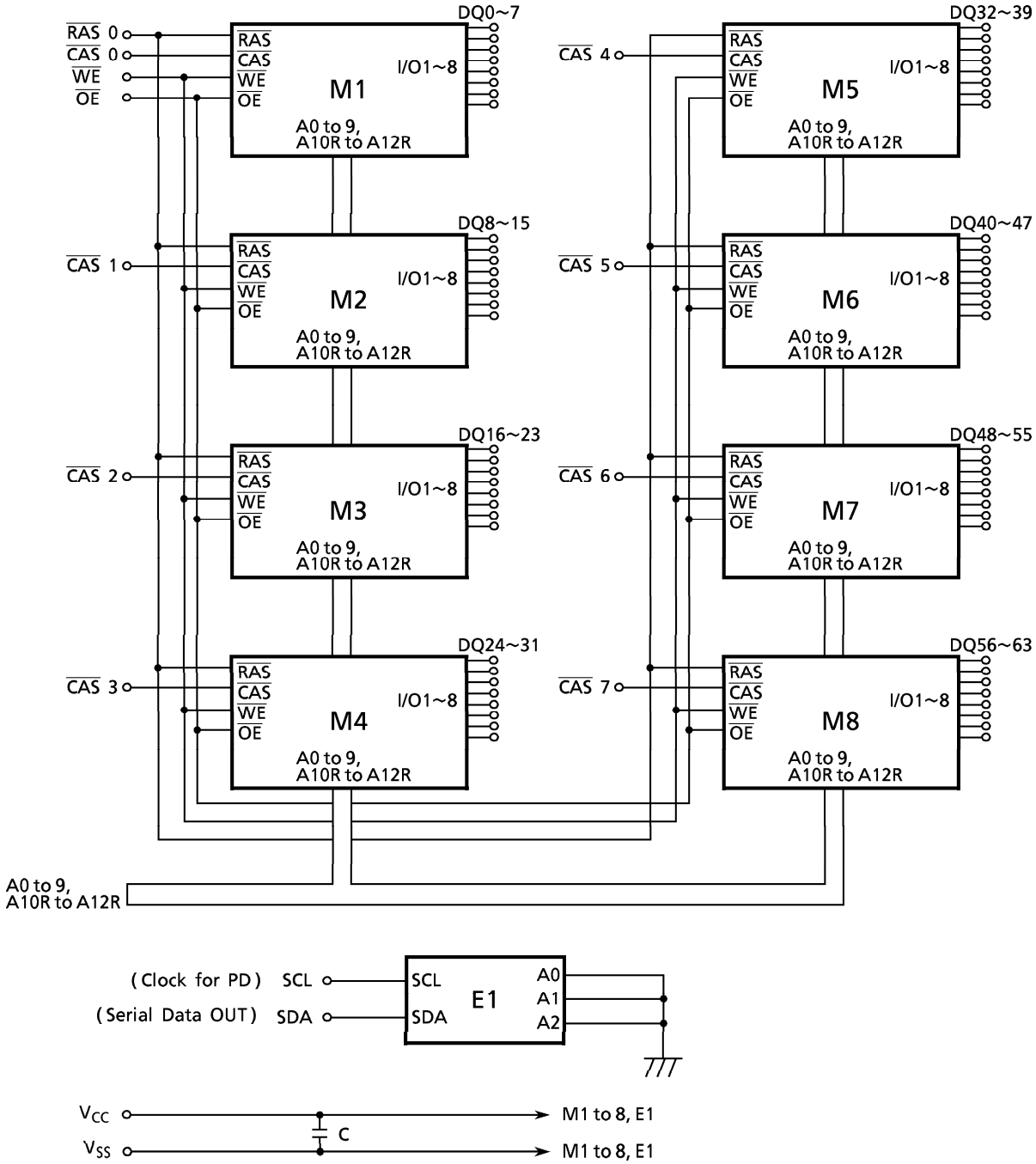
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	$-0.3 \sim V_{CC}+0.3$	V	1
V_{OUT}	Output Voltage	$-0.3 \sim V_{CC}+0.3$	V	1
V_{CC}	Power Supply Voltage	$-0.3 \sim 4.6$	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	−55~125	°C	1
P_D	Power Dissipation	3.7	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	3.13	3.3	3.47	V	2
V_{IH}	Input High Voltage	2.0	−	$V_{CC}+0.3$*	V	2
V_{IL}	Input Low Voltage	−0.3**	−	0.8	V	2

* $V_{CC}+1.2V$ at pulse width ≦ 20ns (pulse width is measured at V_{CC})

** −1.2V at pulse width ≦ 20ns (pulse width is measured at V_{SS})

CAPACITANCE(V_{CC} = 3.3V ± 5%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 to A9, A10R to A12R)	−	T.B.D.	pF
C_{I2}	Input Capacitance ($\overline{WE}$, $\overline{OE}$)	−	T.B.D.	pF
C_{I3}	Input Capacitance ($\overline{RAS0}$)	−	T.B.D.	pF
C_{I4}	Input Capacitance ($\overline{CAS0}$ to $\overline{CAS7}$)	−	T.B.D.	pF
C_{DQ}	I/O Capacitance (DQ0 to 63)	−	T.B.D.	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V ± 5%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THLxxxxxx-4/4S	–	680	mA	3, 4, 5
		THLxxxxxx-5/5S	–	560		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	8	mA	
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, Address Cycling: t_{HPC} = t_{HPC} MIN.)	THLxxxxxx-4/4S	–	720	mA	3, 4, 5
		THLxxxxxx-5/5S	–	600		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)	THLxxxxxx-x	–	4	mA	
		THLxxxxxx-xS	–	1.6		
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THLxxxxxx-4/4S	–	960	mA	3, 5
		THLxxxxxx-5/5S	–	800		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$, $\overline{WE}$, A0~9,A10R~12R = V_{CC}-0.2V or 0.2V, I/O1~I/O16 = V_{CC}-0.2V, 0.2V or Hi-Z : t_{RC} = 31.2μs t_{RAS} = t_{RAS} MIN~300ns)	THLxxxxxx-xS	–	4	mA	
I_{CCS}	SELF REFRESH CURRENT Average Power Supply Current, Self Refresh Mode ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, $\overline{OE}$, $\overline{WE}$, A0~9,A10R~12R = V_{CC}-0.2V or 0.2V, I/O1~I/O16 = V_{CC}-0.2V, 0.2V or Hi-Z)	THLxxxxxx-xS	–	3.2	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦V_{CC}, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦V_{CC})		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 2mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 3.3V ± 5%, Ta = 0~70°C)

Please refer to The DRAM MODULE AC CHARACTERISTICS No.44

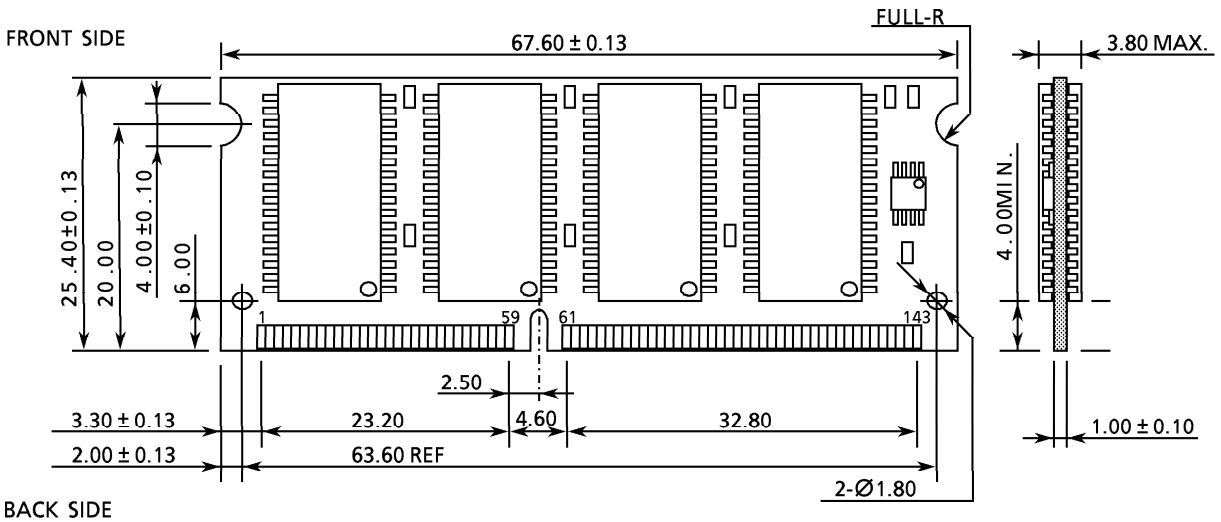
SERIAL PRESENCE DETECT AC OPERATING CONDITIONS

Please refer to The SERIAL PRESENCE DETECT AC CHARACTERISTICS No. 100

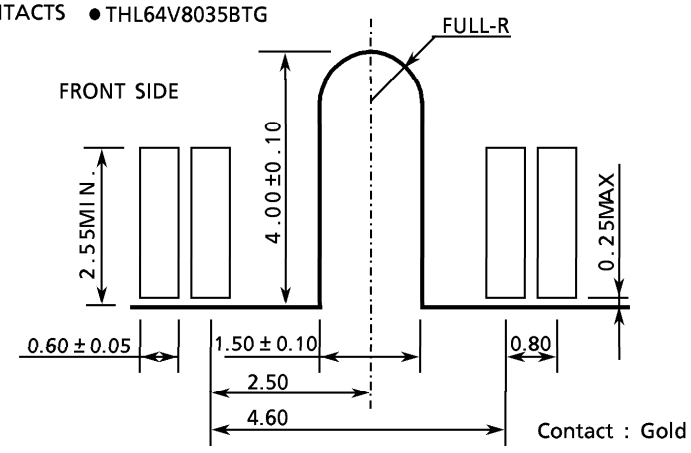
OUTLINE DRAWING

THL64V8035BTG

Unit : mm



DETAIL OF CONTACTS ● THL64V8035BTG



DRAM MODULE
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.44

TC5164405BJ/BFT/BJS/BFTS	USING MODULE
TC5165405BJ/BFT/BJS/BFTS	USING MODULE
TC5164805BJ/BFT/BJS/BFTS	USING MODULE
TC5165805BJ/BFT/BJS/BFTS	USING MODULE
TC5164165BFT/BFTS	USING MODULE
TC5165165BFT/BFTS	USING MODULE

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AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	-40		-50		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	69	–	84	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	92	–	111	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	40	–	50	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	11	–	13	ns	9, 14
t_{AA}	Access Time from Column Address	–	20	–	25	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	22	–	28	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	11	0	13	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	25	–	30	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	40	10,000	50	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	6	–	8	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Hyper Page Mode)	22	–	28	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	30	–	35	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	6	10,000	8	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	29	12	37	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	8	20	10	25	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	6	–	8	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	6	–	8	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	6	–	8	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	6	–	8	–	ns	
t_{WP}	Write Command Pulse Width	6	–	8	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	6	–	8	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	6	–	8	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	6	–	8	–	ns	12

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	-40		-50		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{REF}	Refresh Period	–	64	–	64	ms	
t_{REF}	Refresh Period (Self Refresh)	–	128	–	128	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	26	–	30	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	55	–	67	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	35	–	42	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	37	–	45	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	6	–	8	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	11	–	13	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	11	–	13	–	ns	
t_{OLZ}	$\overline{OE}$ to output in Low-Z	0	–	0	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	11	0	13	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	6	–	8	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RNCD}	$\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode)	40	–	50	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	16	–	20	–	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	47	–	57	–	ns	
t_{COH}	Output Data Hold Time	5	–	5	–	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	11	0	13	ns	10, 16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	11	0	13	ns	10
t_{WED}	$\overline{WE}$ to Data Delay	11	–	13	–	ns	
t_{OE}	$\overline{OE}$ Pulse Width	11	–	13	–	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	6	–	8	–	ns	
t_{CPO}	$\overline{CAS}$ to $\overline{OE}$ Precharge Time	5	–	5	–	ns	
t_{OCH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$	6	–	8	–	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	100	–	100	–	μs	
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self refresh)	69	–	84	–	ns	
t_{CHS}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self refresh)	-50	–	-50	–	ns	

NOTES:

1. Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on the cycle rate.
4. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while $\overline{RAS}=V_{IL}$. In the case of I_{CC4}, it can be changed once at most during a Hyper Page Mode cycle (t_{HPC}).
6. An initial pause of 200μs is required after power-up followed by a minimum of eight $\overline{RAS}$-Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles instead of eight $\overline{RAS}$-Only refresh cycles is required.
7. AC measurements assume $t_T=2$ns.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the V_{IH} and V_{IL} levels.
9. This is measured with a load equivalent to 100pF at V_{OH} = 2.0V (I_{OUT} = −2mA), V_{OL} = 0.8V (I_{OUT} = 2mA).
10. t_{OFF} (max), t_{OEZ} (max), t_{REZ} (max) and t_{WEZ} (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of $\overline{CAS}$ in Early Write cycles and to the leading edge of $\overline{WE}$ in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then the access time is determined by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then the access time is determined by t_{AA}.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the output goes open circuit when $\overline{CAS}$ goes high (t_{OFF}).
    If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the output goes open circuit when $\overline{RAS}$ goes high (t_{REZ}).

DATA-OUT HI-Z CONTROL LOGIC

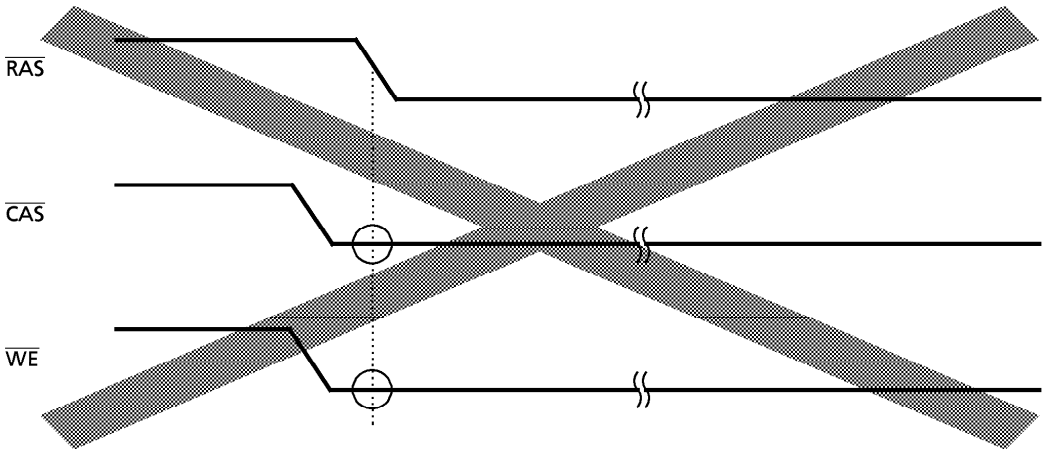
$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
H	↑	L	H	t_{OFF}
↑	H	L	H	t_{REZ}
L	L	↑	H	t_{OEZ}
L	H	L	↓	t_{WEZ}

DATA-OUT LO-Z CONTROL LOGIC

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
L	↓	L	H	t_{CLZ}
L	L	↓	H	t_{OLZ}
L	L	↓↑	H	t_{OLZ}

CAUTION

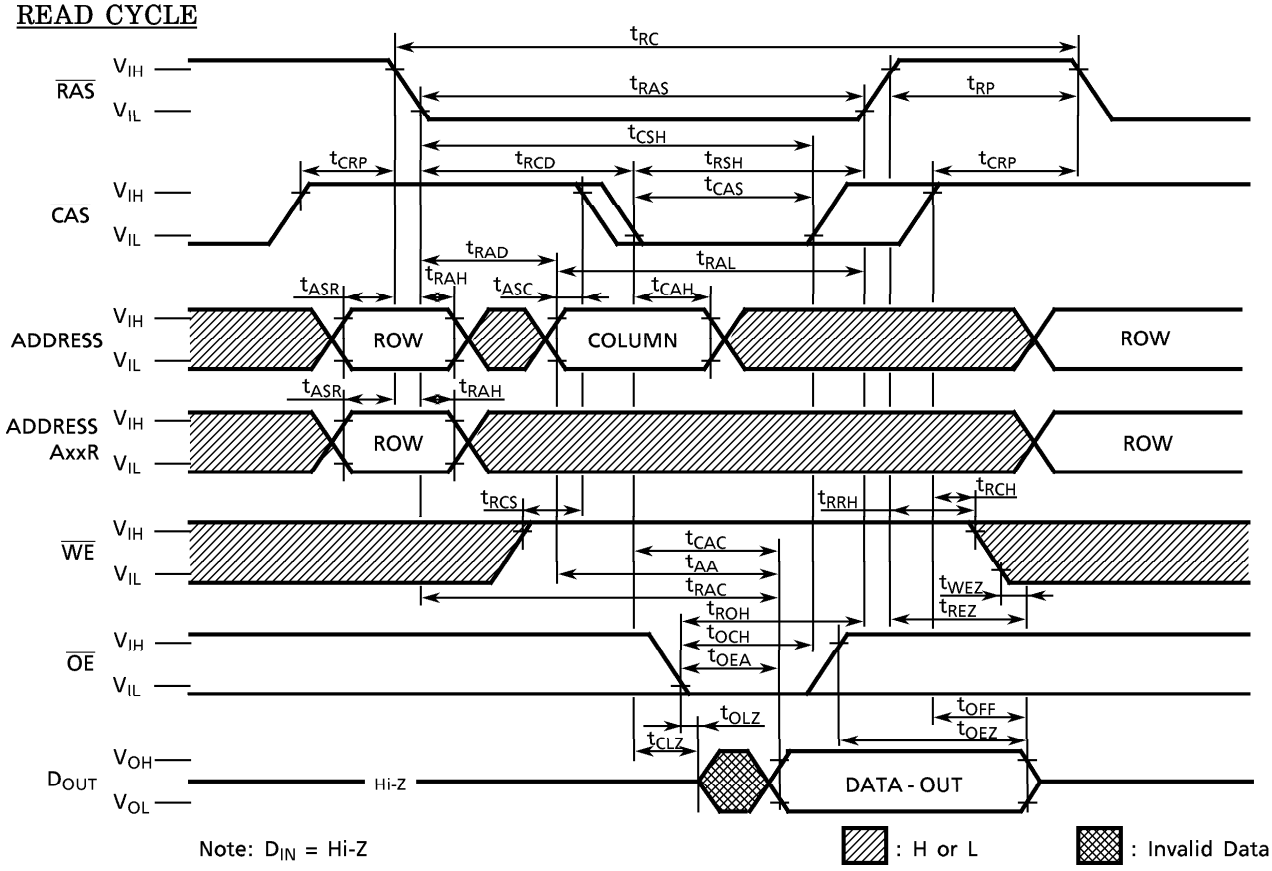
The WCBR ($\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.



WCBR timing

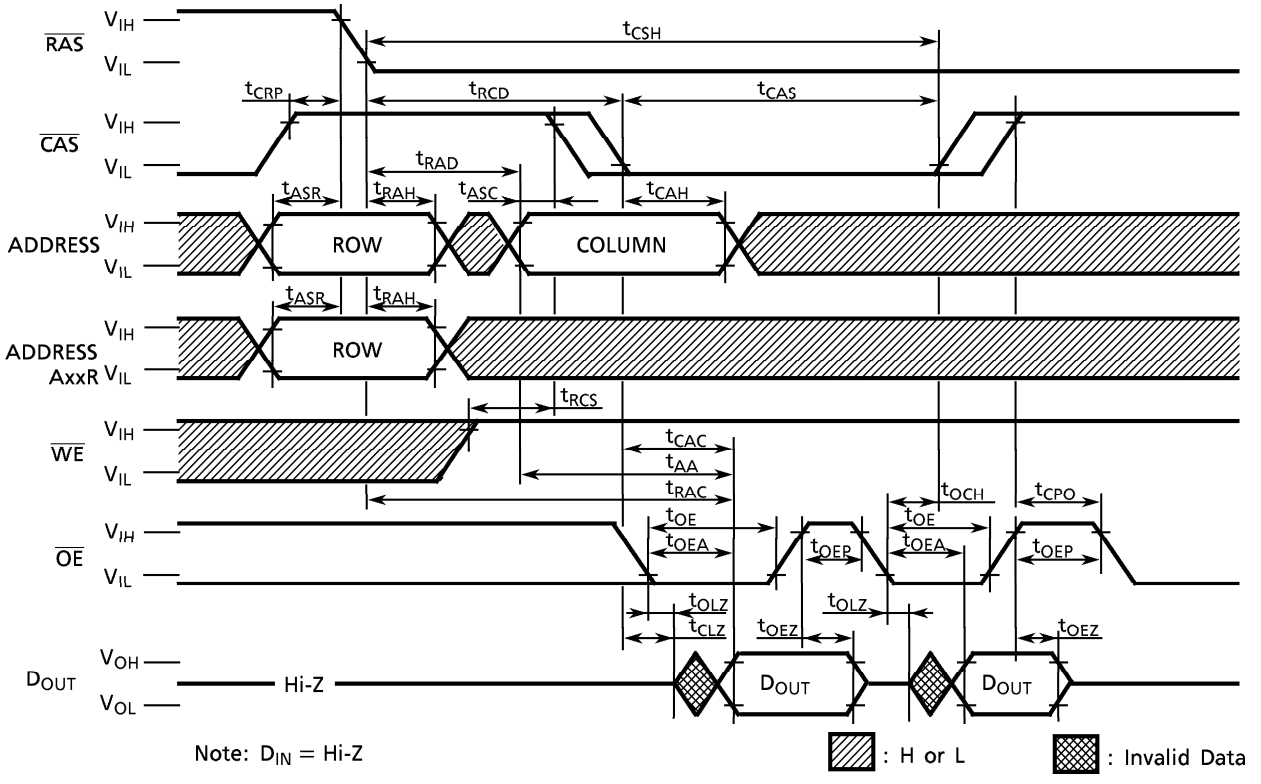
TIMING DIAGRAMS

READ CYCLE



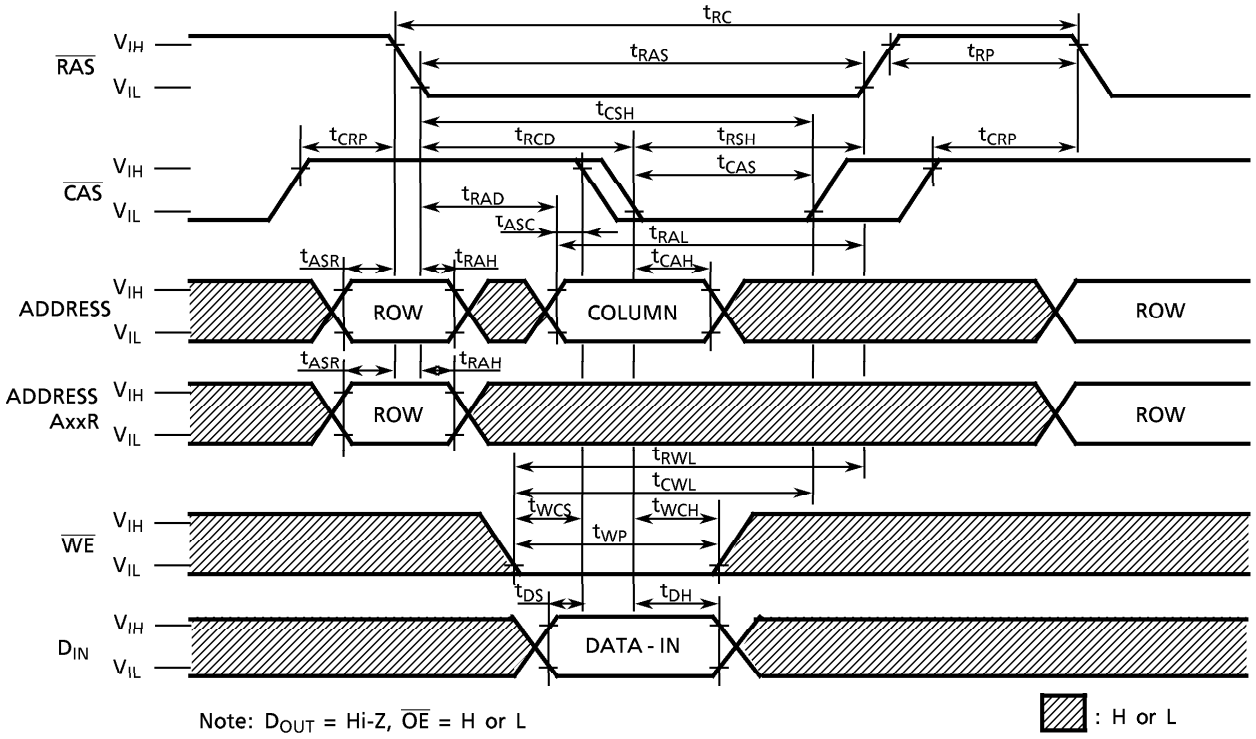
Note: D_{IN} = Hi-Z : H or L : Invalid Data

$\overline{OE}$-CONTROLLED READ CYCLE



Note: D_{IN} = Hi-Z : H or L : Invalid Data

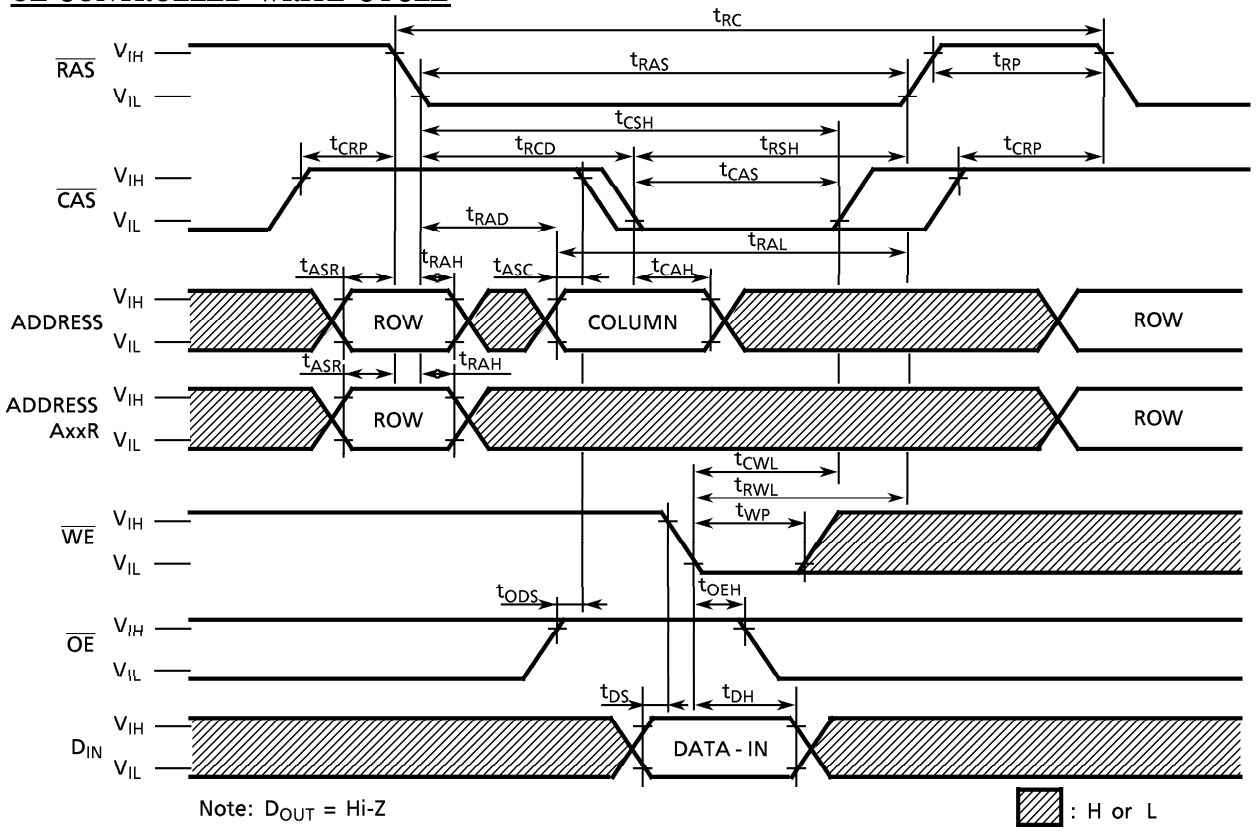
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z, $\overline{OE}$ = H or L

: H or L

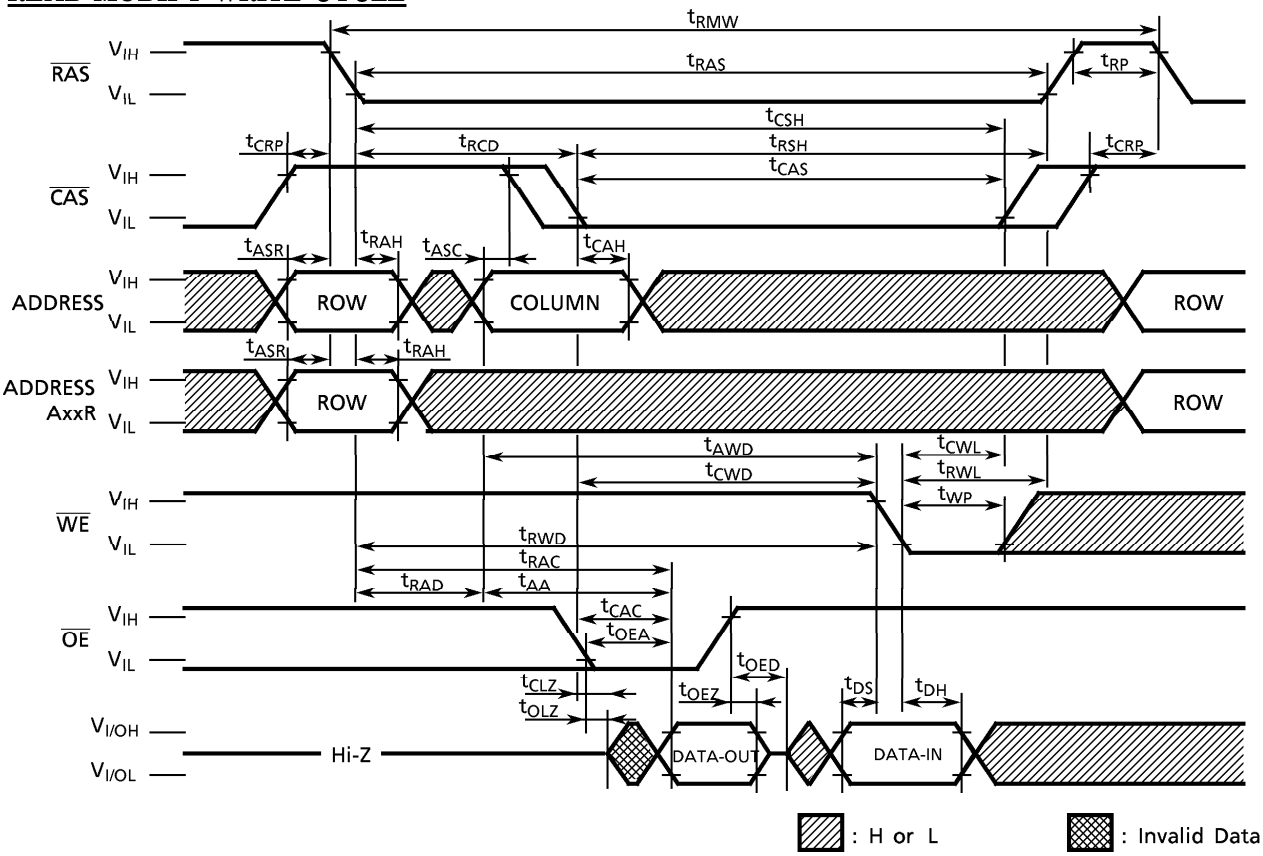
$\overline{OE}$-CONTROLLED WRITE CYCLE



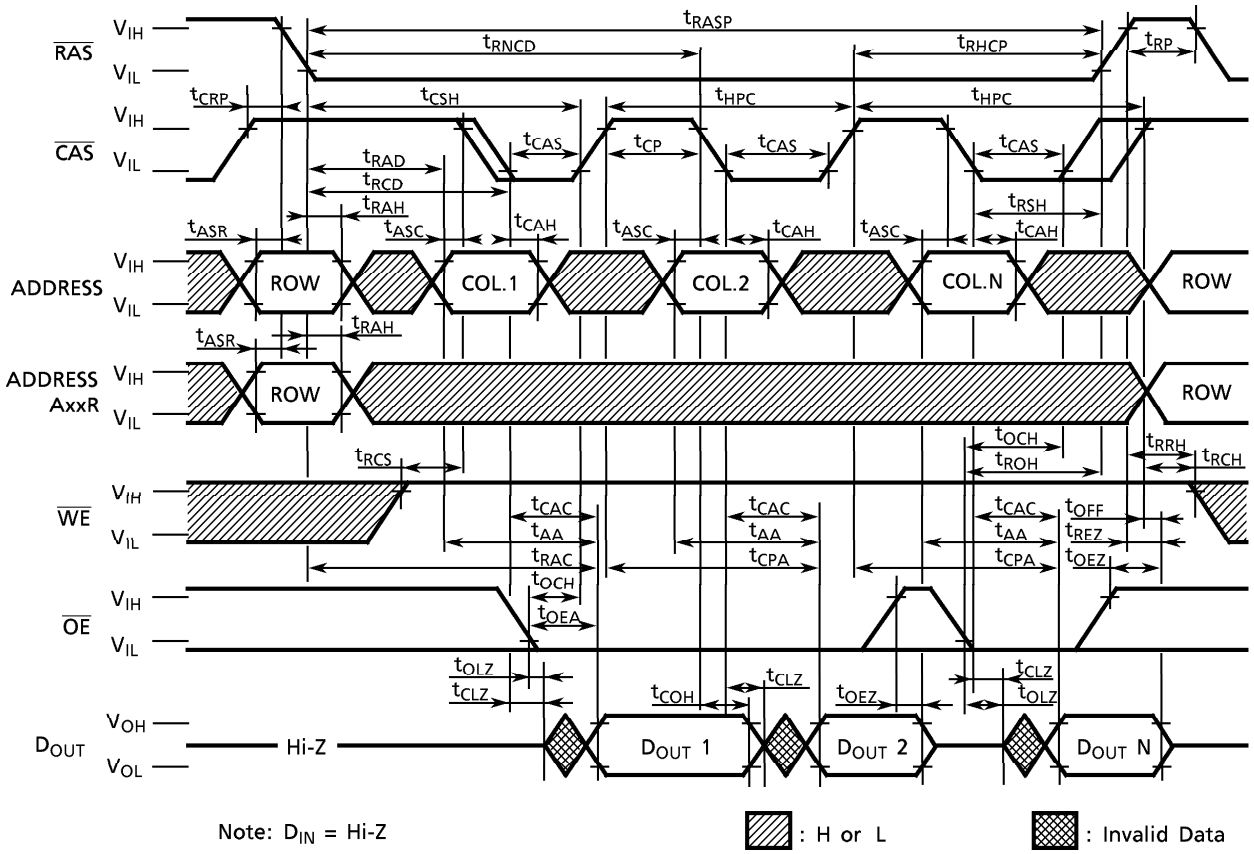
Note: D_{OUT} = Hi-Z

: H or L

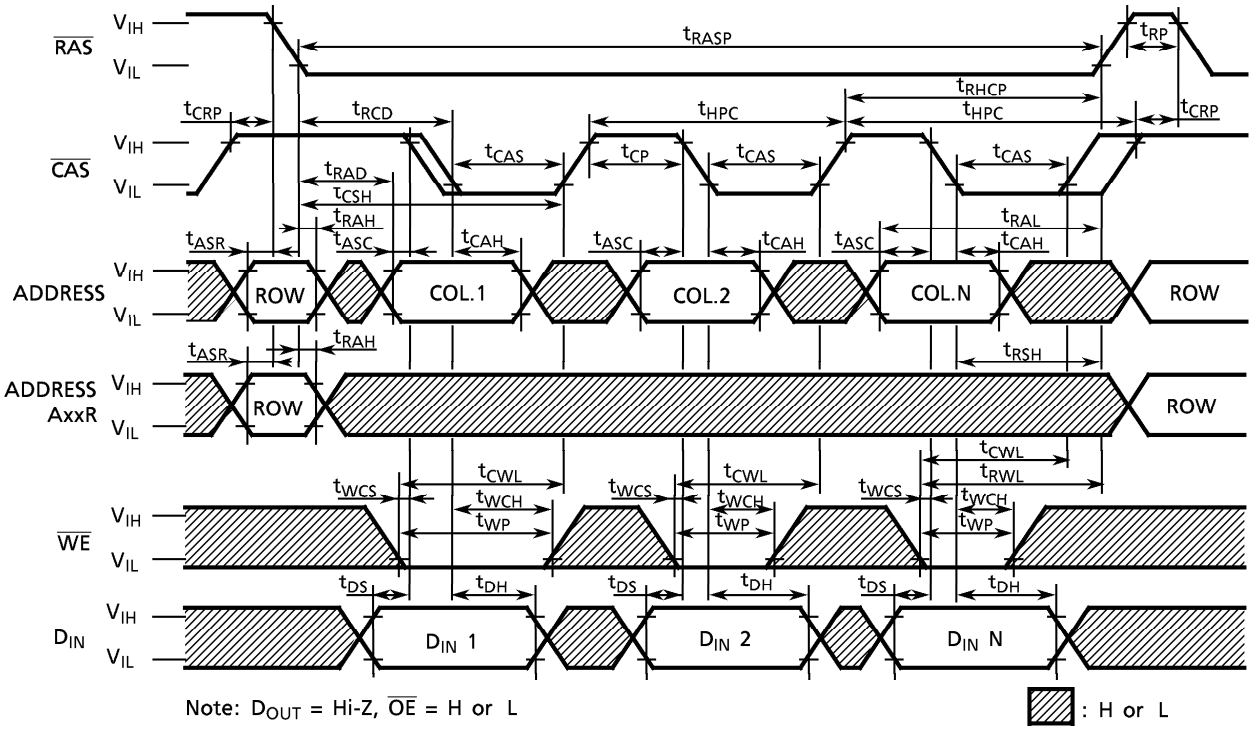
READ-MODIFY-WRITE CYCLE



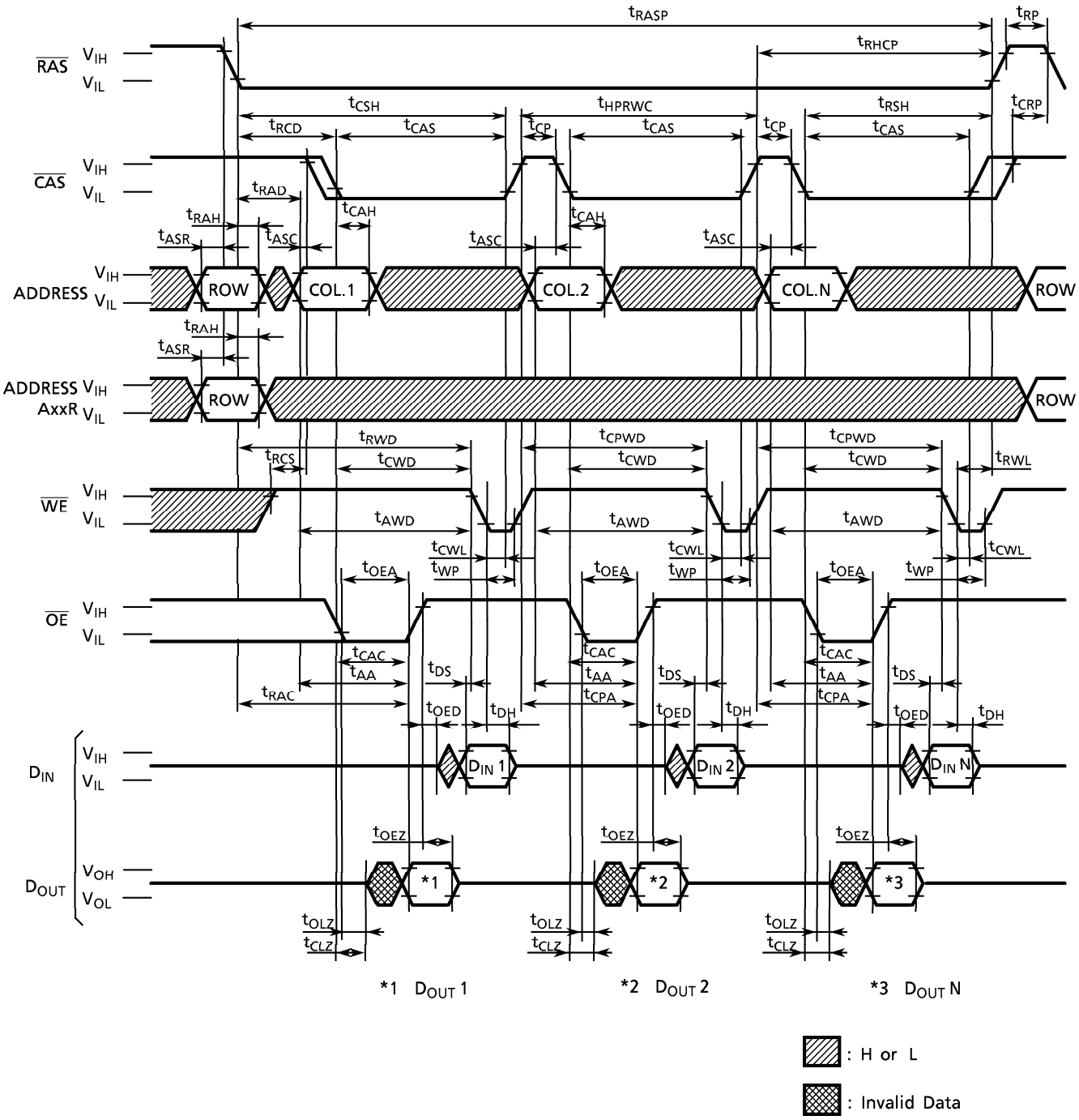
HYPER PAGE MODE READ CYCLE



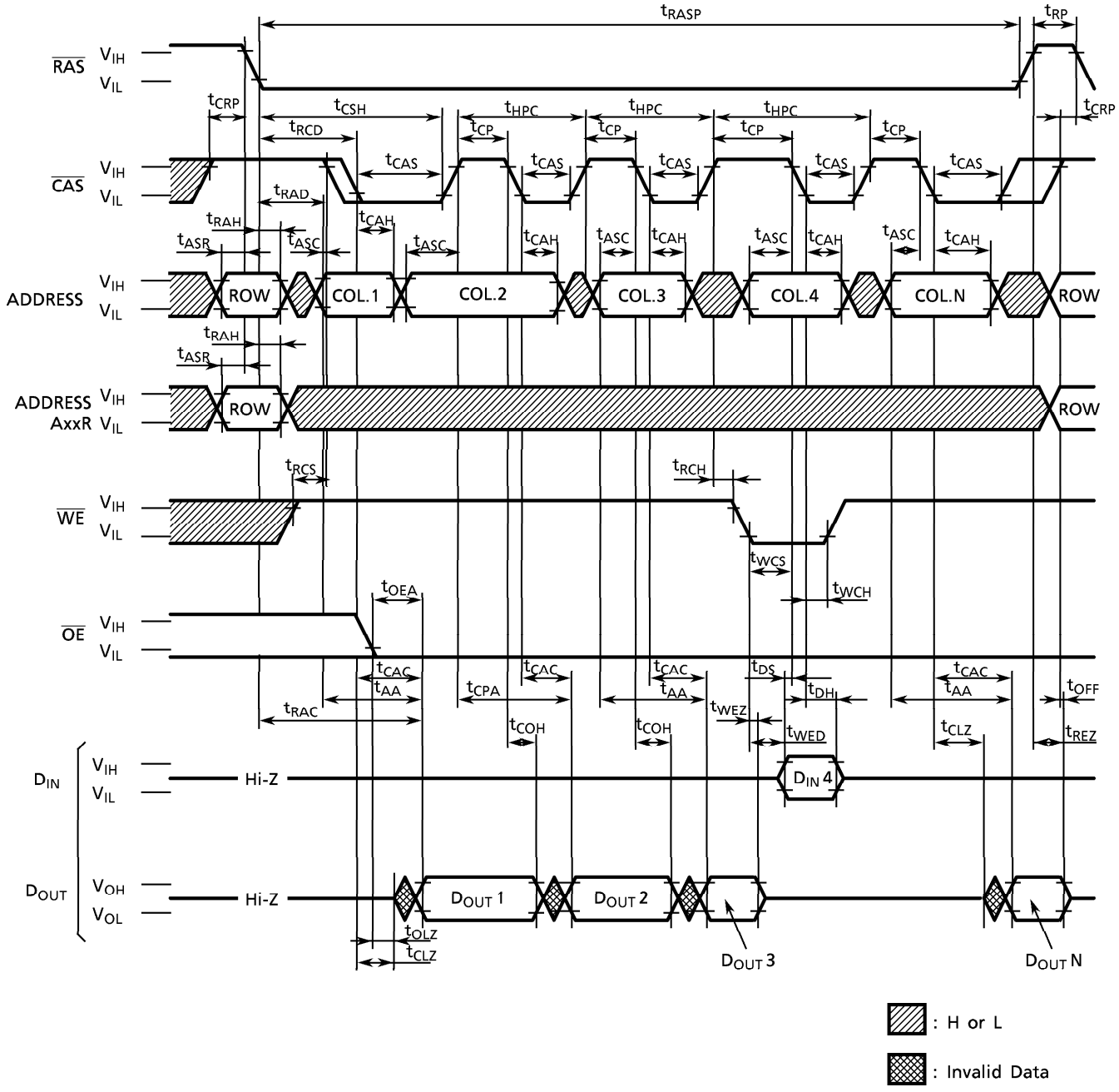
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



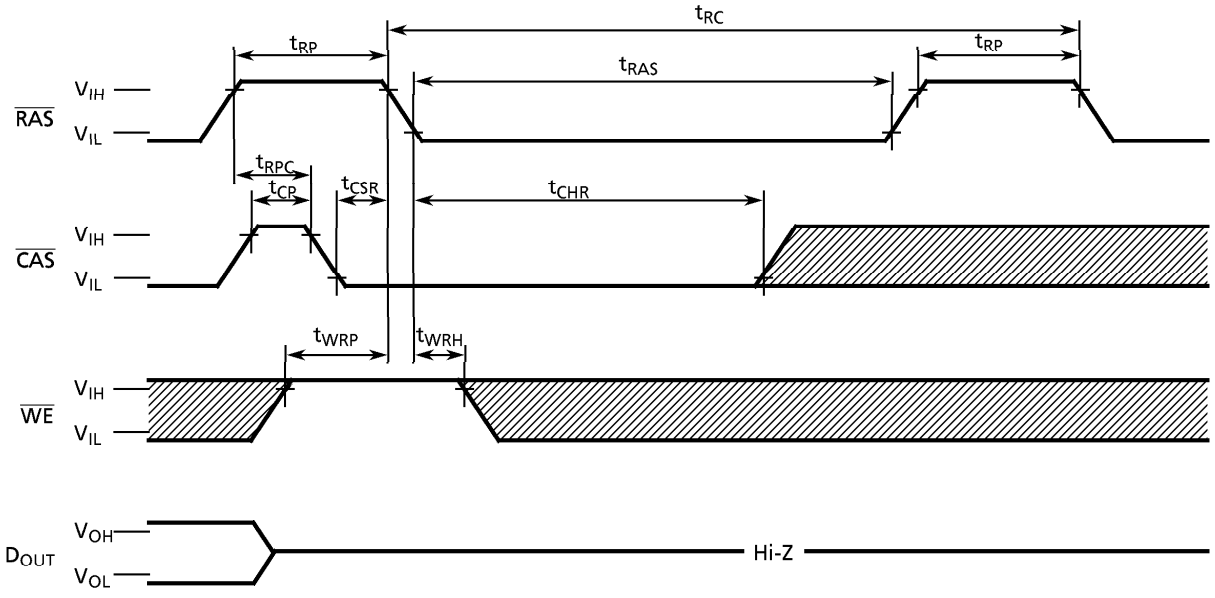
HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE READ-WRITE MIXED CYCLE



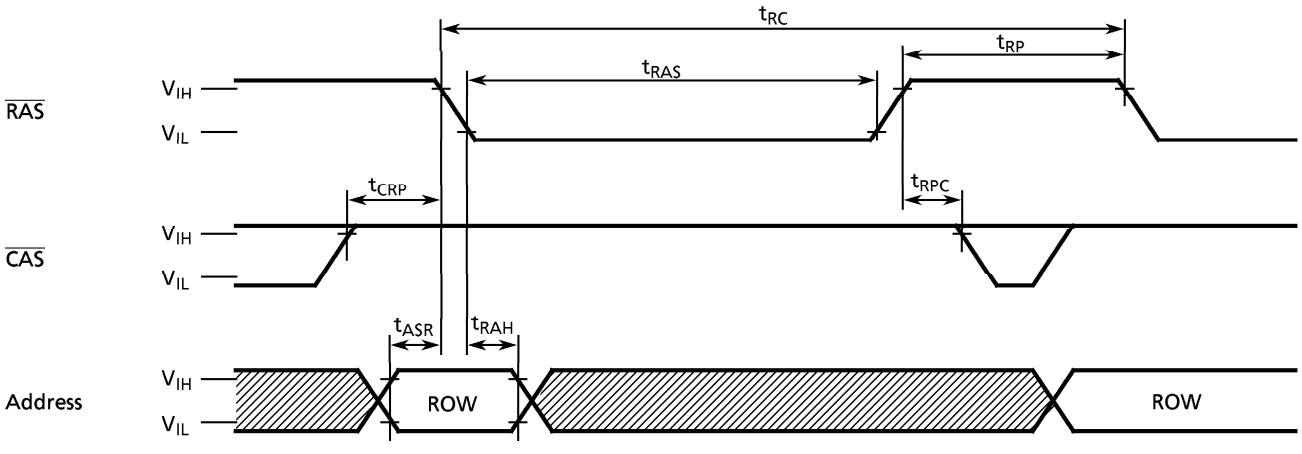
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, ADDRESS = H or L

▨ : H or L

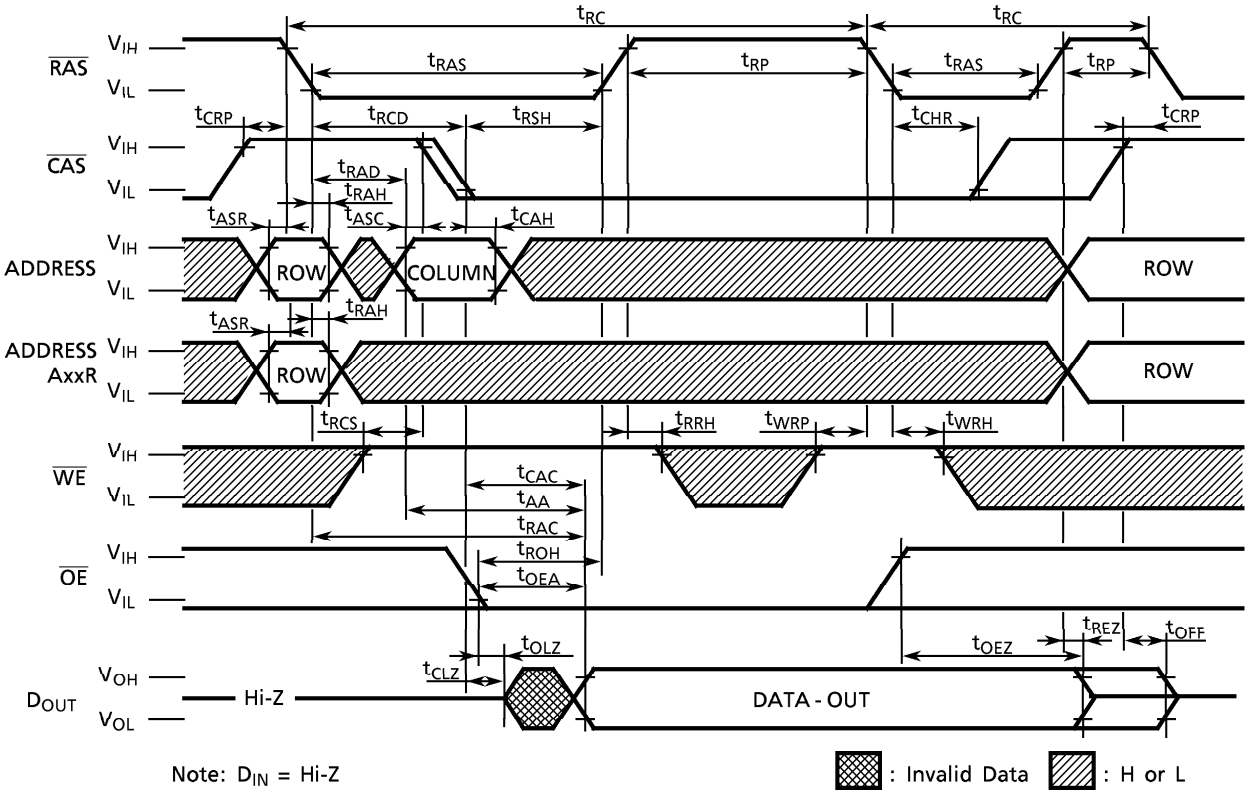
$\overline{RAS}$-ONLY REFRESH CYCLE



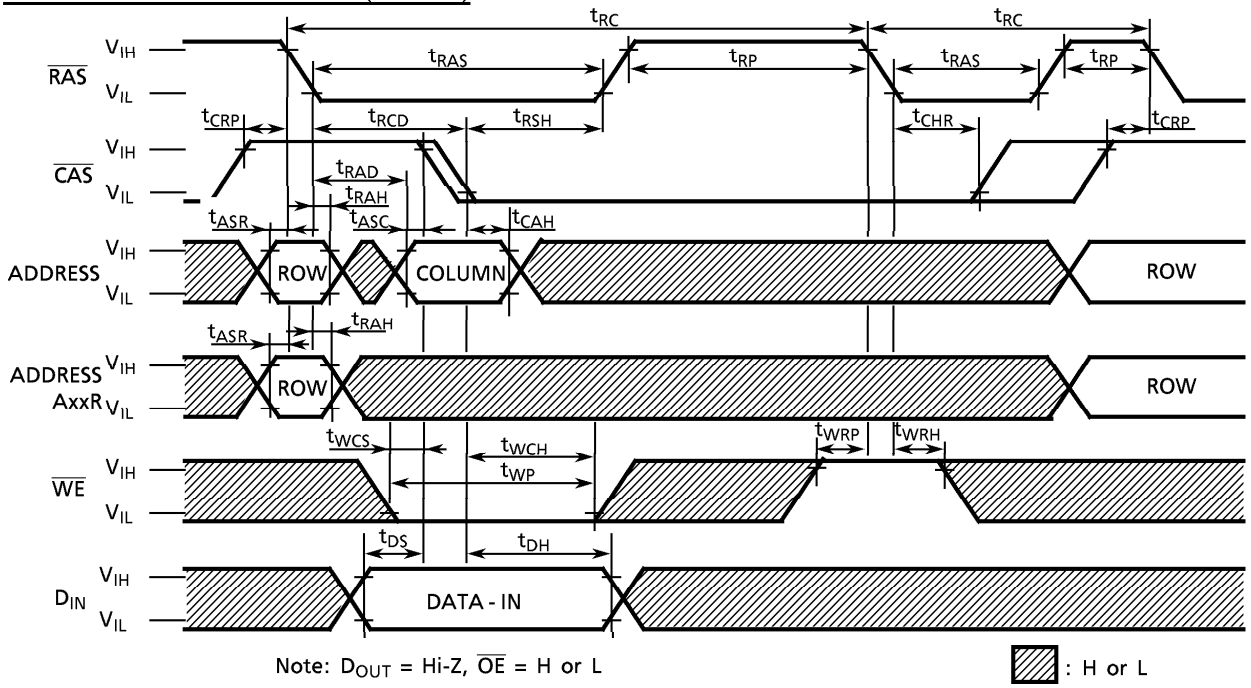
Note: $\overline{WE}$, $\overline{OE}$ and D_{IN} = H or L

▨ : H or L

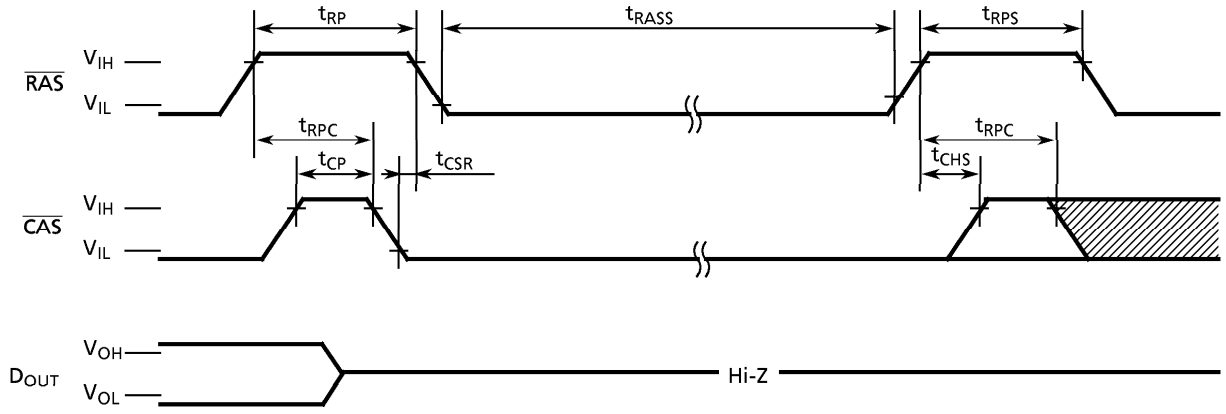
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF-REFRESH CYCLE (THL64VxxxxBTG-xS only)



Note: D_{IN}, $\overline{WE}$, $\overline{OE}$, ADDRESS = H or L

: H or L

SERIAL PRESENCE DETECT AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.100

961001EBA1

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DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ± 0.15 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{IH}	Input High Voltage	V_{CC} × 0.7	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage	–0.3	V_{CC} × 0.3	V	
V_{OL}	Output Low Voltage (I_{OL} = 200 μA)	–	0.4	V	1

Note:

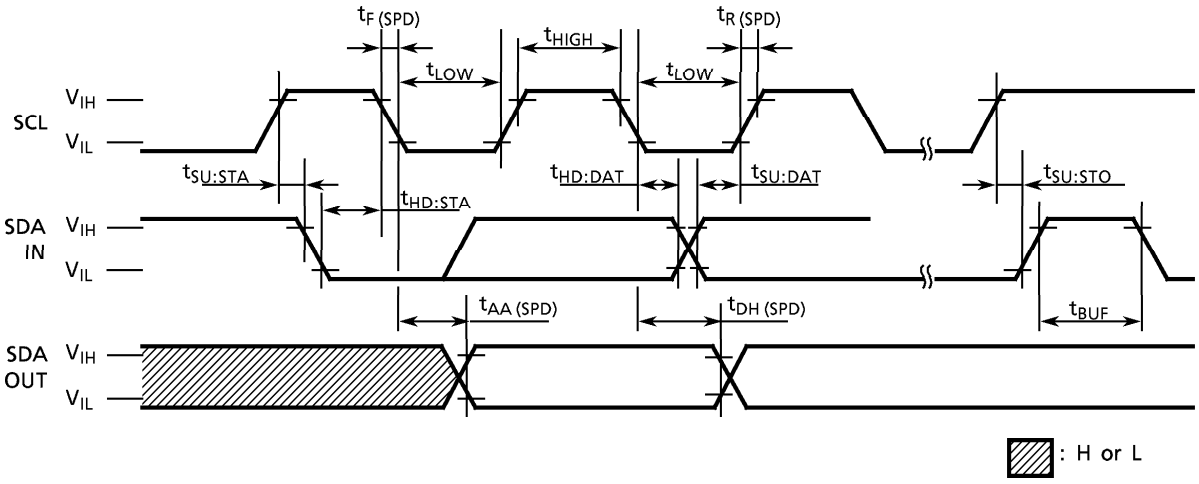
1. Output Load: 1TTL Gate and C_L = 100 pF

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

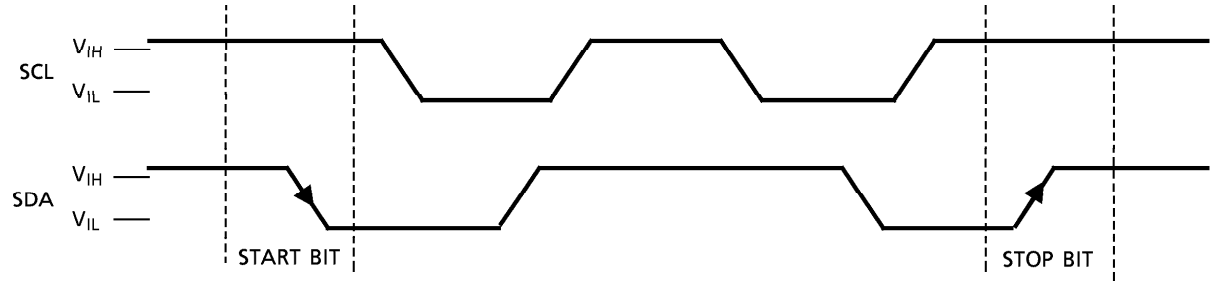
SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{SCL}	SCL Clock Frequency	–	80	KH_Z	
t_{LOW}	Clock Low Period	6.7	–	μs	
t_{HIGH}	Clock High Period	4.5	–	μs	
$t_{AA\ (SPD)}$	SCL Low to SDA Data Out Valid	0.3	7.0	μs	
$t_{HD\ :\ STA}$	Start Condition Hold Time	4.5	–	μs	
$t_{SU\ :\ STA}$	Start Condition Set-up Time (for a Repeated Start Condition)	6.7	–	μs	
$t_{SU\ :\ STO}$	Stop Condition Set-up Time	6.7	–	μs	
$t_{HD\ :\ DAT}$	Data-in Hold Time	0	–	μs	
$t_{SU\ :\ DAT}$	Data-in Set-up Time	500	–	ns	
$t_{DH\ (SPD)}$	Data-out Hold Time	300	–	ns	
$t_{R\ (SPD)}$	SDA and SCL Rise Time	–	1	μs	
$t_{F\ (SPD)}$	SDA and SCL Fall Time	–	300	ns	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7	–	μs	

TIMING DIAGRAMS

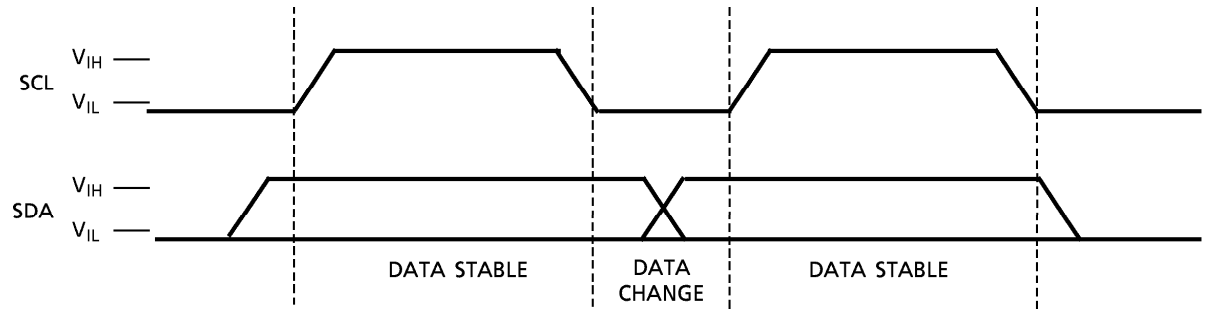
BUS TIMING



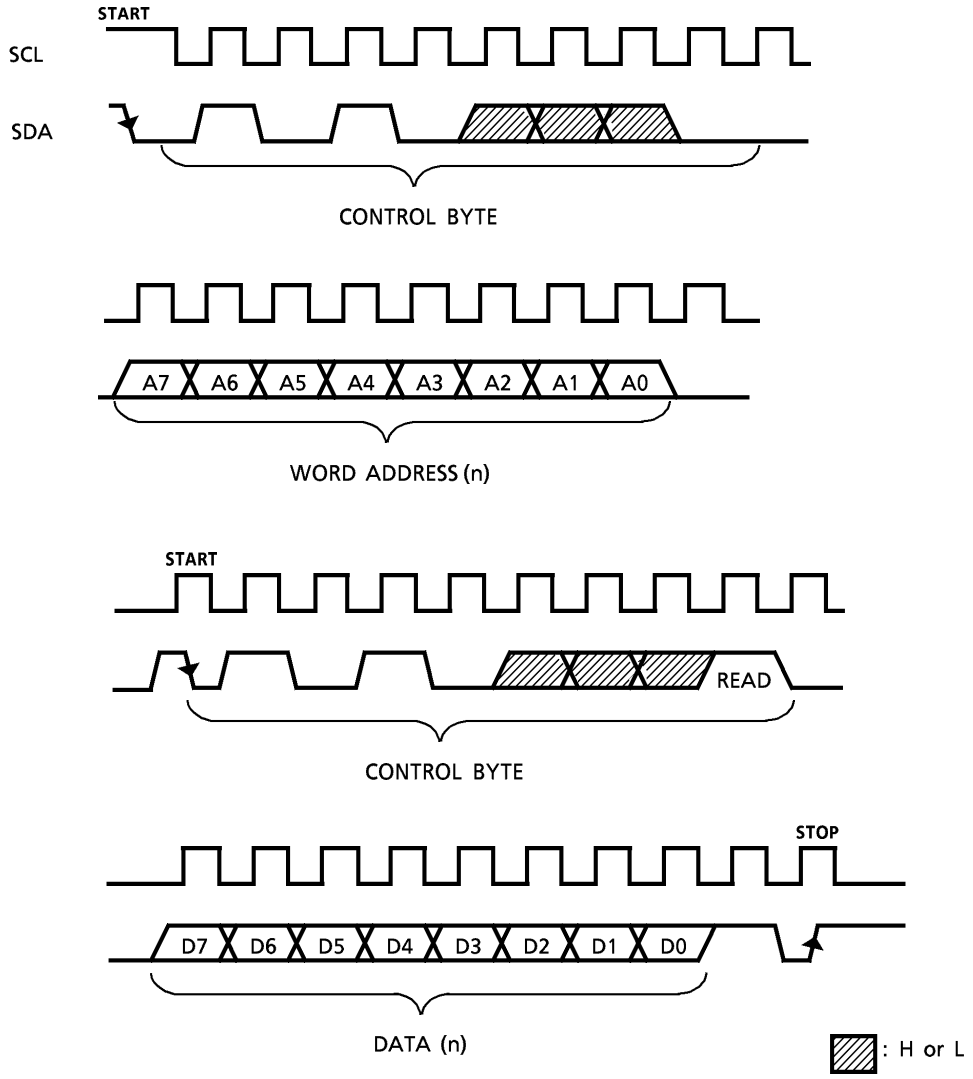
DEFINITION OF START AND STOP



DATA VALIDITY

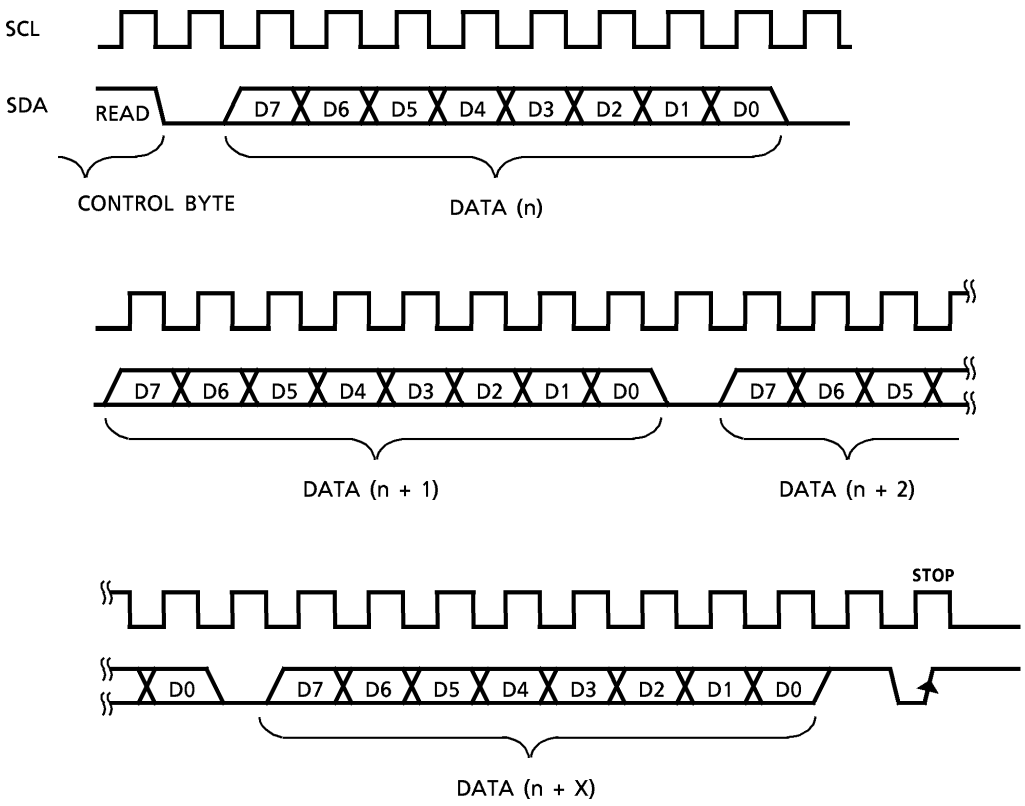


RANDOM READ



NOTE: Random read operations allow the master to access Serial PD DATA in a random manner.
To perform this type of read operation, first the word address must be set. (Dummy Write Operation)
After the word address is sent, the master generates a start condition following the acknowledge.
Then the master issues the control byte again but with READ bit set to a one.
E^2PROM will then issue an acknowledge and transmits the eight bit data word.

SEQUENTIAL READ



NOTE: Sequential reads can be initiated as random access read. The first word is transmitted in the same manner as the other read mode; however, the master now responds with an acknowledge, indicating it requires additional data.
E^2PROM continues to output data for each acknowledge received.
The read operation is terminated by generating a stop condition.