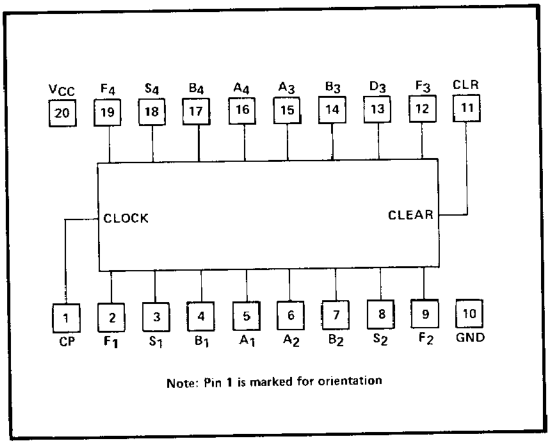
Quad Serial Adder/Subtractor

FEATURES.

- Four Independent Adder/Subtractors
- Use with Two's Complement Arithmetic
- Magnitude Only Addition/Subtraction
- Advanced Low-Power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883



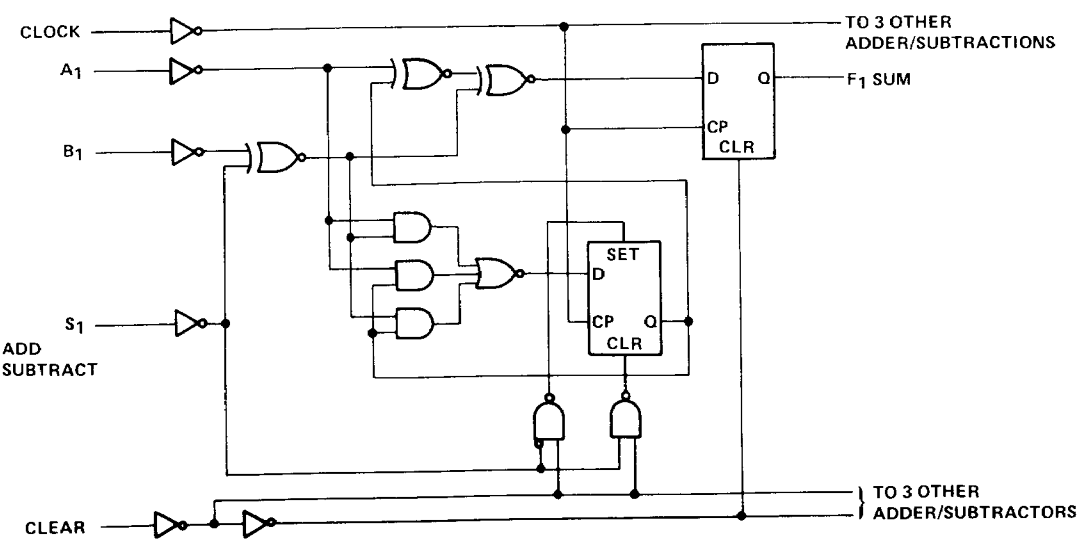
DESCRIPTION

The 25LS15 is a serial/parallel two's complement adder/subtractor designed for use in association with the 25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic one in subtract mode. This least significant plus one is self propagating in the subtract mode as long as zeroes are applied at the LSB's.

The 25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in fast fourier transforms.

LOGIC DIAGRAM
(One of Four Similar Functions)



Recommended Operating Conditions

	Military Min.	Military Typ.	Military Max.	Commercial Min.	Commercial Typ.	Commercial Max.	Units
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5.0	5.25	V
High-Level Output Current I_{OH}			−440			−440	µA
Low Level Output Current I_{OL}			8			8	mA
Operating Free Air Temperature	−55		+125	0		+70	°C

Electrical characteristics Over Operating Temperature Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)		Military Min.	Military Typ. (Note 2)	Military Max.	Commercial Min.	Commercial Typ.	Commercial Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440µA, V_{IN} = V_{IH} or V_{IL}		2.5			2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	Volts
			I_{OL} = 8.0mA			0.45			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				1.5			1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36			−0.36	Volts
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20			20	Volts
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1			0.1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−30		−85	−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.			48	75		48	75	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Input Load Current x Input Load Factor (See Loading Rultes).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All inputs HIGH, measured after a LOW-to-HIGH clock transition.

Switch Characteristics V_{CC} = 5.0V, T_A = +25°C

Parameters	From (Input)	To (Output)	+25°C Min.	+25°C Typ.	+25°C Max.	Units
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	Clock	F		14	22	ns
t_{PHL}	Clock	F		14	22	ns
t_{PHL}	Clear	F		20	30	ns
t_s	Set up time	A, B, S	10			ns
t_h	Hold time	A, B, S	0			ns
t_s	Clear Recovery time		25			ns
t_h	Clear Hold time		0			ns
t_{pw}	Clock Pulse Width	Clock HIGH	17			ns
		Clock LOW	17			ns
t_{pw}	Clear Pulse Width		20			ns
f_{MAX}	Max. Clock Frequency		30	40		MHz

FUNCTION TABLE

External Inputs CP	CLR	S	A	B	Internal Point C	C_1	Output F	Function
X	L	L	X	X	L	L	L	Clear
X	L	H	X	X	H	H	L	Clear
L	H	X	X	X	NC	NC	NC	
H	H	X	X	X	NC	NC	NC	
↑	H	L	L	L	L	L	L	Add
↑	H	L	L	L	H	L	H	Add
↑	H	L	L	H	L	L	H	Add
↑	H	L	L	H	H	H	L	Add
↑	H	L	H	L	L	L	H	Add
↑	H	L	H	L	H	H	L	Add
↑	H	L	H	H	L	H	L	Add
↑	H	L	H	H	H	H	H	Add
↑	H	H	L	L	L	L	H	Subtract
↑	H	H	L	L	H	H	L	Subtract
↑	H	H	L	H	L	L	L	Subtract
↑	H	H	L	H	H	L	H	Subtract
↑	H	H	H	L	L	H	L	Subtract
↑	H	H	H	L	H	H	H	Subtract
↑	H	H	H	H	L	L	H	Subtract
↑	H	H	H	H	H	H	L	Subtract

C = Data In the Carry Flip-Flop Before the Clock Transition
C_1 = Data In the Carry Flip-Flop After the Clock
X = Don't Care
NC = No Change
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition

DEFINITION OF FUNCTIONAL TERMS

A_1,A_2,A_3,A_4 The "A" input into each adder/subtractor

B_1,B_2,B_3,B_4 The "B" input into each adder/subtractor

S_1,S_2,S_3,S_4 The add subtract control for each adder/subtractor. When S is LOW, the F function is A+B. When S is HIGH, the F function is A–B.

F_1,F_2,F_3,F_4 The four independent serial outputs of the adder/subtractor.

CP Clock The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.

CLR Clear When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

APPLICATIONS

The normal butterfly network associated with the Cooley-Tukey Fast Fourier Transform (FFT) algorithm is shown below. Here we assume A, B, C, D and W are all complex numbers such that:

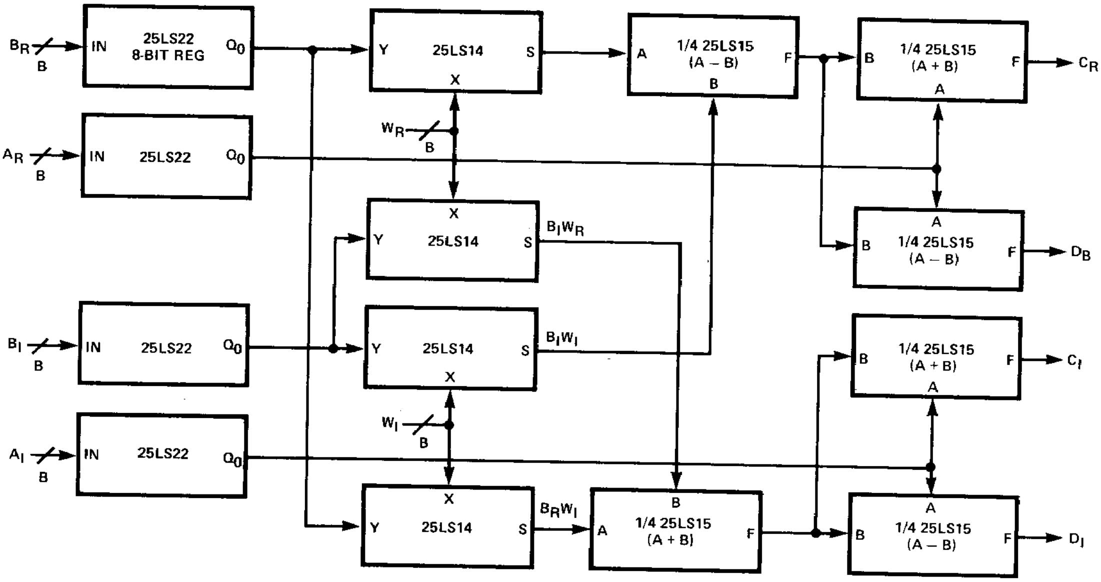
$A = A_R + jA_I$
$B = B_R + jB_I$
$W = W_R + jW_I$

The outputs C and D are also complex numbers and are evaluated as:

$C = C_R + jC_I = (A_R + B_R W_R - B_I W_I) + j(A_I + B_R W_I + B_I W_R)$
$D = C_R + jD_I = (A_R - B_R W_R + B_I W_I) + J(A_I - B_R W_I - B_I W_R)$

The four multiplications can be implemented using four 25LS14 serial-parallel multipliers (the appropriate number of bits must, of course, be used). The additions and the subtractions are implemented using the 25LS15 quad serial adder/subtractors. This diagram depicts only the basic data flow; binary weighting of the numbers, rounding, truncation, etc. must be handled as required by the individual design parameters.

FAST FOURIER TRANSFORM (FFT) BUTTERFLY



An FFT butterfly connection for complex arithmetic inputs and outputs.