

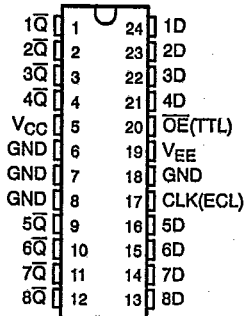
T-52-11

SN10KHT5576, SN100KT5576
OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE
EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D3603, JULY 1990

- ECL and TTL Control Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} , V_{EE} , and GND Configuration Minimizes High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

The SN10KHT5576 and SN100KT5576 are octal ECL-to-TTL inverting translators designed to provide efficient translation between an ECL signal environment and a TTL signal environment.

These devices are designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, receivers, and transmitters.

The eight flip-flops of the '5576 are edge-triggered D-type flip-flops. On the positive transition of the clock, the \bar{Q} outputs take on the complement of the logic levels that were set up at the D inputs. A buffered output-enable input (\bar{OE}) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive give the device the capability to drive bus lines without need for interface or pullup components. The \bar{OE} input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN10KHT5576 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C. The SN100KT5576 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT (TTL)
\bar{OE}	CLK	D	\bar{Q}
L	↑	L	H
L	↑	H	L
L	L	X	\bar{Q}_0
H	X	X	Z

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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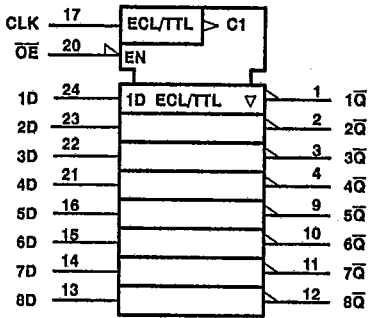
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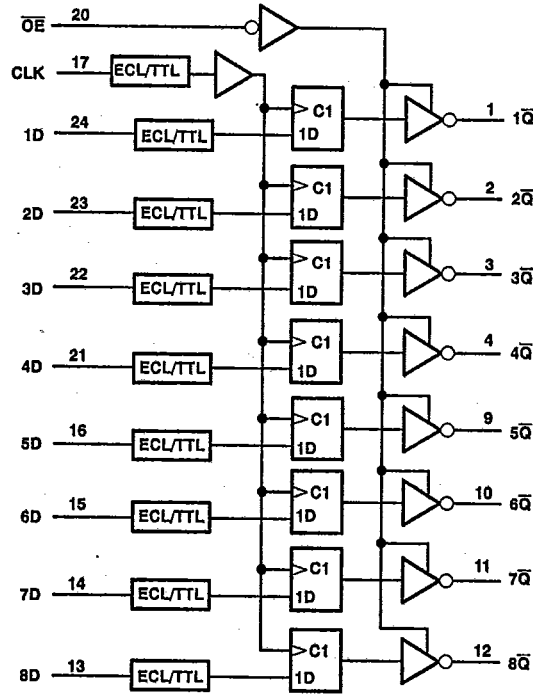
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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