HD151TS303RP

Spread Spectrum Clock for EMI Solution

HITACHI

ADE-205-656C (Z)

Preliminary
Rev. 3
Mar. 2002

Description

The HD151TS303 is a high-performance Spread Spectrum Clock modulator. It is suitable for low EMI solution.

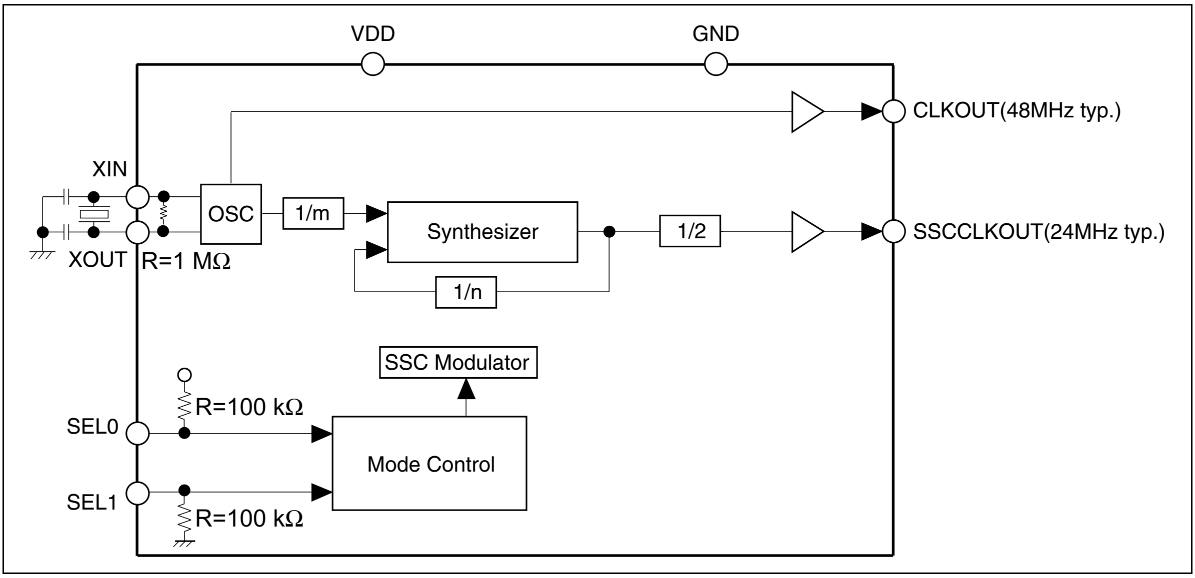
Features

- Supports 10 MHz to 60 MHz operation. (Designed for XIN = 24 MHz and 48 MHz)
- XIN x 1/2 clock frequency with spread spectrum modulation @3.3 V
- 1 copy of reference clock out @3.3 V
- Programmable spread spectrum modulation (±0.25%, ±0.5%, ±1.5% central spread modulation and spread spectrum disable mode.)
- SOP–8pin

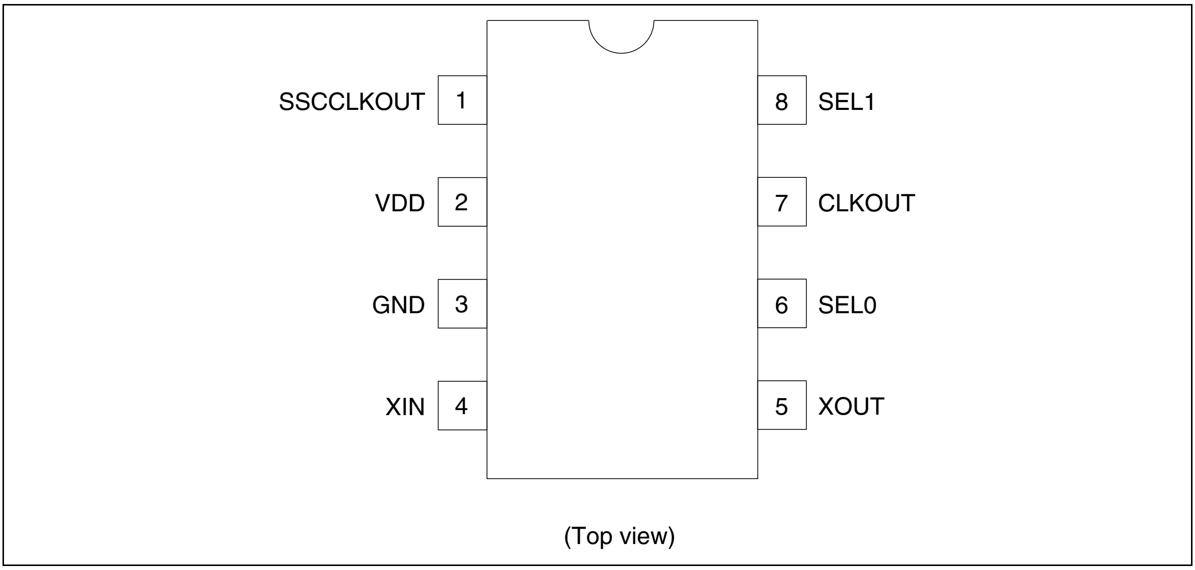
Key Specifications

- Supply voltages : VDD = 3.3 V±0.165 V
- Ta = 0 to 70°C operating range
- Clock output duty cycle = 50±5%
- Cycle to cycle jitter = ±250 ps typ.

Block Diagram



Pin Arrangement



SSC Function Table

SEL1 :0	Spread Percentage
0 0	+0.5%
0 1	±1.5%
1 0	SSC OFF
1 1	±0.25%

Note: ±1.5% SSC is selected for default by internal pull-up & down resistors.

Clock Frequency Table

XIN (MHz)	SSCCLKOUT (MHz)	CLKOUT (MHz)
48	24*1	48*2
24	12*1	24*2

Notes: 1. With spread spectrum modulation.
2. Without spread spectrum modulation.

Pin Descriptions

Pin name	No.	Type	Description
GND	3	Ground	GND pin
VDD	2	Power	Power supplies pin. Normally 3.3 V.
CLKOUT	7	Output	Normally 3.3 V reference clock output.
SSCCLKOUT	1	Output	Spread spectrum modulated clock output. This pin outputs 1/2 frequency of input frequency.
XIN	4	Input	Oscillator input.
XOUT	5	Output	Oscillator output.
SEL0	6	Input	SSC mode select pin. LVCMOS level input. Pull-up by internal resistor. (100 kΩ).
SEL1	8	Input	SSC mode select pin. LVCMOS level input. Pull-down by internal resistor (100 kΩ).

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	–0.5 to 4.6	V	
Input voltage	V_I	–0.5 to 4.6	V	
Output voltage [*1]	V_O	–0.5 to VDD+0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to VDD
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	VDD	3.135	3.3	3.465	V	
DC input signal voltage		–0.3	—	VDD+0.3	V	
High level input voltage	V_{IH}	2.0	—	VDD+0.3	V	
Low level input voltage	V_{IL}	–0.3	—	0.8	V	
Operating temperature	T_a	0	—	70	°C	
Input clock duty cycle		45	50	55	%	

DC Electrical Characteristics

Ta = 0 to 70°C, VDD = 3.3 V±5%

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	—	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	—	V	
Input current	I_I	—	—	±10	μA	V_I = 0 V or 3.465 V, VDD = 3.465 V, XIN pin
		—	—	±100		V_I = 0 V or 3.465 V, VDD = 3.465 V, SEL0, SEL1 pins
Input slew rate		1	—	4	V / ns	20% – 80%
Input capacitance	C_I	—	—	4	pF	SEL0, SEL1
Operating current		—	7	—	mA	XIN = 24 MHz, C_L = 0 pF, VDD = 3.3 V

DC Electrical Characteristics / Clock Output & SSC Clock Output

Ta = 0 to 70°C, VDD = 3.3 V±5%

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V

AC Electrical Characteristics / Clock Output & SSC Clock Output

Ta = 25°C, VDD = 3.3 V, C_L = 30 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter [*1, 2]	t_{CCS}	—	| 250 |	| 300 |	ps	SSCCLKOUT, Fig1, 24 MHz	SSCOFF SEL1:0 = 10
		—	| 250 |	| 300 |		SSCCLKOUT, Fig1, 24 MHz	SSC= ±0.25% SEL1:0 = 11
		—	| 250 |	| 300 |		SSCCLKOUT, Fig1, 24 MHz	SSC= ±1.5% SEL1:0 = 01
		—	| 250 |	| 300 |		CLKOUT, Fig1, 24 MHz & 48 MHz	
Output frequency [*1, 2]		23.8	—	24.2	MHz	SSCCLKOUT, XIN = 48 MHz	SSCOFF SEL1:0 = 10
		23.7	—	24.3		SSCCLKOUT, XIN = 48 MHz	SSC= ±0.25% SEL1:0 = 11
		23.4	—	24.6		SSCCLKOUT, XIN = 48 MHz	SSC= ±1.5% SEL1:0 = 01
		23.8	—	24.2		CLKOUT, 24 MHz	
		47.3	—	48.7		CLKOUT, 48 MHz	
Slew rate [*1]	t_{SL}	1.0	—	—	V/ns	@48 MHz CLKOUT	0.4 V to 2.4 V
Clock duty cycle [*1]		45	50	55	%		
Output impedance [*1]		—	30	—	Ω		
Spread spectrum modulation frequency [*1]		—	33	—	KHz	SSCCLKOUT = 24MHz XIN = 48 MHz	
Input clock frequency		10	—	60	MHz		
Stabilization time [*1,3]		—	—	2	ms		

Notes:
1. Parameters are target of design. Not 100% tested in production.
2. Cycle to cycle jitter and output frequency are included spread spectrum modulation.
3. Stabilization time is the time required for the integrated circuit to obtain phase lock of its input signal after power up.

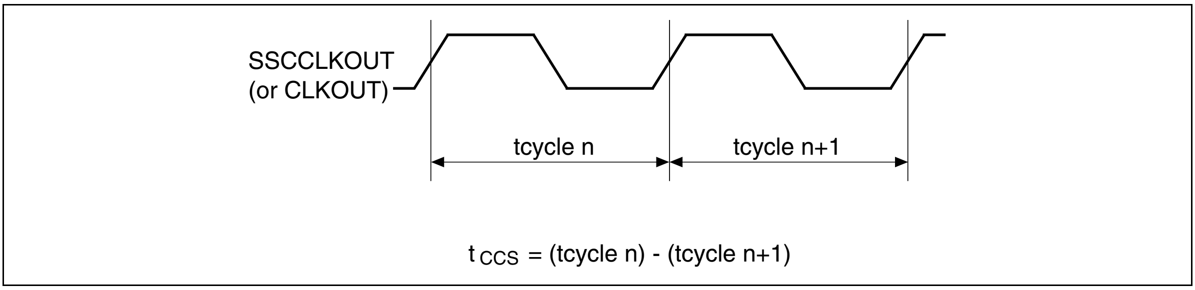


Figure 1 Cycle to cycle jitter

Application Information

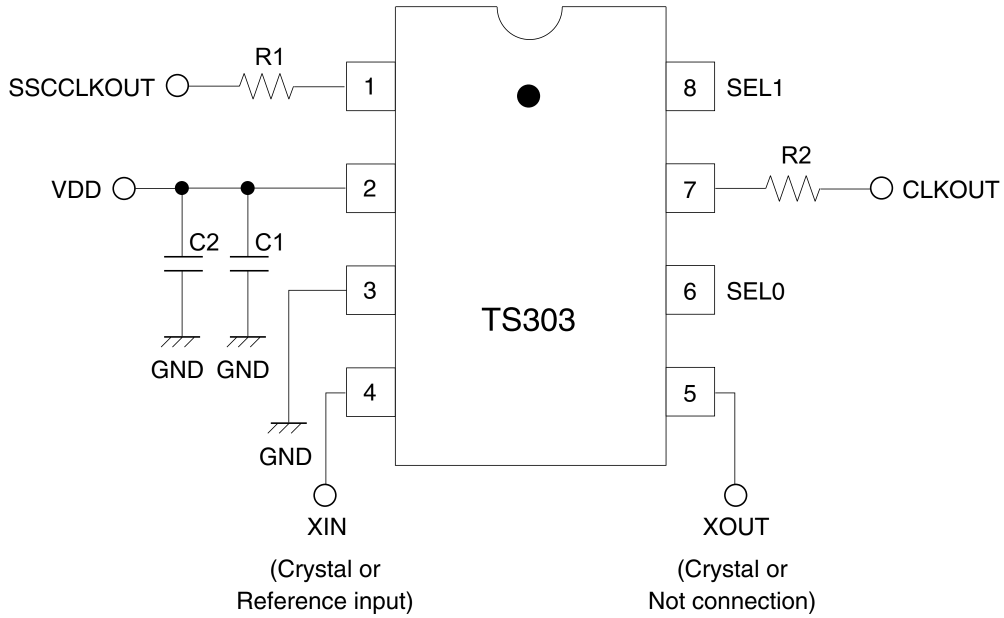
Recommended Circuit Configuration

The power supply circuit of the optimal performance on the application of a system should refer to Fig. 2.

VDD decoupling is important to both reduce Jitter and EMI radiation.

The C1 decoupling capacitor should be placed as close to the VDD pin as possible, otherwise the increased trace inductance will negate its decoupling capability.

The C2 decoupling capacitor shown should be a tantalum type.

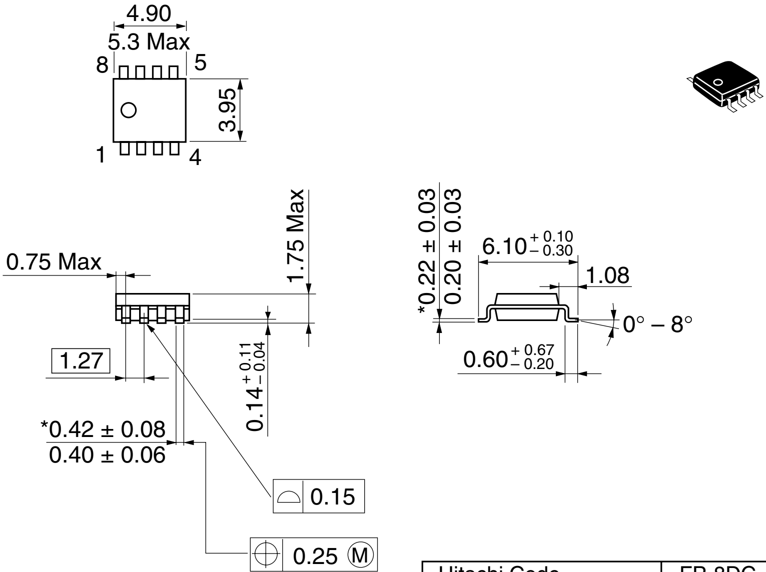


Notes: C1 = High frequency supply decoupling capacitor.
(0.1 µF recommended)
C2 = Low frequency supply decoupling capacitor.
(22 µF tantalum type recommended)
R1, R2 = Match value to line impedance.

Figure 2 Recommended circuit configuration

Package Dimensions

As of July, 2001
Unit: mm



Hitachi Code	FP-8DC
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

*Dimension including the plating thickness
Base material dimension

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL http://www.hitachisemiconductor.com/

For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://semiconductor.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
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