mosaic

Mosaic Semiconductor Inc.

256K x 4 VideoRAM

MVM4259-10/12

Issue 2.0 : February 1992

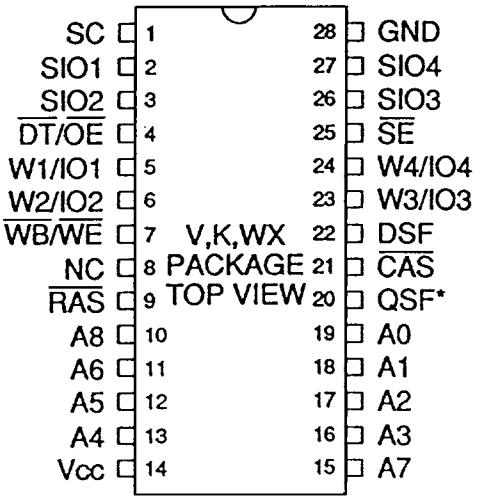
PRELIMINARY

262,144 x 4 CMOS Fully Featured Video RAM

Features

- DRAM organized as 262,144 words x 4 bits.
  SAM organized as 512 words x 4 bits.
- RAM Access Times of 100,120 ns.
  SAM Access Time of 25,30 ns.
- Available in Pinned and Surface Mount Packages.
- Operating Power 715 mW (maximum)
  Low Power Standby 55 mW (maximum)
- Dual Port Accessibility - Simultaneous and Asynchronous Access from the DRAM and SAM Ports
- Bi-directional Data Transfer Function between the DRAM and the Serial Data Register.
- 4 x 4 Block Write feature for Fast Area Fill Operations. As Many as Four Locations Written Per Cycle from an On-chip Colour Register.
- Mask Write function for Selective Write to each RAM I/O, with two Write-per-bit Modes to Simplify System Design.
- Split Serial Data Register for Simplified Real-time Register Reload.
- RAM Output Enable Allows Direct Connection of W/IO and Address Lines to Simplify System Design.
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh, with 512 Refresh Cycles every 8 ms.
- Up to 33 MHz Uninterrupted Serial Data Streams.
- Fast Page-mode Operation for faster access.
- All Inputs and Outputs Directly TTL Compatible (except QSF pin which is open drain type).
- May be Processed to MIL-STD-883D Method 5004.

Pin Definition



Pin Functions

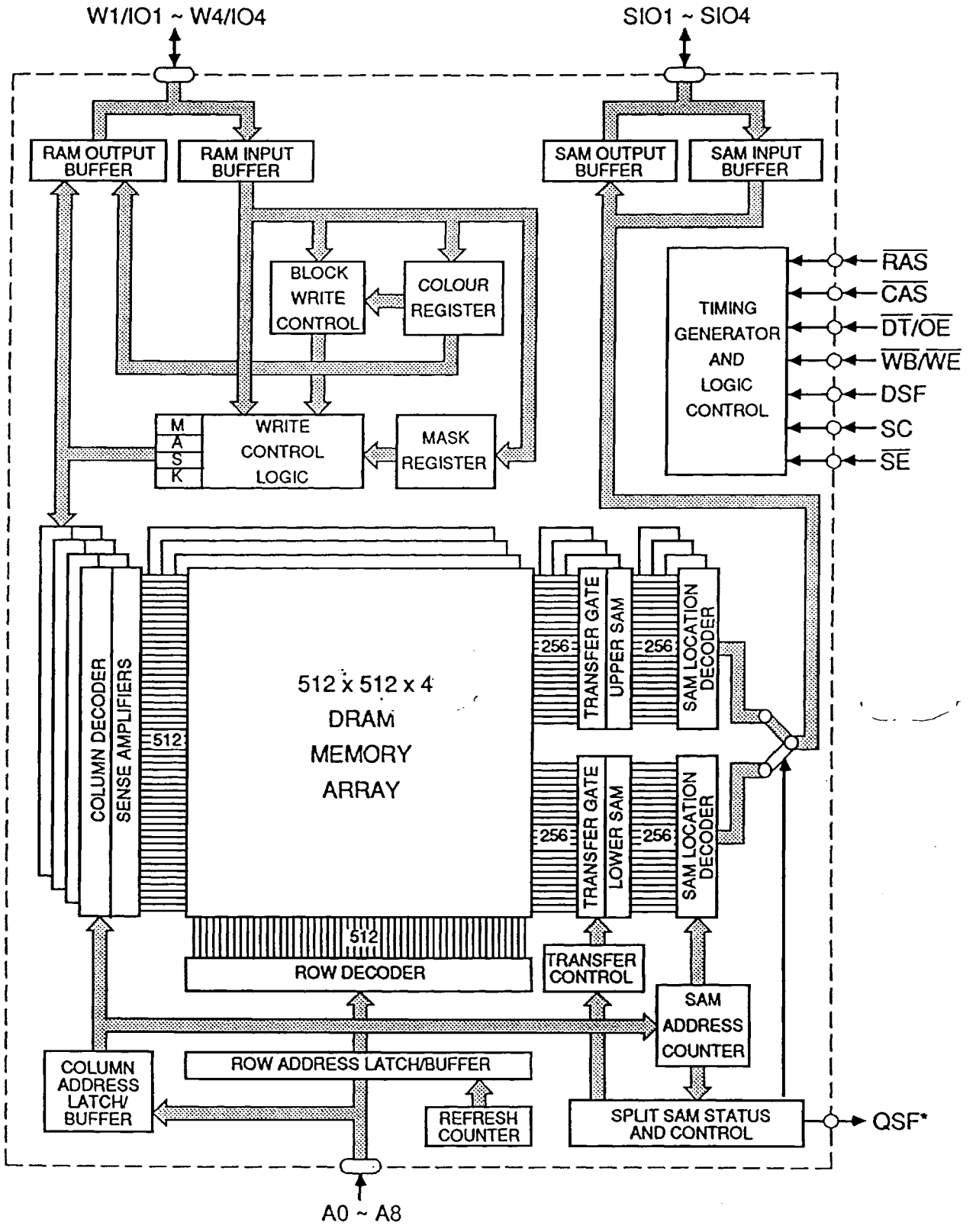
A0~A8	Address Inputs
W/IO1~4	RAM Data Input/Output
SIO1~4	SAM Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WB/WE}$	Write per bit/Write Enable
SC	Serial Clock
$\overline{SE}$	Serial Enable
DSF	Special Function Select
QSF*	Split-Register Activity Status
V_{cc}	Power (+5V)
GND	Ground
NC	No Connect

* THIS PIN IS OPEN DRAIN

Package Details Package Dimensions and details on page 39.

Pin Count	Description	Package Type	Material	Pinout
28	0.1" Vertical-in-Line(VIL™)	V	Ceramic	JEDEC
28	0.4" Leadless Chip carrier (LCC)	WX	Ceramic	JEDEC
28	0.4" Dual-in-Line (DIL)	K	Ceramic	JEDEC

Block Diagram



* Note that the QSF pin is an Open Drain output (see page 8 for details).

MVM4259 Operation Modes

MVM4259 Operation Truth Table

	DSF at $\overline{CAS}$ ↓			L	L	H	H
	DSF at $\overline{RAS}$ ↓			L	H	L	H
L	X	X	X	$\overline{CAS}$ Before $\overline{RAS}$ Refresh			
H	L	L	L	Write Transfer	Write Transfer	Write Transfer	Write Transfer
H	L	L	H	Pseudo Write Transfer		Pseudo Write Transfer	
H	L	H	X	Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
H	H	L	X	Mask Read / Write	Persistent Mask Write	Mask Block Write	Persistent Mask Block Write
H	H	H	X	Normal Read / Write	Load Mask	Block Write	Load Colour
$\overline{CAS}$	$\overline{DT}$/$\overline{OE}$	$\overline{WB}$/$\overline{WE}$	$\overline{SE}$				

MVM4259 Functional Truth Table

TYPE (1)	$\overline{RAS}$↓					$\overline{CAS}$↓	ADDRESS		W/IO		FUNCTION
	$\overline{CAS}$	$\overline{DT}$/$\overline{OE}$	$\overline{WB}$/$\overline{WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$↓	$\overline{CAS}$↓	$\overline{RAS}$↓	$\overline{CAS}$↓ $\overline{WE}$↓	
R	L	X	X	X	X	X	X	X	X	X	$\overline{CAS}$ Before $\overline{RAS}$ Refresh
T	H	L	L	L	L	X	Row Address	Tap Point	X	X	Register to Memory Transfer (Write Transfer)
T	H	L	L	H	X	X	Row Address	Tap Point	X	X	Alternate Transfer Write (Independent of $\overline{SE}$)
T	H	L	L	L	H	X	Refresh Address	Tap Point	X	X	Serial Write Mode Enable (Pseudo Transfer Write)
T	H	L	H	L	X	X	Row Address	Tap Point	X	X	Memory to Register Transfer (Read Transfer)
T	H	L	H	H	X	X	Row Address	Tap Point	X	X	Split Register Transfer Read (Must Reload Tap)
R	H	H	L	L	X	L	Row Address	Column Address	Write Mask	Valid Data	Load and use Write Mask, Write Data to DRAM
R	H	H	L	L	X	H	Row Address	Column A2 - A8	Write Mask	Address Mask	Load and use Write Mask, Block Write to DRAM
R	H	H	L	H	X	L	Row Address	Column Address	X	Valid Data	Persistent Mask Write, Write Data to DRAM
R	H	H	L	H	X	H	Row Address	Column A2 - A8	X	Address Mask	Persistent Mask Write Block Write to DRAM
R	H	H	H	L	X	L	Row Address	Column Address	X	Valid Data	Normal DRAM Read/Write (Non Masked)
R	H	H	H	L	X	H	Row Address	Column A2 - A8	X	Address Mask	Block Write to DRAM (Non Masked)
R	H	H	H	H	X	L	Refresh Address	X	X	Write Mask	Load Write Mask
R	H	H	H	H	X	H	Refresh Address	X	X	Colour Data	Load Colour Register

Note R = Random access operation T = Transfer operation.

GENERAL DESCRIPTION

The MVM4259 multiport video RAM is a fully featured dual ported memory device consisting of a 262,144 word by 4 bit dynamic Random Access Memory (RAM), and a 512 word by 4 bit Serial Access Memory (SAM). Three basic types of operation are supported: random access to and from the RAM, serial access to and from the SAM and bidirectional transfer between any row in the RAM and the SAM. Except during transfer operations, the MVM4259 can be accessed simultaneously and asynchronously from the RAM and SAM ports.

The MVM4259 is provided with several advanced features which allow higher system level bandwidth and simplify design on both the RAM and SAM ports. On the RAM port greater pixel draw rates can be achieved by using the Block Write mode, allowing as many as 16 bits of data to be written to the RAM in each CAS cycle. Also on the RAM port, a Write Mask Register provides a persistent write per bit mode without repeated mask loading.

The SAM is divided into two halves, so while one half is being read from the SAM port the other half can be loaded from the RAM. The QSF output pin indicates which half of the SAM is currently being accessed. The SAM can also be configured in input mode to accept serial data from an external device and can operate at clock rates of upto 33MHz.

PIN FUNCTIONS

Data Transfer/Output Enable (DT/OE)

This pin is a multifunction pin, selecting either register or random access operation as RAS falls. In random access DRAM mode, DT/OE must be high as RAS falls, and DT/OE is used as an Output Enable pin. When DT/OE is held high, the W/IO outputs are in the high impedance state to prevent overlap between the address and the DRAM data. This allows multiplexed address/data, but does not allow the use of the early Write Cycle.

If DT/OE is low as RAS falls, a data transfer operation is initiated between the RAM and SAM ports, in which the 512 bit positions in the serial register are connected to the bit lines.

Address Inputs (A0~A8)

The 18 bits required to decode one of 262,144 cell locations within the DRAM array of the MVM4259 are multiplexed onto nine address input pins. Nine row address bits are latched on the falling edge of RAS, and the nine column address bits are latched on the falling edge of CAS. All addresses must be stable on or before these falling edges.

Row Address Strobe (RAS)

The RAS control input latches the states of the row address, WB/WE, DT/OE, SE and CAS onto the chip to begin the various DRAM and transfer functions of the MVM4259 as shown in the Function Table. RAS has minimum and maximum pulse widths and a minimum precharge requirements which must be met for correct device operation. The RAM port is placed in standby mode when RAS is held high.

Column Address Strobe (CAS)

The CAS input latches the column address and DSF states to control either Read/Write operations or special Block Write features. CAS has minimum and maximum pulse widths and a minimum precharge requirements which must be met for correct device operation. CAS also acts as an output enable for the output buffers on the RAM port.

Mask Write/Write Enable (WB/WE)

This pin is also multifunction. When it is high at the falling edge of RAS during RAM port operations, the data in the memory array can be written in the same way as a standard DRAM. If it is low at RAS fall during RAM port operations, the Mask Write function is enabled. This pin also determines the direction of data transfer between the RAM and the SAM.

When WB/WE is high at RAS fall the data is transferred from RAM to SAM (Read Transfer); when it is low, the transfer is from the SAM to the RAM (Write Transfer).

Mask Data/Data Input and Output (W/IO1 ~ W/IO4)

When the Mask Write mode is enabled, the data on the W/IO pins is latched into the Mask Register at the falling edge of RAS. Data is only written into the DRAM on data lines where the mask data is a "1" and writes are inhibited on lines where the mask data is "0". The mask data is valid for only one cycle.

DRAM data is written during Write or Read-Modify-Write Cycles, with the falling edge of WB/WE latching the data. In an early Write Cycle, WB/WE is brought low before CAS and the data is latched by CAS. In a delayed Write or Read-Modify-Write Cycle, CAS is already low, so the data is strobed in by WB/WE.

The three state output buffers are controlled by CAS and DT/OE. If CAS or DT/OE is held high the outputs remain in the high impedance (floating) state. Data will not appear on the outputs until both CAS and DT/OE are low, and the outputs will remain valid while they are low. In an early Write Cycle or a register transfer operation the outputs remain in the high impedance state for the entire cycle.

Serial Clock (SC)

All operations of the SAM port are synchronised with the SC pin, with data being shifted in or out of the SAM registers at the rising edge of SC. In a Serial Read, the output data becomes valid on the SIO pins after t_{SCA} from the rising edge of SC. The serial clock also increments the 9 bit (8 bit in Split Register mode) serial pointer which is used to select the SAM address. The pointer operates in wrap-around mode (when it reaches location 511 the next SC clock places it at location 0) through the SAM to select sequential locations after the starting location (or Tap Point), which is determined by the column address in the Read Transfer Cycle.

***IMPORTANT NOTE** : While SE is held high the serial clock is NOT DISABLED. Thus, any SC pulses will increment the internal serial address counter regardless of the state of SE. This ungated clock design minimizes the access time for serial output from SE low since the SC input buffer and serial address counter are not disabled by SE.*

Serial Enable (SE)

This pin allows serial access operation. In a Read Cycle, SE is used as an output control, while in a Write Cycle it is used as a write enable control. Note that if SE is high serial access is disabled, but the SAM pointer is still incremented when SC is clocked.

Special Function Control Input (DSF)

DSF is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and enables the selection of various RAM and data transfer operating modes. As well as normal DRAM modes, the MVM4259 special features of Persistent Mask Write, Block Write, Mask Block Write, Persistent Mask Block Write, Load Mask/Colour Register and Split Read Transfer can be invoked.

Special Function Output (QSF)

This pin is an OPEN DRAIN output pin. During the split-register mode, QSF indicates which half of the SAM is being accessed. If QSF is on (low state), then the serial address pointer is accessing the lower 256 bits (0 to 255) of the SAM, while QSF off indicates that the pointer is accessing the upper 256 bits (256 to 511). After QSF has toggled a delay of t_{STS} must be met before a Split Read Transfer operation can be performed on the inactive half of the split SAM.

If the detection of the zero to one transition of QSF is required an external pull-up resistor is needed, and the output rise time is determined by the load capacitance and the value of the resistor. The specification of the QSF switching time assumes a resistor value of 820Ω and a load capacitance of 50pF.

Serial Data Input/Output (SIO1 ~ SIO4)

Serial input and output share common pins. The mode of these pins is determined by the most recent Read, Write or Pseudo Write Transfer Cycle. When a Read Transfer is inititaed, the SAM is in the output mode; when a Write or Pseudo Write cycle is now invoked, the SAM port switches from output to input, and during subsequent writes the SAM remains in the input mode.

Detailed Pin Description vs Operational Mode

PIN	*DRAM*	*TRANSFER*	*SAM*
A0~A8	Row and Column Address	Row and Tap Address	
W/IO1~4	Write Mask / Data IN, OUT		
SIO1~4			Serial Data I/O
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{WB}/\overline{WE}$	Write per bit/Write Enable	Transfer Write Enable	
DSF	Block Write Enable Persistent Write-per-Bit Enable Colour Register Load Enable Write per Bit Mask Load Enable	Split-register Enable Alternate Write Transfer Enable	
QSF			Split Register Status
$\overline{SE}$		Serial in Mode Enable	Serial Enable
SC			Serial Clock
$\overline{DT}/\overline{OE}$	Output Enable	Data Transfer	

RAM PORT OPERATION

Fast Page Mode Cycle

Fast Page-mode operation allows faster access by keeping the same row address while selecting random column addresses. The times for row address setup, row address hold and address multiplex are eliminated, and the memory cycle time can be reduced by up to a third. The maximum number of columns which can be accessed is limited by the maximum RAS low time of 100µs.

For the initial page mode access, the output data is valid after the specified access times from RAS, CAS, column address and DT/OE. For all subsequent page read operations, the output data is valid after the specified access times from CAS, column address and DT/OE.

During Mask Write operations, the mask data is loaded at the falling edge of RAS and is maintained throughout the Page mode or Read-Modify-Write cycles.

RAS-only Refresh

A refresh operation must be performed to each of the 512 rows at least once every 8 ms to retain data. Although any normal memory cycle will perform this operation, refresh is most easily performed with a RAS Only cycle.

CAS-before-RAS Refresh

If CAS is brought low for a specified period (t_{CSR}) before RAS goes low, an internal counter and clock generators are enabled and an internal refresh operation takes place. When this refresh is complete, the address counter automatically increments in preparation for the next CAS-before-RAS cycle. For successive cycles, CAS may be held low while RAS cycles.

Hidden Refresh

This mode is a CAS-before-RAS refresh performed by holding CAS low from a previous Read Cycle. The output data from the previous memory cycle remains valid while performing the refresh. The internal refresh counter provides the address and the refresh is accomplished by cycling RAS.

Mask Write Function

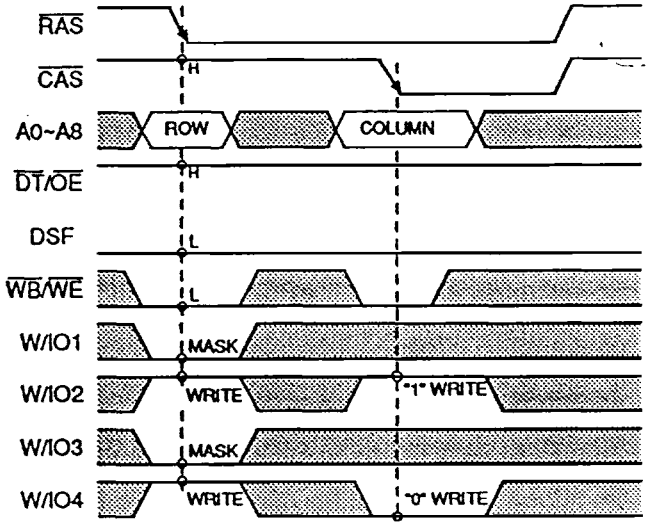
The WB/WE pin is used to select the DRAM Mask Write mode of operation. A high on WB/WE selects the Read mode and a low selects the write mode. In an early Write Cycle, WB/WE is brought low before CAS and the W/IO pins remain in the high impedance state throughout the entire cycle. During DRAM Write Cycles, holding WB/WE low on the falling edge of RAS will begin the Mask Write operation, as shown in the following table:

RAS↓					CAS↓	
CAS	DT/OE	WB/WE	DSF	W/IO	DSF	Function
H	H	H	L	X	L	NORMAL WRITE
H	H	L	L	MASK DATA	L	MASK WRITE
H	H	L	H	X	L	PERSISTENT MASK WRITE

(1) If DSF is low at the falling edge of RAS the write mask is reloaded. This means that mask data is required on the W/IO pins, latched on the falling edge of RAS, and new mask data is required at every RAS fall. This mask selects which of the four W/IO inputs are written and which are not, with a mask bit high indicating data will be written to that particular bit, and a mask bit low indicating that it will not. After RAS has latched the mask data on chip, the input data is latched on the falling edge of CAS.

(2) If DSF is high at the falling edge of RAS, the mask is not reloaded, but instead retains the value loaded during the last mask Write Mask reload; any data on the W/IO pins is a don't care. This mode is known as Persistent Mask Write because the mask is persistent over any number of Write Cycles. The mask data is loaded into the register using either the Load Write Mask, Mask Write or Persistent Mask Write cycles.

NOTE: The Mask Write operation is initiated only if WB/WE is low at the falling edge of RAS. If it is high, the Write operation is identical to that of standard 256K x 4 DRAMs.



Load Colour Register

The MVM4259 is provided with an on-chip 4 bit colour register which is used in the Block Write operation, with each bit of this register corresponding to one of the RAM I/O blocks. The Load Colour Register cycle is initiated by holding CAS, DT/OE, WB/WE and DSF high at the falling edge of RAS, and by holding DSF low at the falling edge of CAS. The data on the W/IO pins is

latched into the colour register at the falling edge of CAS or WB/WE, whichever occurs later. During this cycle a valid row address (A0~A8) is not required, but the cells of the row address which was latched at RAS fall will be refreshed.

Load Mask Register

The MVM4259 is provided with an on-chip 4 bit mask register which provides the I/O mask data during the Mask Write (normal and Persistent) and Block Write (normal and Persistent) functions. Each bit of the mask register corresponds to one of the RAM I/O blocks, with the mask data being loaded into the register via the Load Write Mask Cycle prior to the execution of a Persistent Mask Cycle.

The Load Write Mask Cycle requires that CAS, DT/OE, WB/WE and DSF are high at the falling edge of RAS and by DSF high at the falling edge of CAS. The data on the W/IO pins is latched into the mask register at the falling edge of CAS or WB/WE, whichever occurs later. The data loaded into this register will also be updated by the Mask Write or Mask Block Write modes. During this cycle a valid row address (A0~A8) is not required, but the cells of the row address which was latched at RAS fall will be refreshed.

Block Write

This is a special RAM port write function which, in a single RAS cycle, allows data in the Colour Register to be written into 4 consecutive column address locations starting from a selected column in a selected row. There are three block write modes, with column mask capability applicable on all three modes. The address lines A2~A8 are latched on the falling edge of CAS giving the starting column address, with A0~A1 being replaced by the four W/IO bits, which are latched on the falling edge of CAS. These four bits are used as an address mask and indicate which of the four column address locations addressed by A2~A8 will be written with the contents of the colour register.

In the following table each W/IO enables the specified column addresses, where a 1 enables a write to that column and a 0 disables the write.

DATA PIN	A1	A0
W1/IO1	0	0
W2/IO2	0	1
W3/IO3	1	0
W4/IO4	1	1

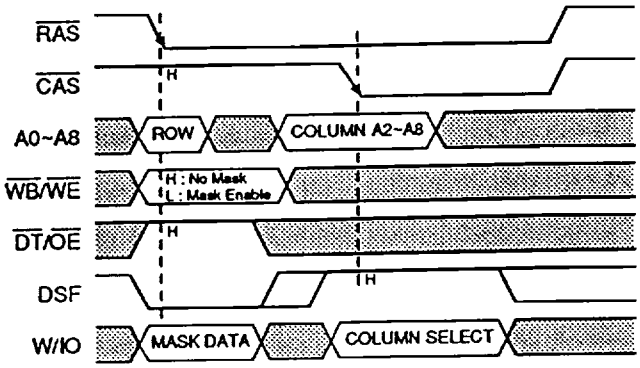
A Block Write Cycle is initiated by holding CAS and DT/OE high at RAS fall and DSF high at CAS fall. The state of the WB/WE and DSF pins at the falling edge of RAS selects one of the three block write modes:

RAS↓					CAS↓		
CAS	DT/OE	WB/WE	DSF	W/IO	DSF	W/IO	Function
H	H	H	L	X	H	COL MASK	BLOCK WRITE
H	H	L	L	MASK DATA	H	COL MASK	MASK BLOCK WRITE
H	H	L	H	X	H	COL MASK	PERSISTENT MASK BLOCK WRITE

(1) When DSF is low and WB/WE is high at RAS fall, the Block Write mode is selected.

(2) If DSF and WB/WE are low at the falling edge of RAS, the Mask Block Write mode is selected, and the mask data on the W/IO pins is latched and used in the same way as the Mask Write mode.

(3) When DSF is high and WB/WE is low at RAS fall, the Persistent Block Write mode is selected, and the data previously loaded into the mask register is used, as in the Persistent Mask Write mode.



The example below shows this mode with a data mask on W/IO1 and W/IO4 and a column mask on column 1.

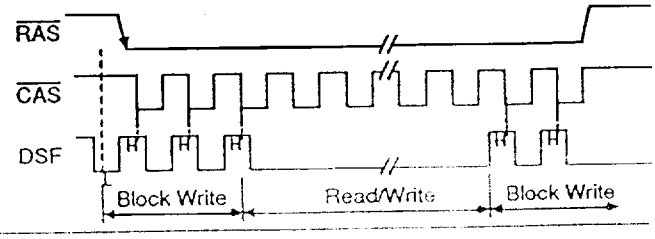
	Mask Data	Column Select	Colour Reg.
W/IO1	0	1	1
W/IO2	1	0	1
W/IO3	1	1	0
W/IO4	0	1	0

	COL. 0	COL. 1	COL. 2	COL. 3	
W/IO1					MASK
W/IO2	1		1	1	
W/IO3	0		0	0	
W/IO4					MASK
		MASK			

Fast Page Mode Block Write Cycle

This mode can be used to perform high speed clear and fill operations, and is initiated by holding DSF low at the falling edge of RAS; with each subsequent CAS cycle with DSF high at CAS fall a Block Write is performed.

If DSF is low at CAS fall, a normal Page Mode Cycle occurs, thus Block Write and Read/Write operations can be mixed during a Page Mode Block Write Cycle:

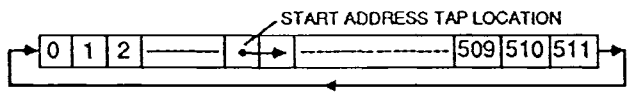


SERIAL PORT OPERATION

Single Register Mode

Operation in this mode allows high speed read or write operations through the SAM port independent of the RAM port operations, except during Read/Write/Pseudo Write Transfer Cycles, with the preceding transfer operation determining the direction of data flow through the SAM port. If the previous transfer was a Read, the SAM is in the output mode, and if it was a Write or Pseudo Write Transfer the SAM port will be in the input mode. Note that the Pseudo Write operation only switches the SAM port from output to input mode; no data is transferred from SAM to RAM.

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of the RAM. Serial data can be read from the SAM after a Read Transfer (RAM to SAM) has been performed, and data is accessed from the SAM starting at any of the 512 data bit locations, with the start location being selected by A0~A8 on the falling edge of CAS. The SAM is then accessed starting from this location and proceeding from the lowest to the highest significant bits, with wrap-around occurring at bits 511 and 0.



Subsequent real time Read Transfers may be performed on-the-fly as many times as necessary within the refresh time constraints of the DRAM memory array. (Simultaneous serial read operations can be performed with some timing restrictions.)

A Pseudo Write Transfer Cycle is used to change the SAM from output to input mode in order to write data into the serial registers, and subsequently a Write Transfer Cycle must be used to load the SAM data into the RAM row selected by the row address on A0~A8 at the falling edge of RAS. The starting location or Tap Point in the SAM for the next serial write is selected by the column address at the falling edge of CAS. The truth table for single register mode operation is shown below:

SAM port Operation	$\overline{RAS}\downarrow$ $\overline{DT}/\overline{OE}$	SC	$\overline{SE}$	Function for Serial Read	Preceded by
Serial Output Mode	H	⎍	L	Enable	Read Transfer
			H	Disable	
Serial Input Mode		⎍	L	Enable	Write Transfer
			H	Disable	
Serial Input Mode		⎍	L	Enable	Pseudo Write Transfer
			H	Disable	

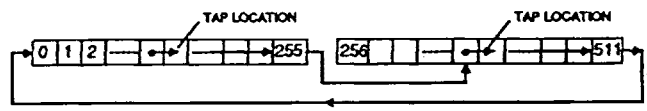
During all transfer cycles CAS must be cycled so that the column addresses are latched on the falling edge of CAS to set the SAM tap location. If CAS remains high during a transfer cycle the SAM pointer would be undefined; ***a transfer with CAS high is not allowed.***

Split-register Mode

In this mode data can be shifted out of one half of the SAM while a Split Read Transfer is being performed on the other half. A normal non split Read Transfer (which places the SAM into output mode) must precede any Split Read Transfer operation. ***Split Read Transfers do not change the SAM port mode previously set by normal transfer operations.*** RAM port operation may be performed independently except during Split Transfers.

The low half of the SAM contains bits 0 to 255 and the upper half bits 256 to 511. When a split-register transfer is being performed, the tap address must be strobed in on the falling edge of CAS. The half of the SAM which is inactive (as indicated by the QSF pin) is loaded during a Split Read Transfer, with data being clocked out of the other half via the serial port pins.

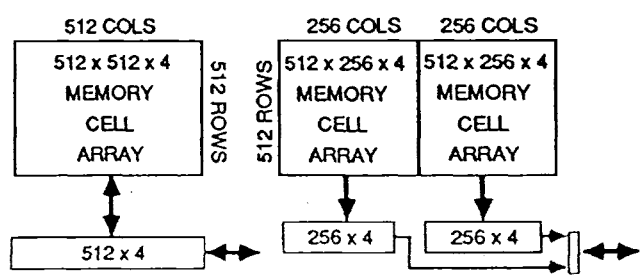
Serial data can be shifted out of one of the split SAM registers starting from any of the 256 tap locations ***excluding the last address of each half.*** Data is shifted out sequentially starting from the selected tap location to the most significant bit (255 or 511) of the first SAM and then the SAM pointer moves to the tap location selected for the second split SAM. Data is then shifted out sequentially starting from this new tap location to the most significant bit (511 or 255) and finally wraps around to the least significant bit. This process is illustrated below.



Note that the serial start address must be supplied for every split-register transfer.

Data Transfer Operations

Two types of internal data transfer are possible with the MVM4259, and are shown graphically below:



(a) Normal Transfer (b) Split Read Transfer

During a normal transfer, 512 words x 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). In a split read transfer, 256 words x 4 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM. These transfer modes are controlled by the DSF pin.

The table below illustrates all of the possible transfer operations, namely Read Transfer, Split Read Transfer, Write Transfer and Pseudo Write Transfer. Data transfer operations are invoked by holding DT/OE low at the falling edge of RAS, and the type of transfer is determined by the states of CAS, WB/WE, SE and DSF, which are latched at the falling edge of RAS.

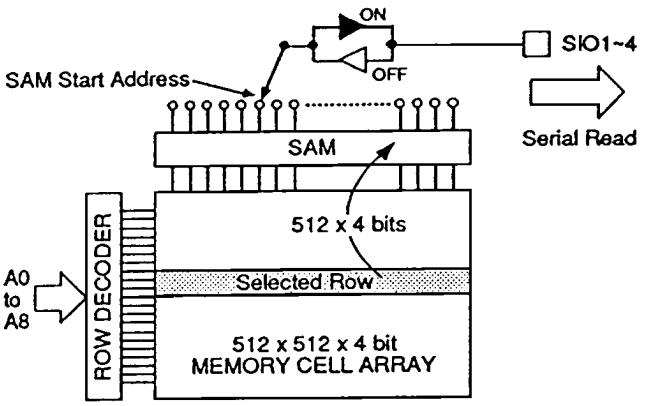
During normal non split transfers, the SAM is switched from input to output mode by a Read Transfer Cycle, and from output to input by a Write Transfer Cycle, but its state remains unchanged during Split Read Transfer operations. During a transfer cycle, the row address A0~A8 select one of the 512 rows in the RAM to or from which data will be transferred, and the column address A0~A8 selects one of the tap locations in the SAM. This location is the start position in the SAM from which the first serial data will be read out from during subsequent Serial Read Cycles, or the start position in the SAM into which the first serial data will be written. During Split Read Transfer Cycles, column address A8 is controlled internally to determine which half of the SAM will be reloaded from the RAM.

Note that all transfer write operations will switch the SIO pins into the input (write) mode, and transfer read operations will switch the SIO pins into the output (read) mode. However, before data can be clocked into the serial port via the SIO pins and SC clock, it is necessary to switch the SIO pins into input mode via a previous transfer write operation. (The Pseudo Transfer mode serves to switch the direction of the SIO pins without actual data transfer taking place.) All transfer read operations and the pseudo transfer write operation will perform a memory refresh on the selected row.

Read Transfer Cycle

A Read Transfer Cycle consists of storing a selected row of data in the RAM into the SAM. This cycle is initiated by holding CAS and WB/WE high, DT/OE and DSF low at the falling edge of RAS. The row address available at RAS fall determines to RAM row to be loaded into the SAM. The transfer cycle is completed at the rising edge of DT/OE, and the SAM is placed in the output mode.

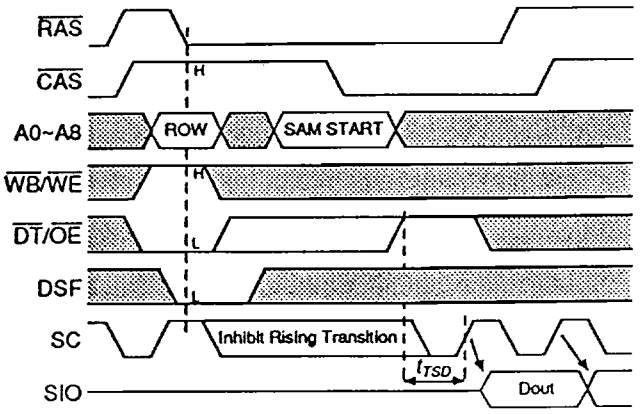
In a Read/Real Time Read Transfer Cycle, the transfer of a new row of data is completed at the rising edge of DT/OE and this data becomes valid on the SIO pins after t_{SCA} from the rising edge of the next SC clock cycle. The tap point for the SAM is set by the column address selected at the falling edge of CAS. The Read Transfer operation is shown diagrammatically below:



In a Read Transfer Cycle (preceded by a Write Transfer Cycle) the SC clock must be held at V_{IH} or V_{IL} after the specified SC high time has been satisfied. An SC rising edge must not occur until after t_{TSD} from the rising edge of DT/OE as shown in the waveform overleaf:

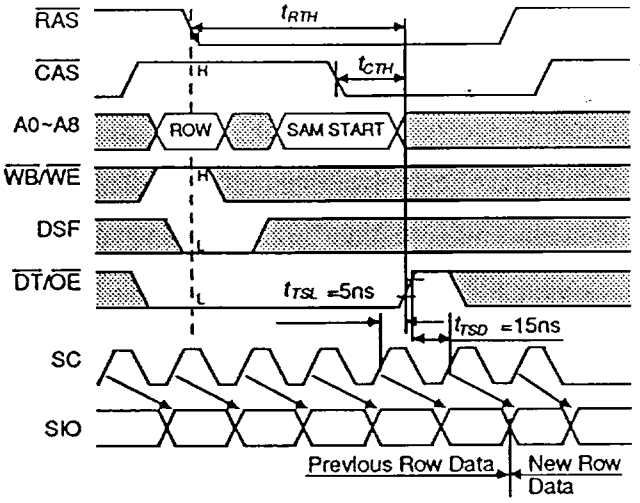
MVM4259 Transfer Modes

$\overline{RAS}$↓					Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	DSF				
H	L	H	X	L	READ TRANSFER	RAM → SAM	512 x 4	INPUT → OUTPUT
H	L	L	L	L	WRITE TRANSFER	SAM → RAM	512 x 4	OUTPUT → INPUT
H	L	L	H	L	PSEUDO WRITE TRANSFER			OUTPUT → INPUT
H	L	L	X	H	WRITE TRANSFER	SAM → RAM	512 x 4	OUTPUT → INPUT
H	L	H	X	H	SPLIT READ TRANSFER	RAM → SAM	256 x 4	NOT CHANGED



Read Transfer Timing

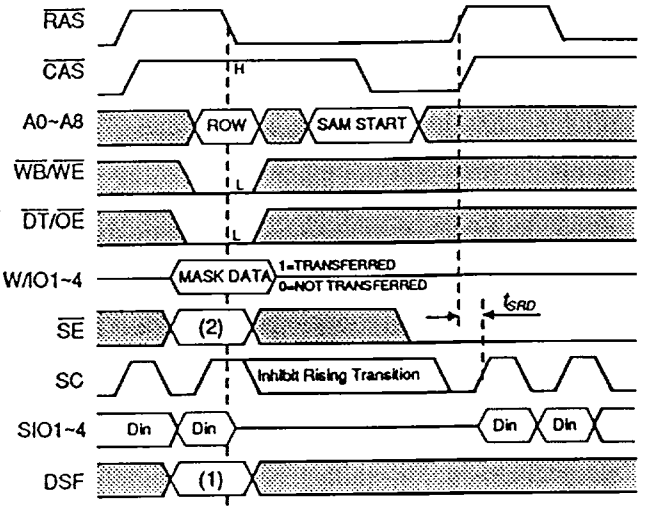
In a Real Time Read Transfer Cycle (which is preceded by another Read Transfer Cycle), the previous row data remains on the SIO pins until DT//OE goes high and serial access time t_{SCA} is satisfied. This feature means that the first bit of the new row of data appears on the SIO pins as soon as the last bit of the previous row has been clocked without any timing loss. To make this continuous data flow possible, the DT/OE rising edge must be synchronised with RAS, CAS and the subsequent rising edge of SC, with t_{RTH}, t_{CTH} and t_{TSL}/t_{TSD} being satisfied as shown below:



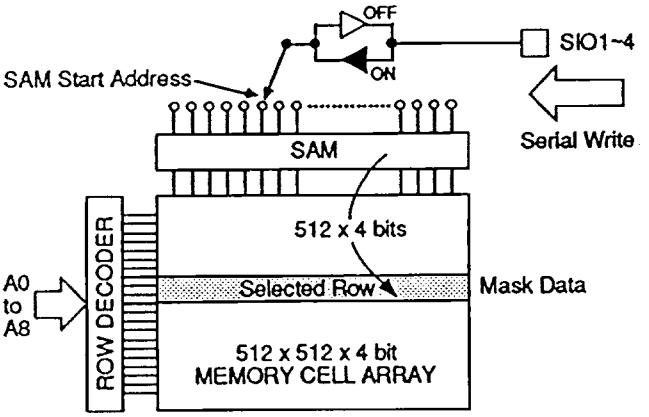
The timing restrictions for t_{TSL}/t_{TSD} are 5/15 ns minimum, but the Split Read Transfer mode eliminates these.

Write Transfer Cycle

This cycle transfers the contents of the SAM into a selected row of the RAM. If the SAM data is to be first loaded through the SAM SIO pins, a Pseudo Write Transfer operation must precede this cycle. However, if the SAM was previously loaded via a Read Transfer, the SAM to RAM transfer can be performed simply by executing a Write Transfer Cycle. The Write Transfer Cycle is initiated by holding CAS high and DT/OE, WB/WE, SE, DSF low at RAS fall. Additionally, a Write Transfer independent of SE is possible if, at the falling edge of RAS, DSF is high and CAS, DT/OE, WB/WE are low.



The row address selected at RAS fall determines the RAM row into which the data from the SAM will be transferred, and the column address selected at CAS fall selects the tap point within the SAM. After the Write Transfer is completed, the SIO pins are placed in the input mode so that data synchronised with the SC clock can be loaded.



Block Diagram for Write Transfer Operation

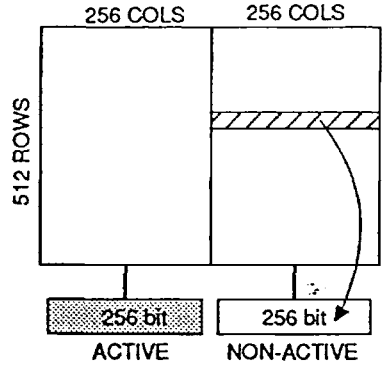
When consecutive Write Transfer operations are performed, no new data can be written into the SAM until the RAS cycle of the preceding Write Transfer is completed; ***the SC clock must be held constant at V_{IL} or V_{IH} during this RAS cycle.*** An SC rising edge is only allowed after t_{SRD} from the rising edge of RAS, at which time a new row of data can be written into the SAM.

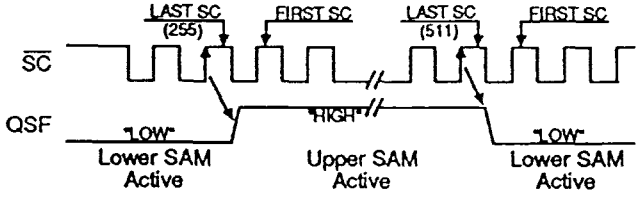
Pseudo Write Transfer Cycle

After a Read Transfer operation has been performed a Pseudo Write Transfer Cycle must be executed before loading data into the SAM; this cycle only switches the SAM from output to input mode - no data transfer takes place. After the SAM is loaded, a Write Transfer Cycle must be invoked to transfer data from the SAM to the RAM. A Pseudo Write Transfer is initiated by holding CAS, SE high and DT/OE, WB/WE, DSF low at the falling edge of RAS. The critical timing conditions are the same as those for the Write Transfer Cycle except for the state of SE at RAS fall.

Split Read Transfer and QSF

During Split Read Transfers, the SAM is split into two halves of 256 x 4 bits which can be controlled independently. Split Read Transfer operations can be performed to the inactive half of the SAM while serial data is being shifted out of the active half as shown below: Note that address A8 is controlled internally to determine which half of the SAM is loaded from the RAM, with the QSF output pin indicating which half of the SAM is currently active. To set up the tap point in the active half of the SAM, only address line A0~A7 are required, which are latched on the falling edge of CAS. QSF changes state when the last SC clock is applied to the active split SAM as shown below:

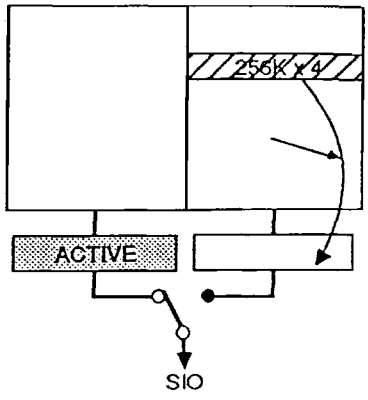




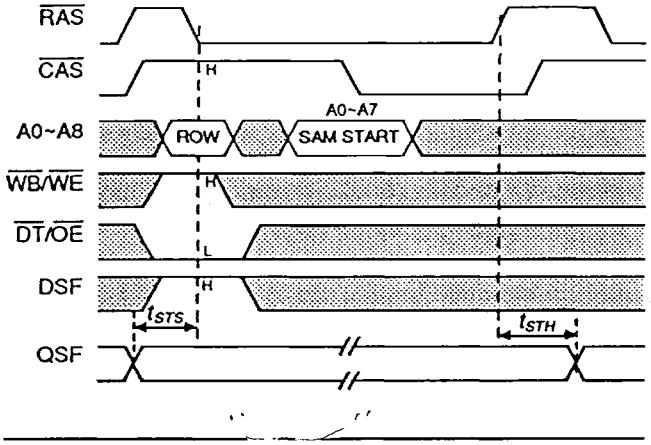
Split Read Transfer Cycle

A Split Read Transfer Cycle loads 256 words of 4 bits of data from a selected row of the split RAM into the corresponding non active half of the split SAM, with serial data being shifted out of the active half of the SAM simultaneously.

During Split Read Transfer operation, the RAM input



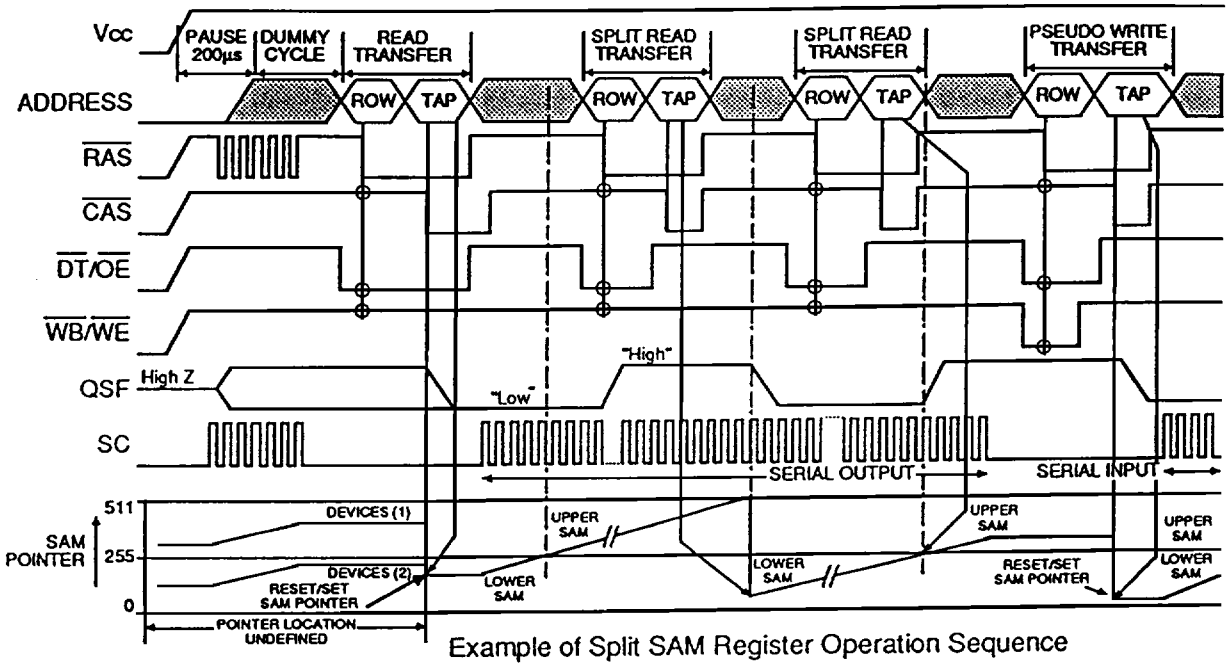
clocks do not have to be synchronized with the SC clock, thus eliminating timing restrictions as in the case of on-the-fly transfers. A Spit Read Transfer can be performed once the delay of tSTS after the change of state of QSF has been satisfied as shown below:



Split Register Operation Sequence

A normal non split Read Transfer ***MUST*** precede Split Read Transfer Cycles, and the following waveform illustrates the split register sequence after the MVM4259 is powered up and initialized. Initialization consists of a minimum of 8 RAS and 8 SC clock cycles. A Read Transfer is now performed, and the column address which is latched at the falling edge of CAS sets the SAM tap pointer location which was until that point undefined.

Now pointer address can be incremented by cycling SC from the starting location to the last location in the SAM (address 511), at which point it wraps around to the tap location set by the Split Read Transfer performed on the inactive half (here the lower) of the SAM while the active half (the upper) was being accessed. The SAM address is incremented as long as SC is clocked. Then, the next Split Read Transfer sets a new tap location in the inactive (upper) half of the SAM (in the example location 256) and the pointer is incremented from this location by the SC clock.

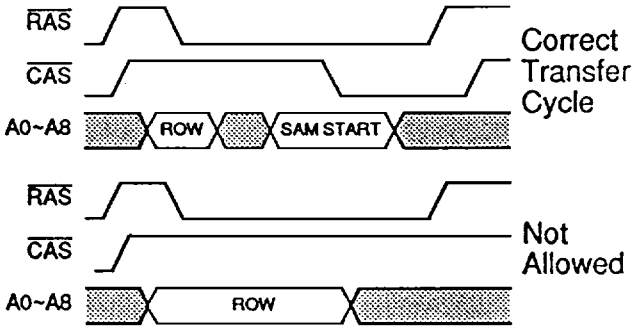


Example of Split SAM Register Operation Sequence

The next operation is a Pseudo Write Transfer which switches the SAM from output to input mode in preparation for either Write or Split Write Transfers. The column address latched at the falling edge of CAS during this cycle sets a new SAM tap location, and serial data will be written into the SAM starting from this tap point.

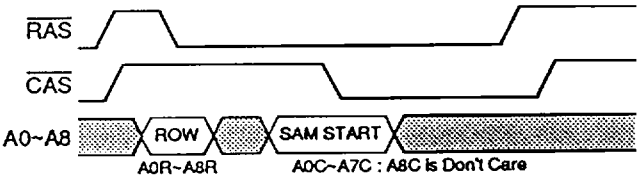
Transfer Operations Without CAS

During all transfer cycles CAS must be cycled to latch the column address at CAS fall; this sets the new tap location. If CAS was held high during a transfer cycle, the SAM pointer location would be undefined, and so a **transfer cycle with CAS high is not allowed** - see the following examples.

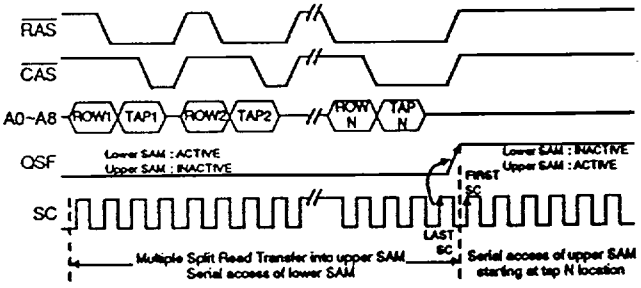


Tap Location Selection In Split Read Transfers

In a Split Read Transfer operation, the column address A0~A7 is latched at the falling edge of CAS to set the tap point in the inactive half of the SAM. A8 is controlled internally, and so is ignored at the falling edge of CAS. During a split transfer, the tap point cannot be set to the last location of either half of the split SAM (A0~A7=FF_H).

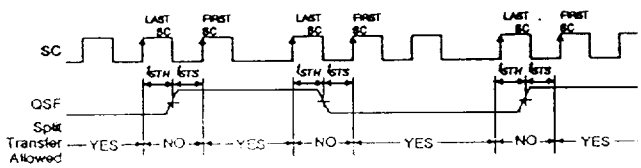


In multiple Split Read Transfers performed into the same split SAM register, the tap location set during the last Split Read Transfer, before QSF changes state, will prevail. The example below shows multiple Split Read Transfers into the upper (non active) SAM, while the lower (active) SAM is being accessed at the time when QSF toggles. Here, the first SC clock will start shifting serial data from the tap N address location.



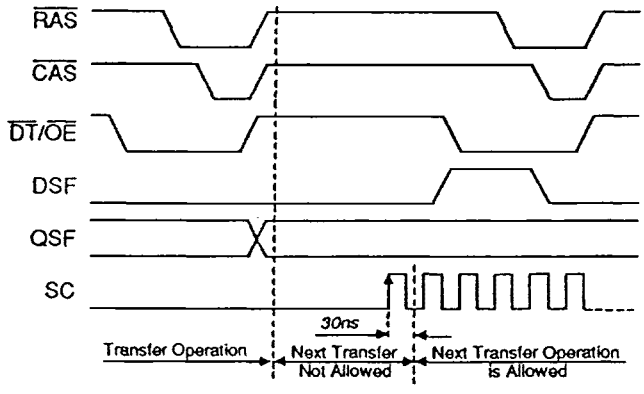
Split Read Transfer Operation Allowable Period

The following waveform shows the relationship between the SC clock and the QSF pin during Split Read Transfers and highlights the times when Split Read Transfers are allowed.



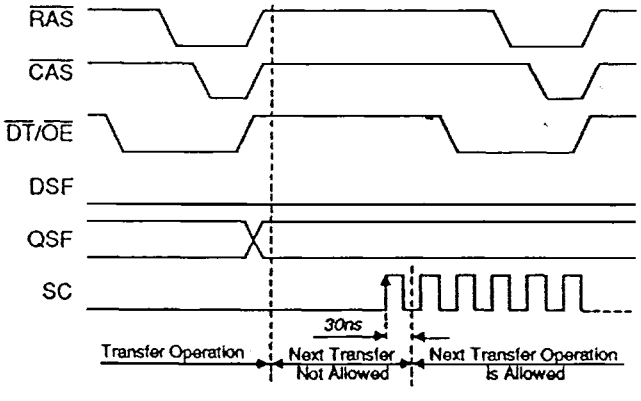
Split Read Transfers After Normal Read Transfers

A Split Read Transfer may be executed after a normal Read Transfer provided that a minimum delay of 30 ns is allowed from the rising edge of the first SC clock - see waveform below.



Normal Read Transfers After a Read Transfer Cycle

Another Read Transfer may be performed following a Read Transfer providing that a minimum of 30 ns from the rising edge of the first SC clock is satisfied as shown below:



Power Up Initialisation

At switch on, the RAS and DT/OE must be high before or at the same time as V_{CC} reaches its final value. After power up, a pause of 200 µs minimum is required with RAS and DT/OE held high. After this pause, a minimum of 8 RAS and 8 SC dummy cycles must be performed to stabilize the internal circuitry of the MVM4259 before valid Read, Write or Transfer operations can begin. During this initialization period, DT/OE must be held high. (If the internal refresh counter is used, a minimum of 8 CAS Before RAS initialization cycles are required instead of 8 RAS cycles.)

Initial State After Power Up

When power up is achieved with RAS, CAS, DT/OE and WB/WE held high, the internal state of the MVM4259 is as follows:

	State After Power Up
SAM Port	Input Mode
QSF Pin	High Impedance
Colour Register	All bits = 0
Mask Register	Write Enable
TAP Pointer	Invalid

However, for any other power up conditions and signal levels the internal states cannot be guaranteed. To achieve correct device operation it is recommended that the initial state be set by the user after the device is initialised by a 200µs pause followed by a minimum of 8 RAS cycles and 8 SC cycles and before valid operations begin.

MVM4259 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage on any pin except W/IO and SIO	V_{T1}	-1 V to +7	V
Voltage on W/IO and SIO	V_{T2}	-1 V to +V_{CC}+1	V
Power Dissipation	P_T	1.0	W
Operating Free air Temperature range	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics(T_A= -55 to +125°C, V_{CC}= 5V±10%)

Parameter	*Symbol*	*Test Conditions RAM Port* (1)	*Test Conditions SAM Port* (1)	*-10 max*	*-12 max*	*Unit*
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	90	75	mA
	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IL} SC cycling	130	115	mA
$\overline{RAS}$-only Refresh	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	$\overline{SE}$ = V_{IH}, SC = V_{IL}	90	75	mA
	I_{CC9}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}	$\overline{SE}$ = V_{IL}, SC cycling	130	115	mA
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	I_{CC5}	$\overline{RAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	90	75	mA
	I_{CC11}	$\overline{RAS}$ cycling	$\overline{SE}$ = V_{IL}, SC cycling	130	115	mA
Page-mode Current (1)	I_{CC4}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	80	65	mA
	I_{CC10}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IL}, SC cycling	120	100	mA
Data Transfer Current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	110	95	mA
	I_{CC12}	$\overline{RAS}$, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IL}, SC cycling	150	135	mA
Block Write Current	I_{CC13}	$\overline{RAS}$, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	100	85	mA
	I_{CC14}	$\overline{RAS}$, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IL}, SC cycling	140	125	mA
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	$\overline{SE}$ = V_{IH}, SC = V_{IL}	10	10	mA
	I_{CC8}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	$\overline{SE}$ = V_{IL}, SC cycling	50	50	mA
Input Leakage Current	I_{LI}	V_{IN}= 0 to +5.8V, V_{CC} = 5.5V		±10	±10	µA
Output Leakage Current	I_{IO}	V_{OUT}= 0 to V_{CC}, V_{CC} = 5.5V, D_{OUT} is disabled		±10	±10	µA

Notes (1) Where applicable, t_{RC} = minimum and t_{SCC}=minimum.

Capacitance (V_{CC}=5V±10%,T_A=25°C) Capacitance calculated, not measured.

Parameter		*Symbol*	*typ*	*max*	*Unit*
Input Capacitance:	Address, Clocks	C_I	-	7	pF
I/O Capacitance:	Data In/Out	$C_{I/O}$	-	9	pF
Output Capacitance:	QSF pin	C_O	-	9	pF

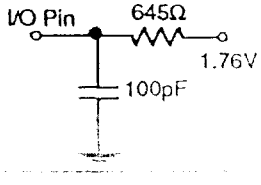
Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V
Output High Voltage, I_{OH} = -2.0 mA	V_{OH}	2.4	-	-	V
Output Low Voltage, I_{OL} = 2.0 mA	V_{OL}	-	-	0.4	V
Output Low Voltage, I_{OL} = 6.0 mA, QSF pin	V_{OLQ}	-	-	0.4	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I suffix)
	T_{AM}	-55	-	125	°C (M, MB suffix)

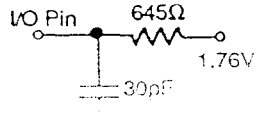
AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* I/P and O/P timing reference levels: 2.0V, 1.0V
* Output load: see diagrams below

Output Load - RAM



Output Load - SAM



AC Timing Parameters

Parameter	Symbols	-10 min	-10 max	-12 min	-12 max	Unit	Notes
Random Read or Write cycle time	t_{RC}	180	-	210	-	ns	
Read-modify-write cycle time	t_{RMW}	235	-	280	-	ns	
Fast Page Mode cycle time	t_{PC}	55	-	70	-	ns	
Fast Page-mode read-modify-write cycle time	t_{PRMW}	100	-	125	-	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	100	-	120	ns	8,14
Access time from column address	t_{AA}	-	50	-	60	ns	8,14
Access time from $\overline{CAS}$	t_{CAC}	-	25	-	25	ns	8,15
Access time from $\overline{CAS}$ Precharge	t_{CPA}	-	50	-	60	ns	8,15
Output Buffer turn off Delay	t_{OFF}	0	20	0	20	ns	10
Transition time (Rise and Fall)	t_T	3	35	3	35	ns	7
Pulse duration, $\overline{RAS}$ high	t_{RP}	70	-	80	-	ns	
Pulse duration, $\overline{RAS}$ low	t_{RAS}	100	10^4	120	10^4	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode only)	t_{RASP}	100	10^5	120	10^5	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	-	25	-	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	-	120	-	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10^4	25	10^4	ns	
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	t_{RCD}	20	75	20	90	ns	14
$\overline{RAS}$ to Column Address Delay time	t_{RAD}	15	50	15	65	ns	14
Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50	-	60	-	ns	
Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	10	-	10	-	ns	
Pulse duration, $\overline{CAS}$ high	t_{CPN}	10	-	10	-	ns	
Pulse duration, $\overline{CAS}$ high (Fast Page Mode)	t_{CP}	10	-	10	-	ns	
Row address setup time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	12	-	12	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	ns	
Column address hold time after $\overline{CAS}$ low	t_{CAH}	15	-	15	-	ns	
Column address hold time after $\overline{RAS}$ low	t_{AR}	70	-	80	-	ns	
Read command setup time	t_{RCS}	0	-	0	-	ns	
Read Command hold time	t_{RCH}	0	-	0	-	ns	11
Read Command hold time referenced to $\overline{RAS}$	t_{RRH}	0	-	0	-	ns	11
Write Command hold time	t_{WCH}	15	-	15	-	ns	
Write Command hold time referenced to $\overline{RAS}$	t_{WCR}	70	-	85	-	ns	
Write Command pulse width	t_{WP}	15	-	15	-	ns	
Write setup time before $\overline{RAS}$ high	t_{RWL}	25	-	30	-	ns	
Write setup time before $\overline{CAS}$ high	t_{CWL}	25	-	30	-	ns	
Data Set up time	t_{DS}	0	-	0	-	ns	12
Data hold time	t_{DH}	15	-	15	-	ns	12
Data hold time after $\overline{RAS}$ low	t_{DHR}	70	-	85	-	ns	
Early write command setup time before $\overline{CAS}$ low	t_{WCS}	0	-	0	-	ns	13
Delay time, $\overline{RAS}$ low to $\overline{WE}$ low	t_{RWD}	130	-	155	-	ns	13
Delay time, column address to $\overline{WE}$ low	t_{AWD}	80	-	100	-	ns	13
Delay time, $\overline{CAS}$ low to $\overline{WE}$ low	t_{CWD}	55	-	65	-	ns	13

AC Timing Parameters

Parameter	Symbols	-10 min	-10 max	-12 min	-12 max	Unit	Notes
Data to $\overline{CAS}$ delay time	t_{DZC}	0	-	0	-	ns	
Data to $\overline{OE}$ delay time	t_{DZO}	0	-	0	-	ns	
Access time from $\overline{OE}$ low	t_{OEA}	-	25	-	30	ns	8
Output Buffer turn off delay from $\overline{OE}$	t_{OEZ}	0	20	0	20	ns	10
$\overline{OE}$ to Data delay time	t_{OED}	20	-	30	-	ns	
$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	20	-	30	-	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15	-	15	-	ns	
CAS set up time for $\overline{CAS}$ before $\overline{RAS}$ cycle	t_{CSR}	10	-	10	-	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ cycle	t_{CHR}	10	-	10	-	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ active time	t_{RPC}	0	-	0	-	ns	
Refresh time interval, RAM	t_{REF}	-	8	-	8	ms	
$\overline{WB}$ setup time before $\overline{RAS}$ low	t_{WSR}	0	-	0	-	ns	
$\overline{WB}$ hold time	t_{RWH}	15	-	15	-	ns	
DSF setup time before $\overline{RAS}$ low	t_{FSR}	0	-	0	-	ns	
DSF hold time referenced to $\overline{RAS}$ (1)	t_{RFH}	15	-	15	-	ns	
DSF hold time referenced to $\overline{RAS}$ (2)	t_{FHR}	70	-	85	-	ns	
DSF setup time before $\overline{CAS}$ low	t_{FSC}	0	-	0	-	ns	
DSF hold time after $\overline{CAS}$ low	t_{CFH}	15	-	15	-	ns	
Mask data set up time	t_{MS}	0	-	0	-	ns	
Mask data hold time	t_{MH}	15	-	15	-	ns	
$\overline{DT}$ high setup time before $\overline{RAS}$ low	t_{THS}	0	-	0	-	ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ low	t_{THH}	15	-	15	-	ns	
$\overline{DT}$ low set up time	t_{TLS}	0	-	0	-	ns	
$\overline{DT}$ low hold time	t_{TLH}	15	10^4	15	10^4	ns	
$\overline{DT}$ low hold time referenced to $\overline{RAS}$	t_{RTH}	80	10^4	100	10^4	ns	
$\overline{DT}$ low hold time referenced to Column Address	t_{ATH}	30	-	30	-	ns	
$\overline{DT}$ low hold time referenced to $\overline{CAS}$	t_{CTH}	25	-	25	-	ns	
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ESR}	0	-	0	-	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{REH}	15	-	15	-	ns	
Delay time, $\overline{DT}$ high to $\overline{RAS}$ low	t_{TRP}	70	-	80	-	ns	
$\overline{DT}$ Precharge time	t_{TP}	30	-	40	-	ns	
$\overline{RAS}$ to First SC delay time (Read Transfer)	t_{RSD}	100	-	120	-	ns	
Column Address to First SC delay time (Read Transfer)	t_{ASD}	50	-	60	-	ns	
$\overline{CAS}$ to First SC delay time (Read Transfer)	t_{CSD}	25	-	25	-	ns	
Last SC to $\overline{DT}$ lead time (Real Time Read Transfer)	t_{TSL}	5	-	5	-	ns	
Delay time, $\overline{DT}$ high to SC high	t_{TSD}	15	-	15	-	ns	22
Last SC to $\overline{RAS}$ set up time (Serial Input)	t_{SRS}	30	-	30	-	ns	
Delay time, $\overline{RAS}$ high to SC high (Serial Input)	t_{SRD}	25	-	25	-	ns	
$\overline{RAS}$ to Serial Input delay time	t_{SDD}	50	-	50	-	ns	21
Serial Output Buffer turn off delay from $\overline{RAS}$	t_{SDZ}	10	50	10	50	ns	10
Serial clock cycle time	t_{SCC}	30	-	35	-	ns	
Pulse duration, SC high	t_{SC}	10	-	10	-	ns	

AC Timing Parameters

Parameter	Symbols	-10 min	-10 max	-12 min	-12 max	Unit	Notes
Pulse duration, SC low	t_{SCP}	10	-	10	-	ns	
Access time from SC high	t_{SCA}	-	25	-	25	ns	9
Serial Output hold time after SC high	t_{SOH}	5	-	5	-	ns	
Serial Input setup time before SC high	t_{SDS}	0	-	0	-	ns	
Serial Input hold time after SC high	t_{SDH}	15	-	15	-	ns	
Access time from $\overline{SE}$	t_{SEA}	-	25	-	25	ns	9
$\overline{SE}$ Pulse Width	t_{SE}	25	-	25	-	ns	
$\overline{SE}$ Precharge time	t_{SEP}	25	-	25	-	ns	
Serial output disable time from $\overline{SE}$ high	t_{SEZ}	0	20	0	20	ns	10
Serial input to $\overline{SE}$ delay time	t_{SZE}	0	-	0	-	ns	
Serial input to first SC delay time	t_{SZS}	0	-	0	-	ns	
Delay time, $\overline{SE}$ low to SC high	t_{SWS}	0	-	0	-	ns	
Serial Write Enable hold time	t_{SWH}	15	-	15	-	ns	
Serial Write Disable set up time	t_{SWIS}	0	-	0	-	ns	
Serial Write Disable hold time	t_{SWIH}	15	-	15	-	ns	
Split Transfer set up time	t_{STS}	30	-	30	-	ns	
Split Transfer hold time	t_{STH}	30	-	30	-	ns	
SC to QSF delay time	t_{SQD}	-	60	-	60	ns	16

NOTES:

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

(2) All voltages are referenced to GND.

(3) These parameters depend on the cycle rate.

(4) These parameters depend on the output loading. Specified values are measured with the output open.

(5) An initial pause of 200µs is required after power up, followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ high) and any 8 SC cycles before correct device operation is achieved. If the internal refresh counter is used, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialisation cycles instead of 8 $\overline{RAS}$ cycles are required.

(6) All measurements assume t_T = 5ns.

(7) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

(8) RAM port outputs are measured with the load specified under "AC Test Conditions".

(8) SAM port outputs are measured with the load specified under "AC Test Conditions".

(10) t_{OFF}, t_{OEZ}, t_{SEZ} and t_{SDZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

(11) Either t_{RCH} or t_{RRH} must be satisfied for Read Cycles.

(12) These parameters are referenced to the $\overline{CAS}$ leading edge in Early Write Cycles and to the $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$ controlled Write Cycles and Read-Modify-Write Cycles.

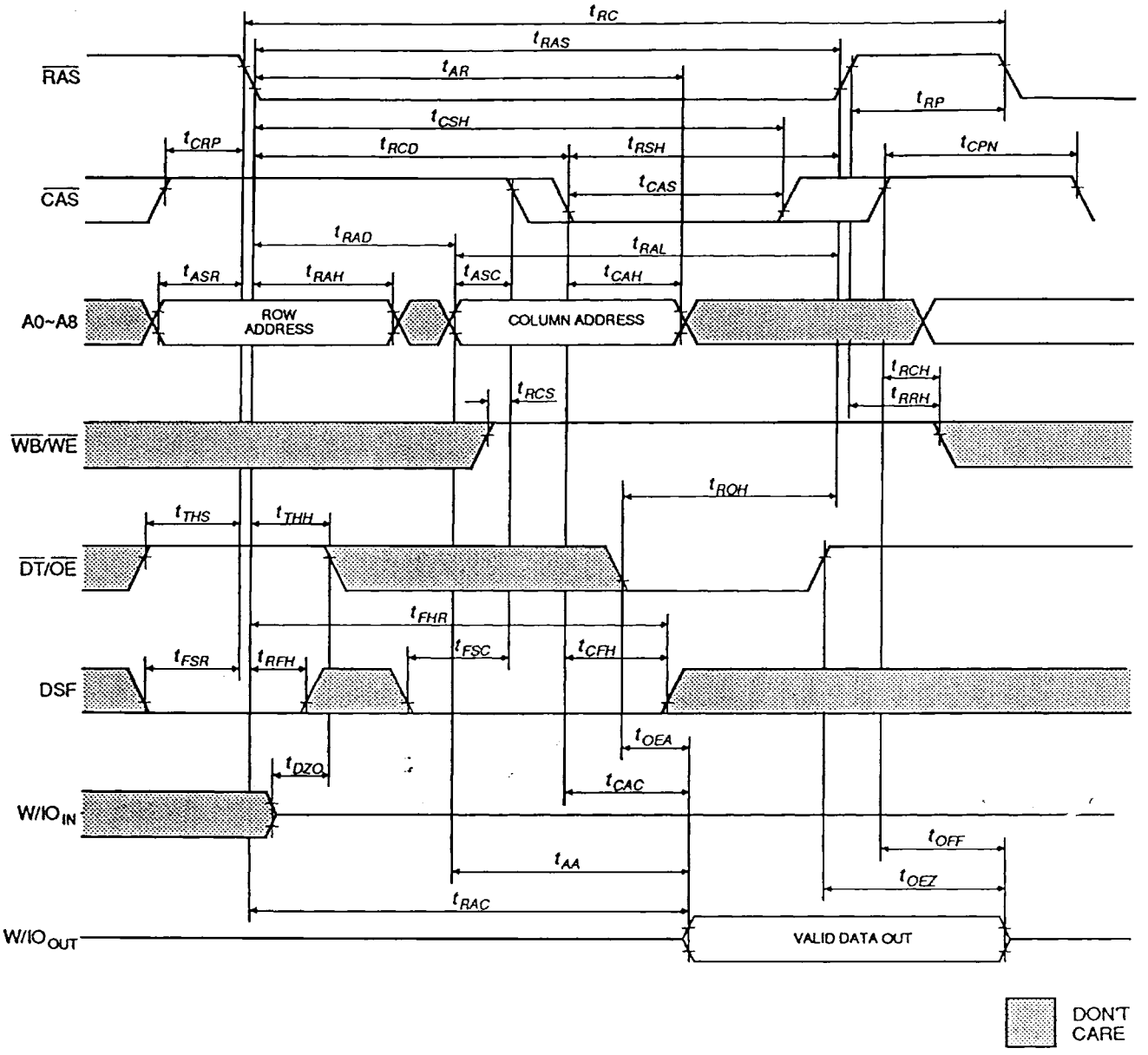
(13) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters; they are included here as electrical characteristics only. If $t_{AWD} \geq t_{AWD}$ (min), the cycle is an Early Write Cycle and the data out pins will remain in the high impedance state throughout the entire write cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a Read-Modify-Write Cycle and the data out will contain data read from the selected memory cell. If neither of the above sets of conditions are satisfied, the state of the data pins at access time is indeterminate.

(14) Operations with the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the maximum value, then access time is controlled by t_{CAC}.

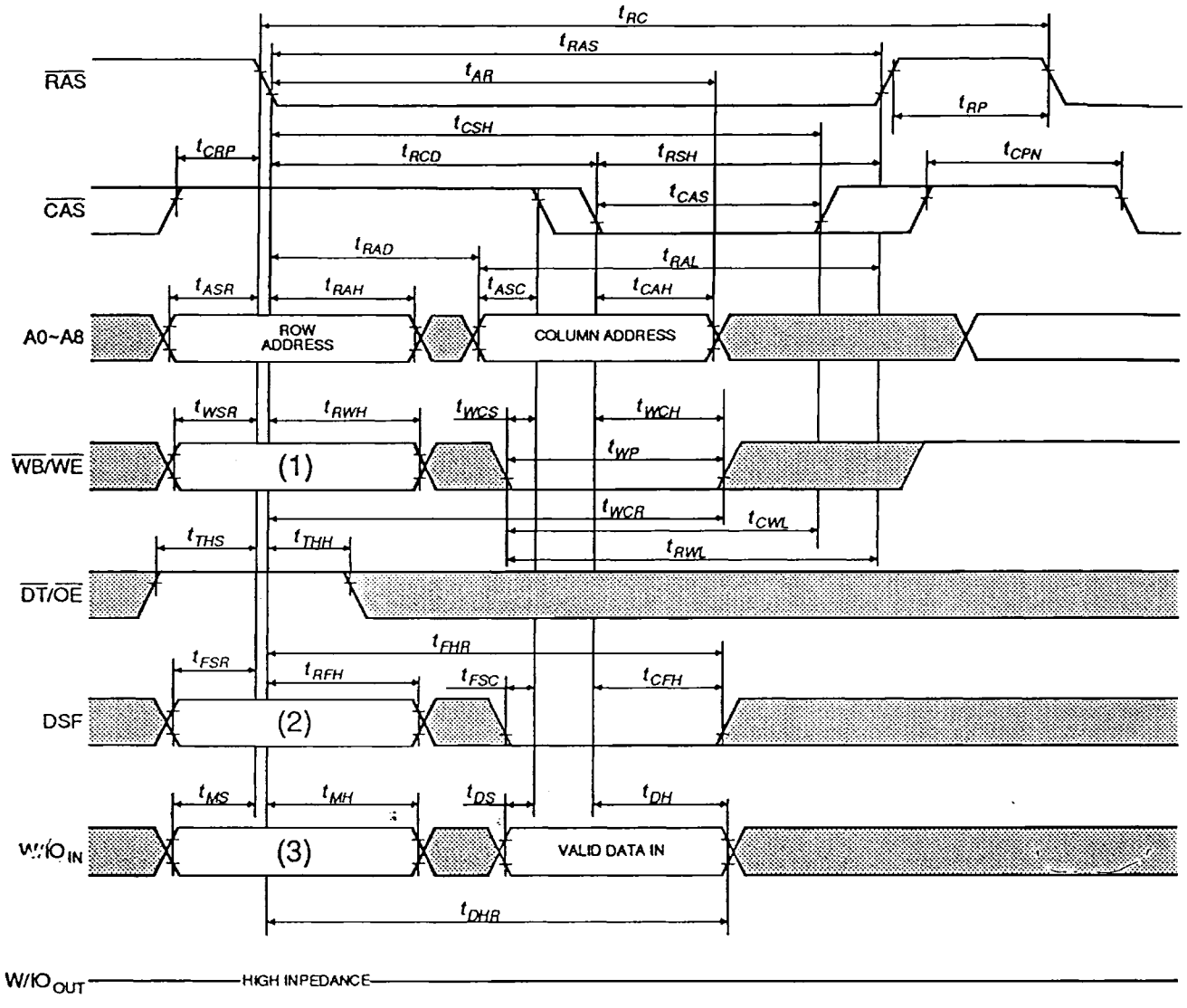
(15) Operations with the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the maximum value, then access time is controlled by t_{AA}.

(16) This parameter measurement assumes a pull up resistor of 820Ω

Read Cycle Timing



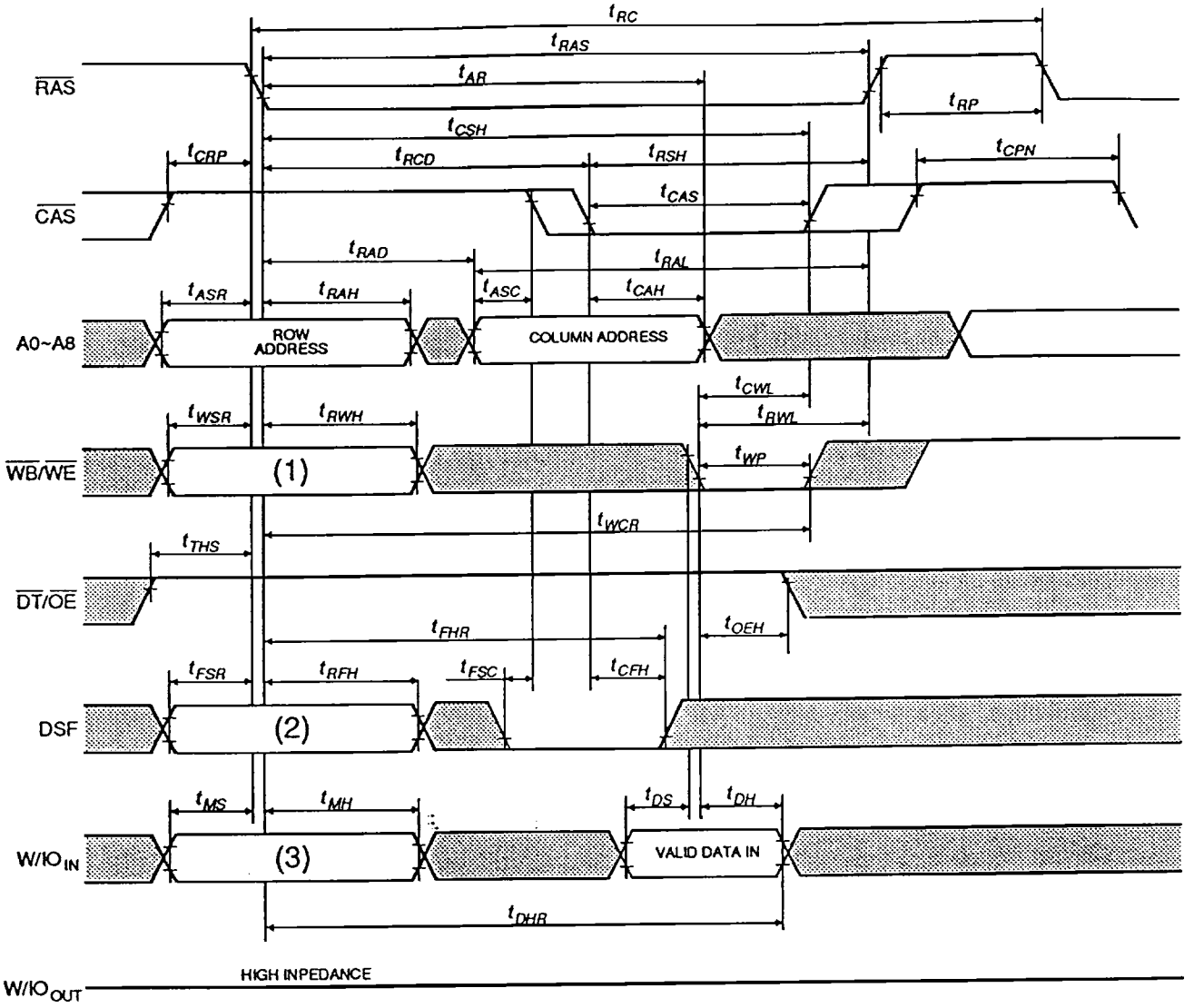
Early Write Cycle Timing



WRITE CYCLE STATE TABLE

CYCLE	STATE 1	STATE 2	STATE 3
Write mask Load/Use Write W/IOs to I/Os	L	L	WRITE MASK
Use Previous Write Mask, Write W/IOs to I/Os	L	H	X
Normal Early or Late Write Operation	H	L	X

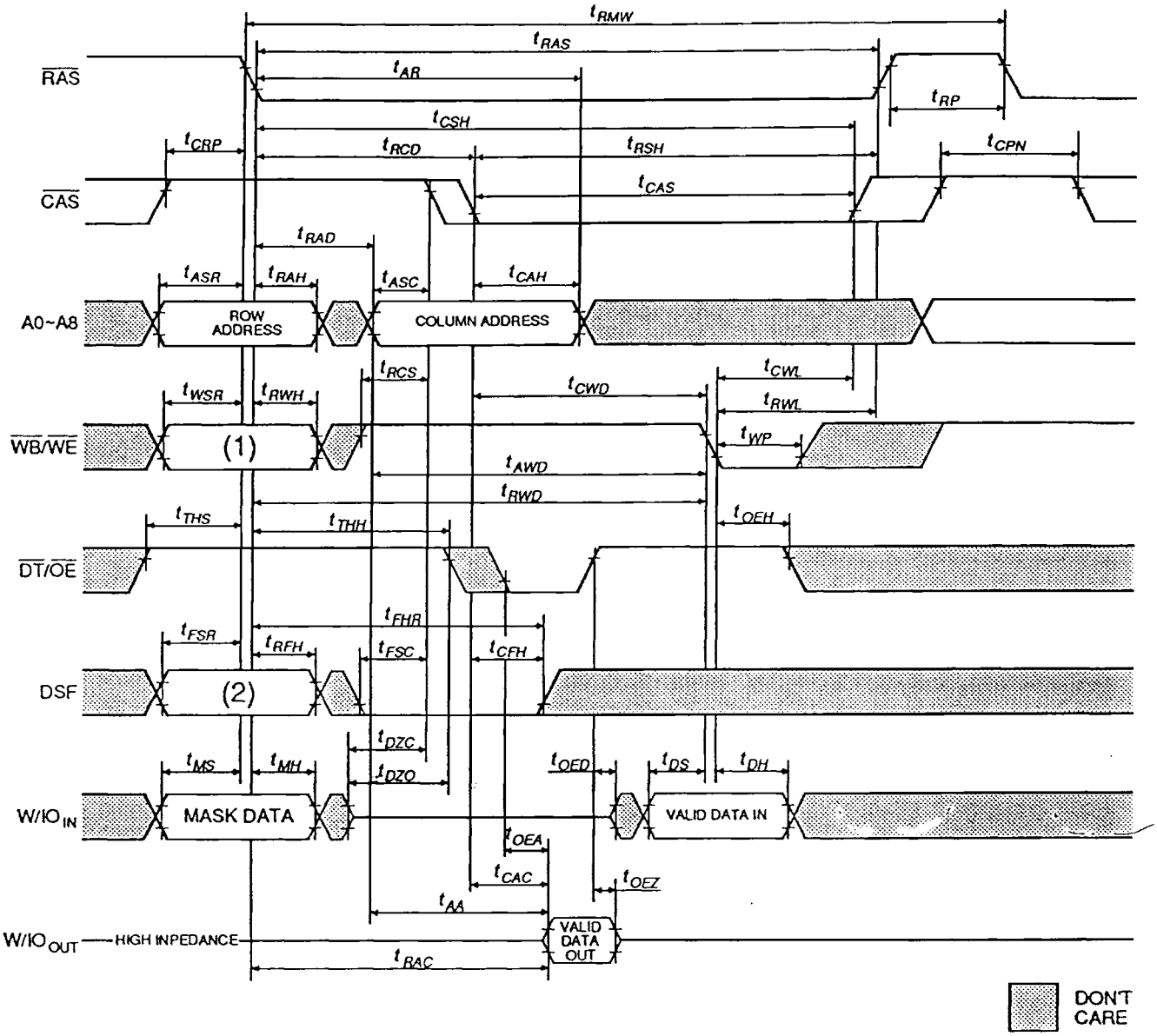
Write Cycle ($\overline{OE}$ Controlled) Timing



WRITE CYCLE STATE TABLE

CYCLE	STATE 1	STATE 2	STATE 3
Write mask Load/Use Write W/IOs to I/Os	L	L	WRITE MASK
Use Previous Write Mask, Write W/IOs to I/Os	L	H	X
Normal Early or Late Write Operation	H	L	X

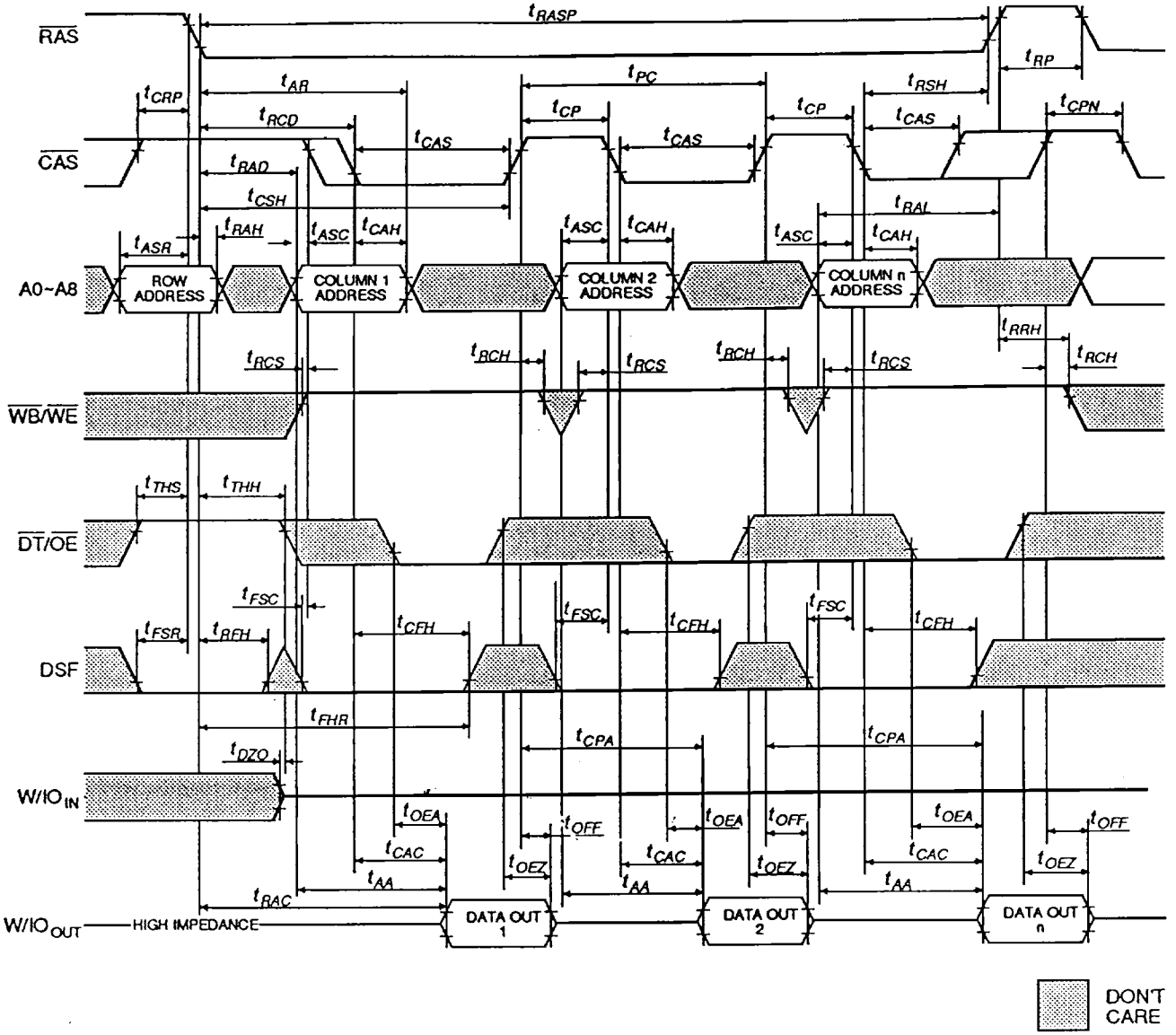
Read-modify-write Cycle Timing



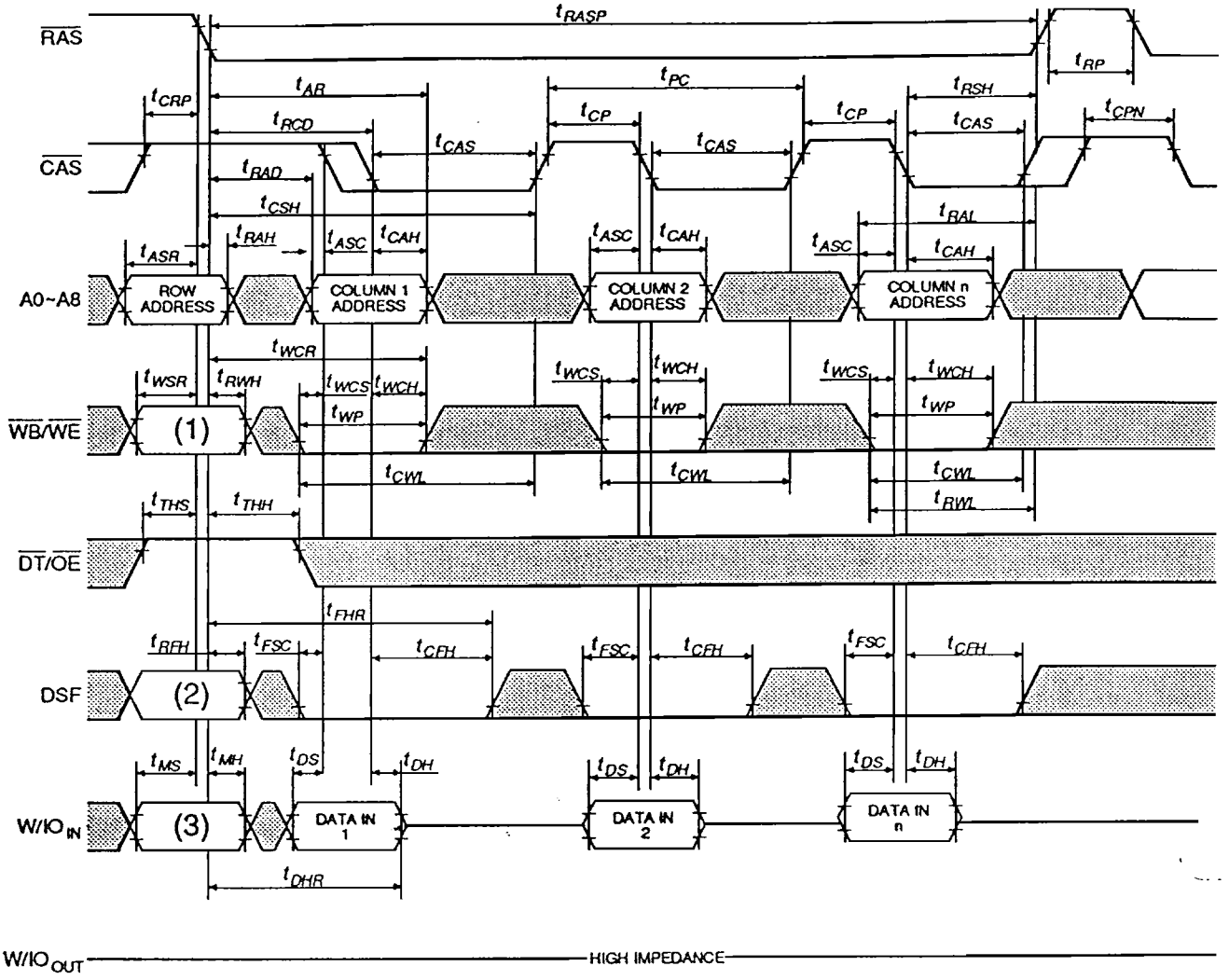
WRITE CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
Write mask Load/Use Write W/IOs to I/Os	L	L	WRITE MASK
Use Previous Write Mask, Write W/IOs to I/Os	L	H	X
Normal Early or Late Write Operation	H	L	X

Fast Page-mode Read Cycle Timing



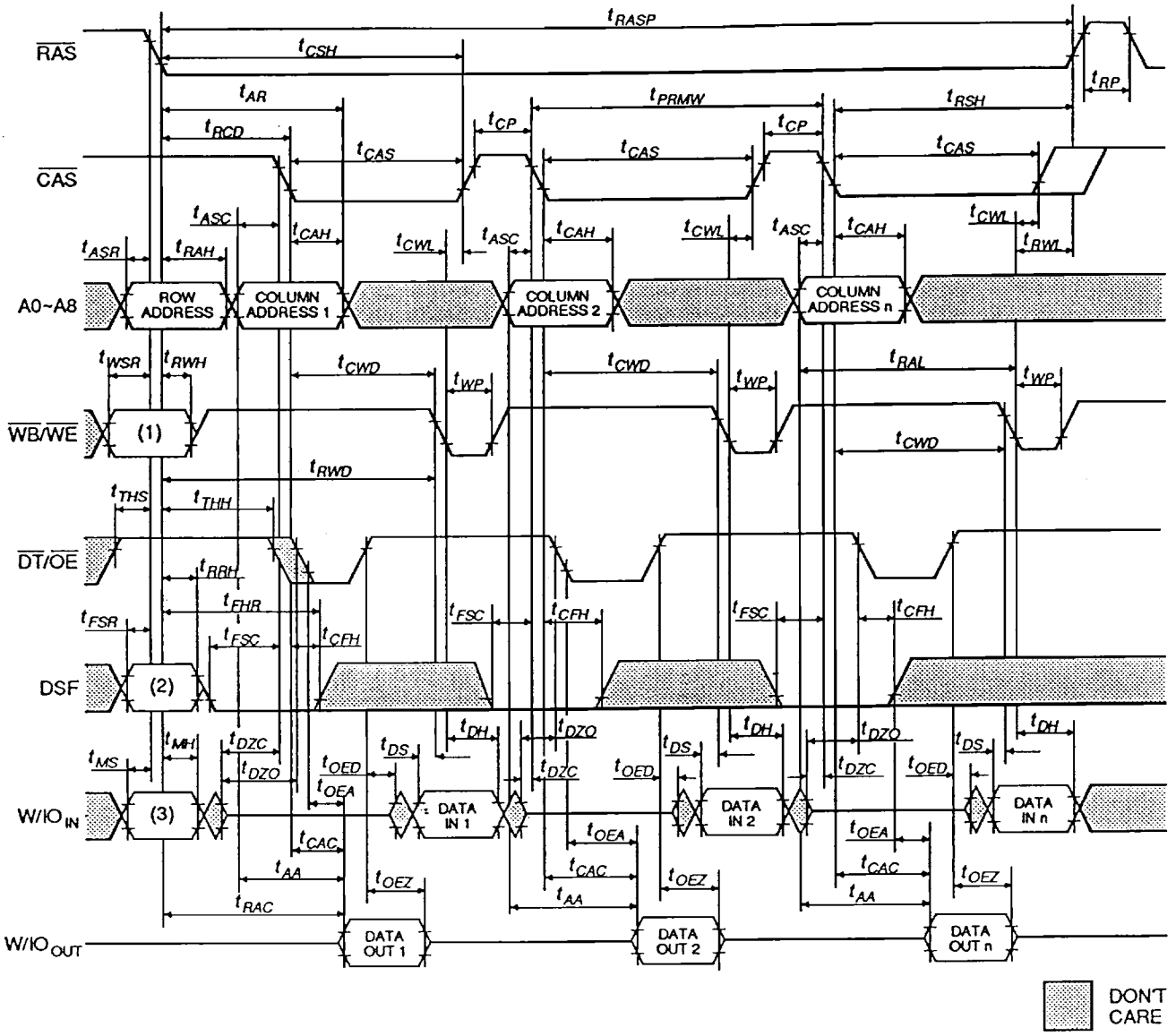
Fast Page-mode Write Cycle (Early Write) Timing



WRITE CYCLE STATE TABLE

CYCLE	STATE 1	STATE 2	STATE 3
Write mask Load/Use Write W/IOs to I/Os	L	L	WRITE MASK
Use Previous Write Mask, Write W/IOs to I/Os	L	H	X
Normal Early or Late Write Operation	H	L	X

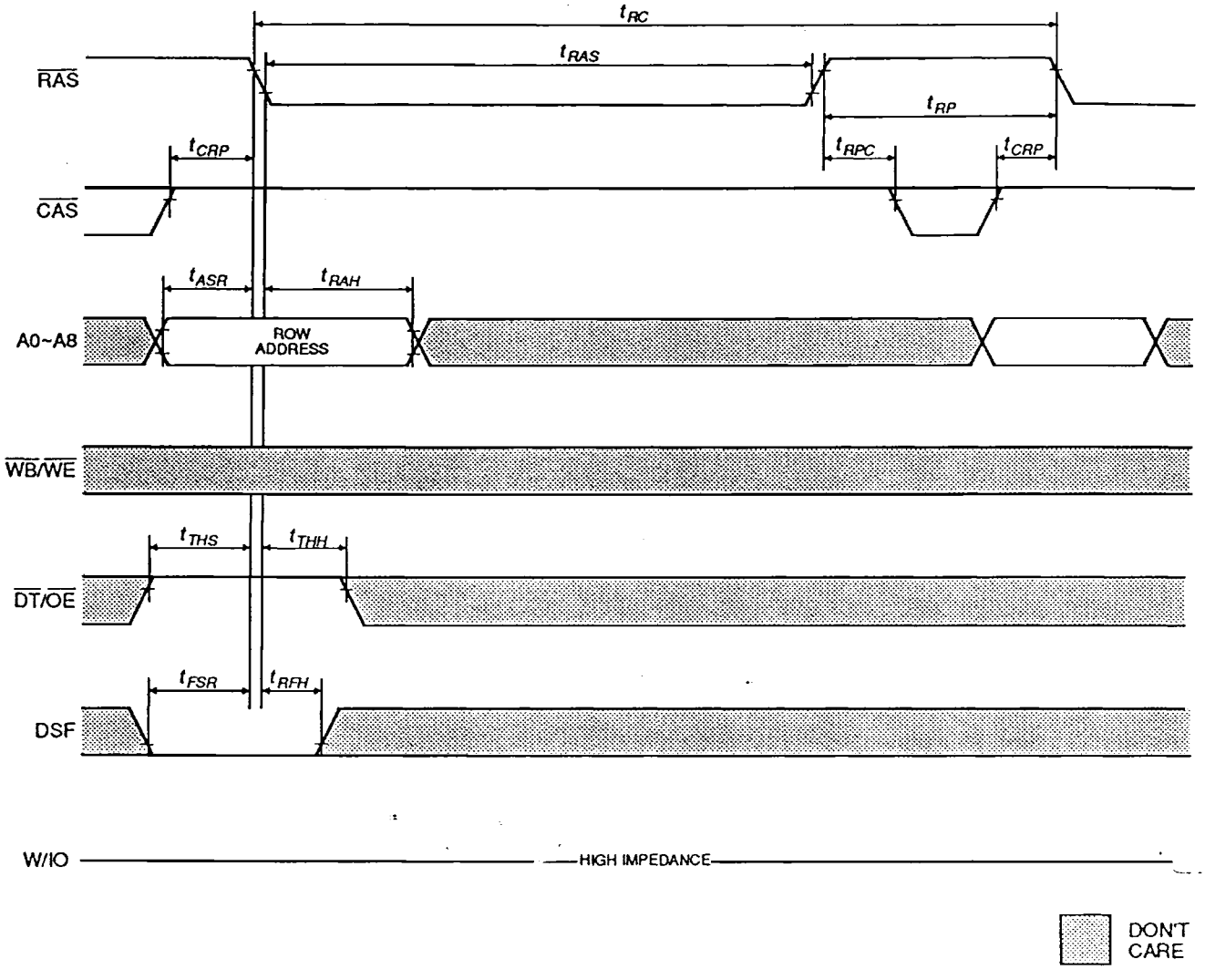
Fast Page-mode Read-modify-write Cycle Timing



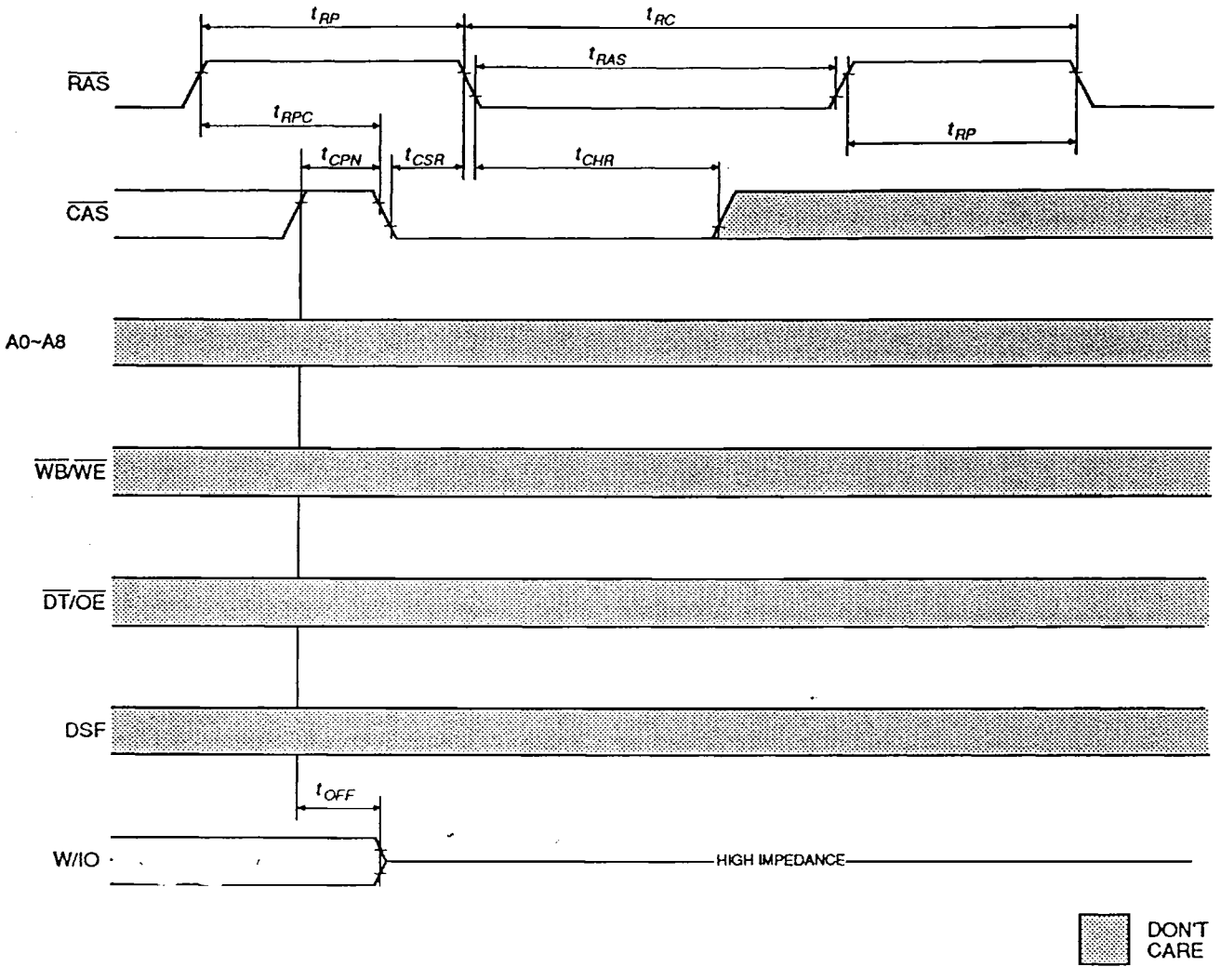
WRITE CYCLE STATE TABLE

CYCLE	STATE 1	STATE 2	STATE 3
Write mask Load/Use Write W/IOs to I/Os	L	L	WRITE MASK
Use Previous Write Mask, Write W/IOs to I/Os	L	H	X
Normal Early or Late Write Operation	H	L	X

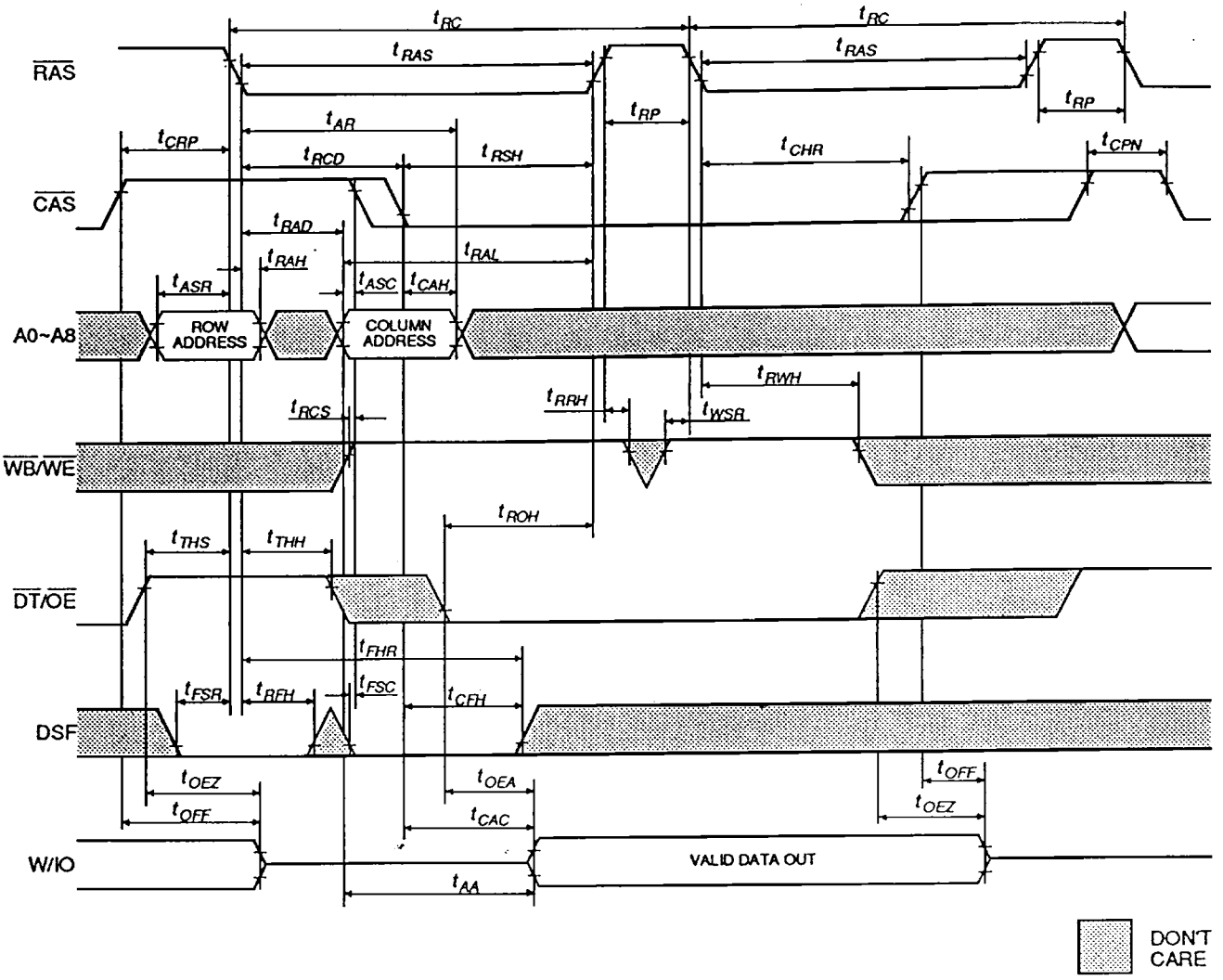
RAS-only Refresh Timing



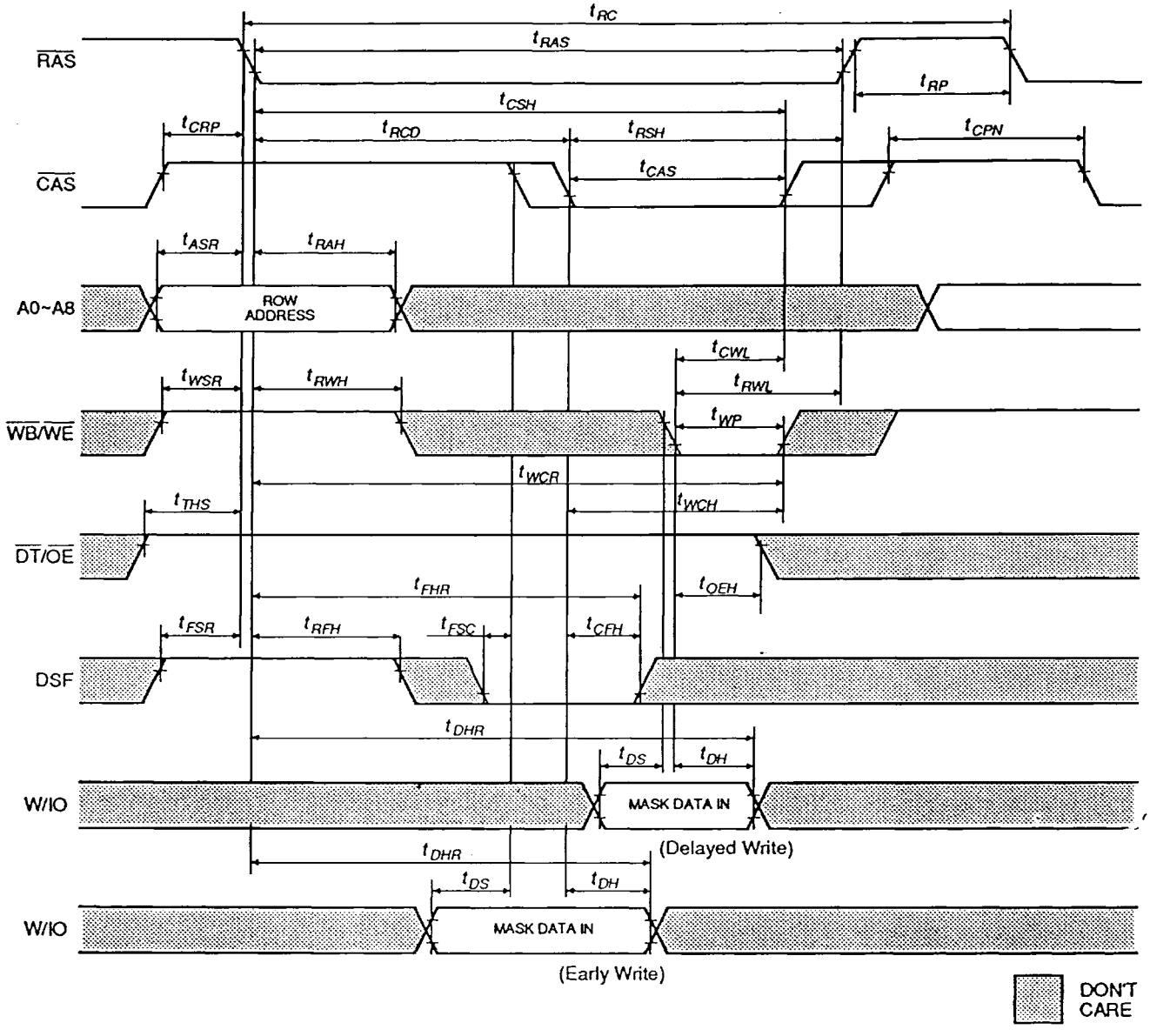
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Timing



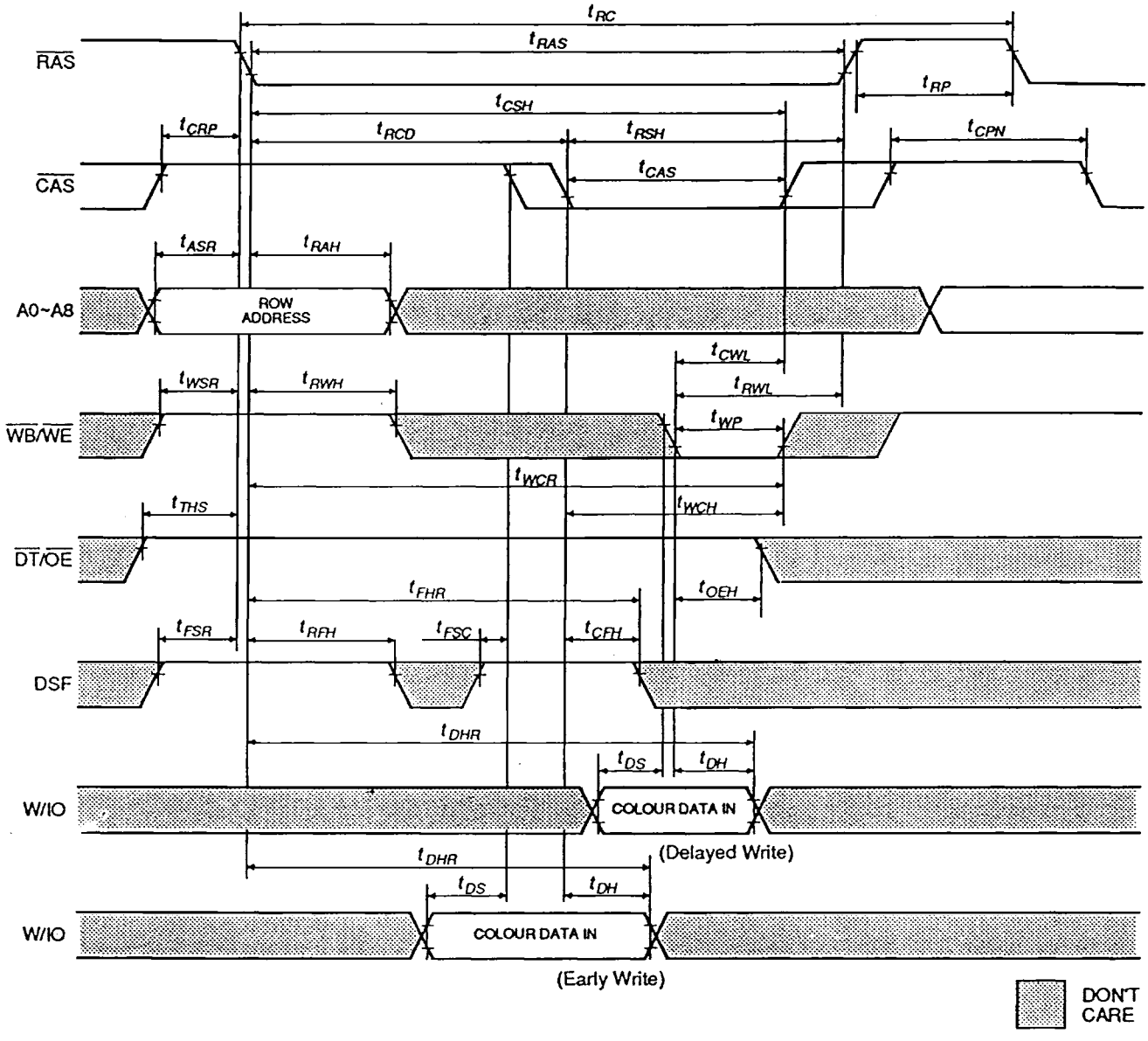
Hidden Refresh Cycle Timing



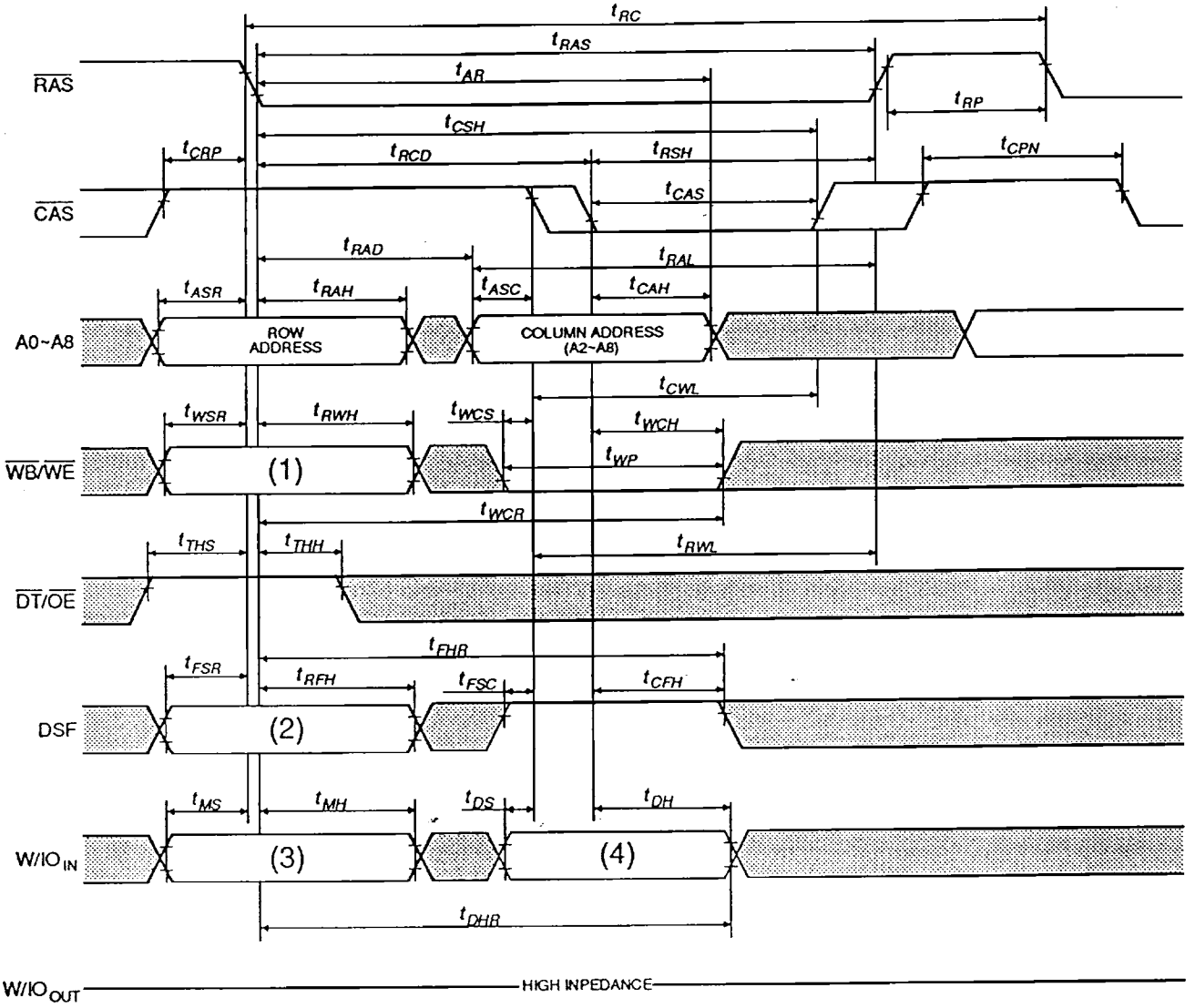
Load Mask Register Cycle Timing



Load Colour Register Cycle Timing



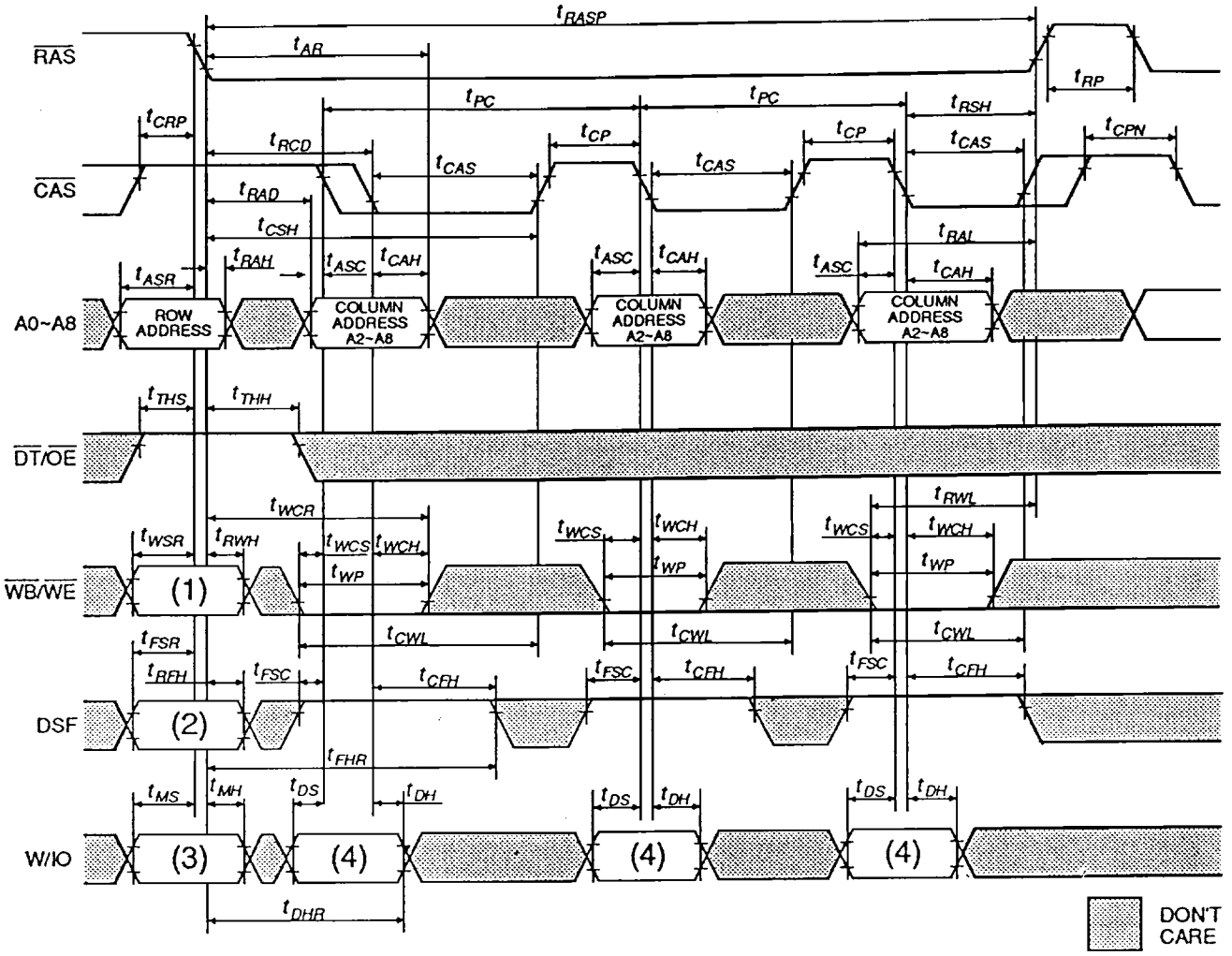
Block Write Cycle Timing



BLOCK WRITE CYCLE STATE TABLE

CYCLE	STATE					
	1	2	3	4		
Write Mask Load/Use Block Write	L	L	WRITE MASK	DATA PIN	A1	A0
				W1/IO1	0	0
Use Previous Write Mask, Block Write	L	H	X	W2/IO2	0	1
				W3/IO3	1	0
Write Mask Disabled, Block Write to all I/O's	H	L	X	W4/IO4	1	1

Page Mode Block Write Cycle Timing

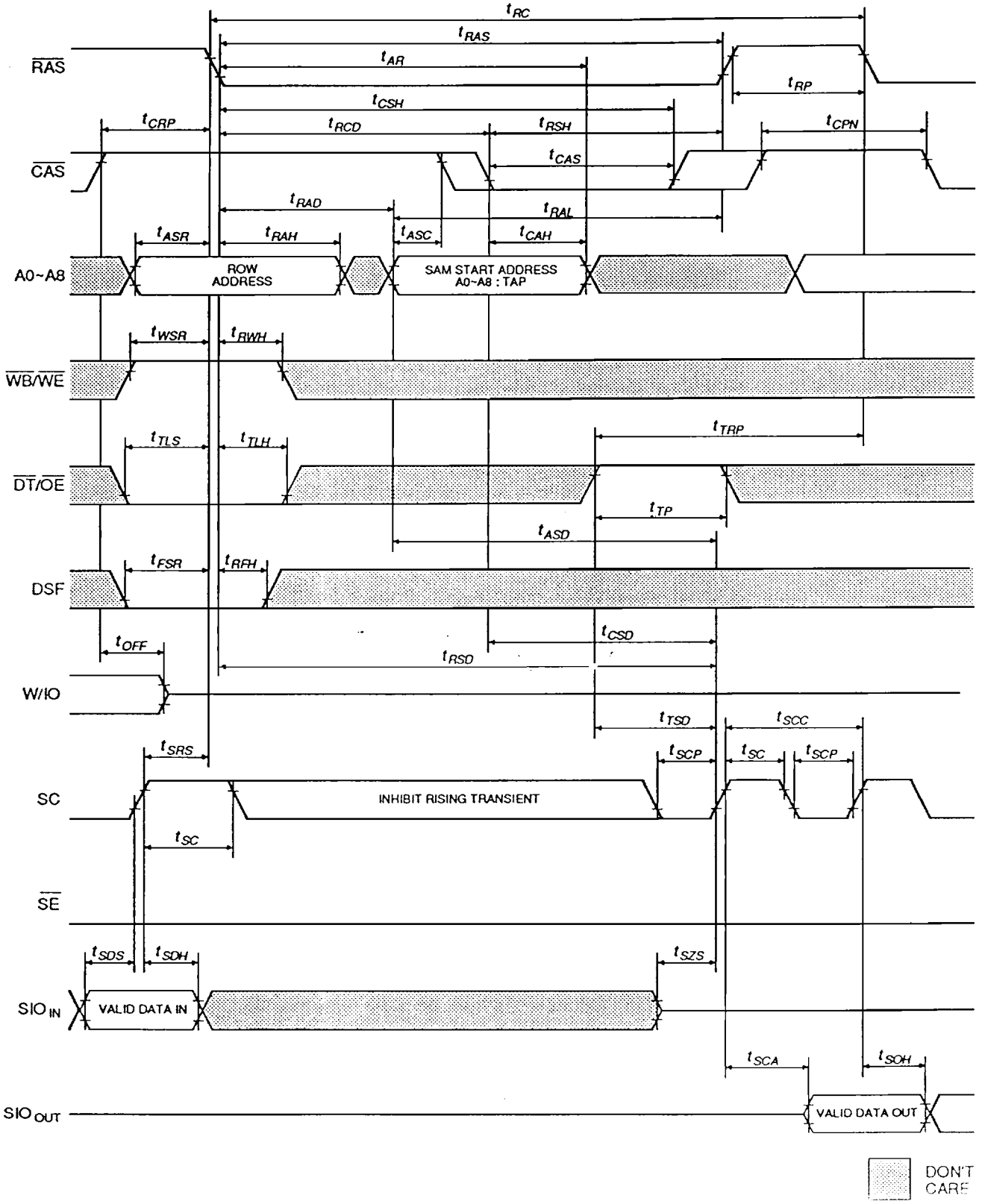


BLOCK WRITE CYCLE STATE TABLE

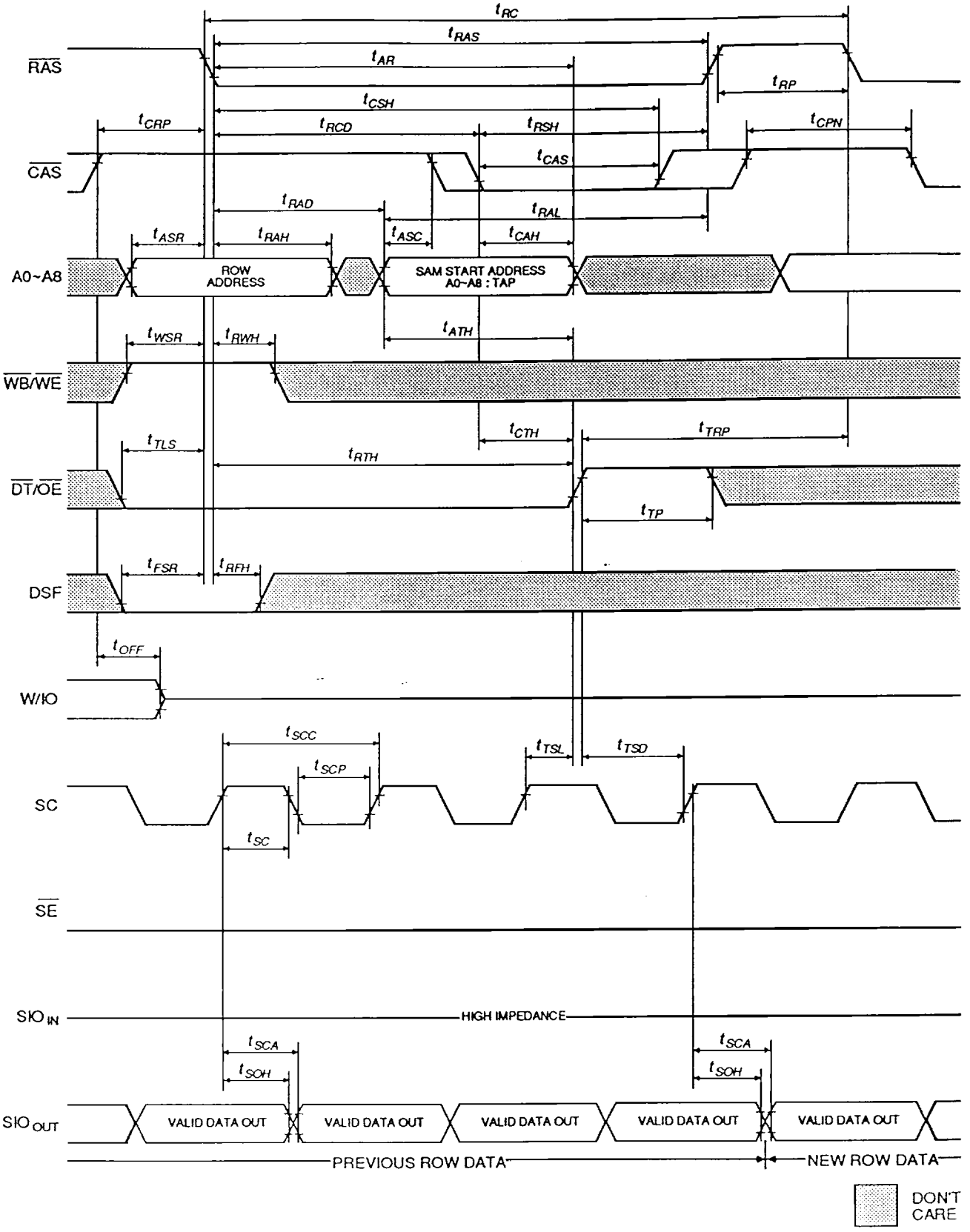
CYCLE	STATE 1	2	3	4		
				DATA PIN	A1	A0
Write Mask Load/Use Block Write	L	L	WRITE MASK	W1/IO1	0	0
Use Previous Write Mask, Block Write	L	H	X	W2/IO2	0	1
Write Mask Disabled, Block Write to all I/O's	H	L	X	W3/IO3	1	0
				W4/IO4	1	1

Read Transfer Cycle Timing

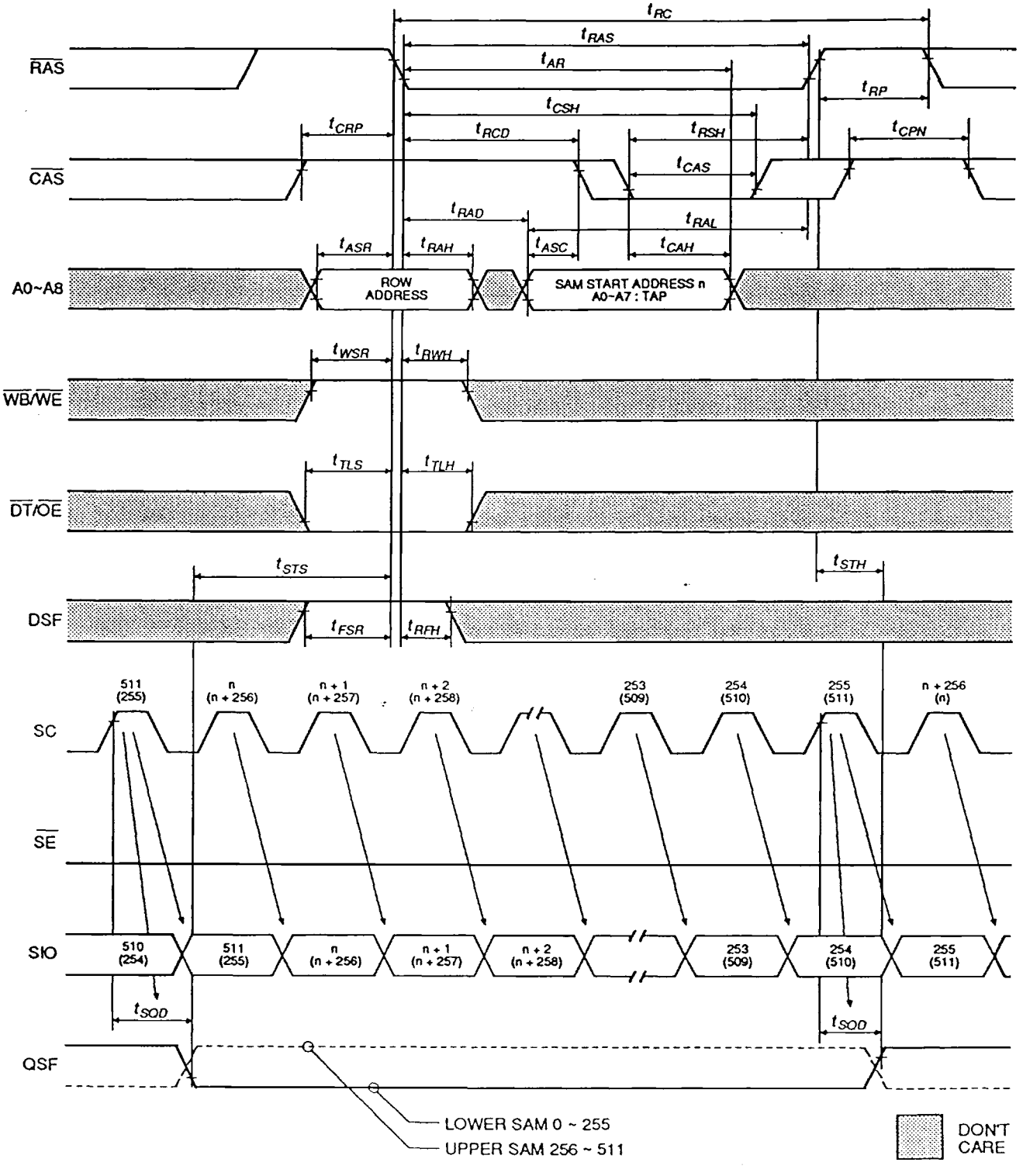
Note that the previous transfer must be a Write Transfer Cycle.



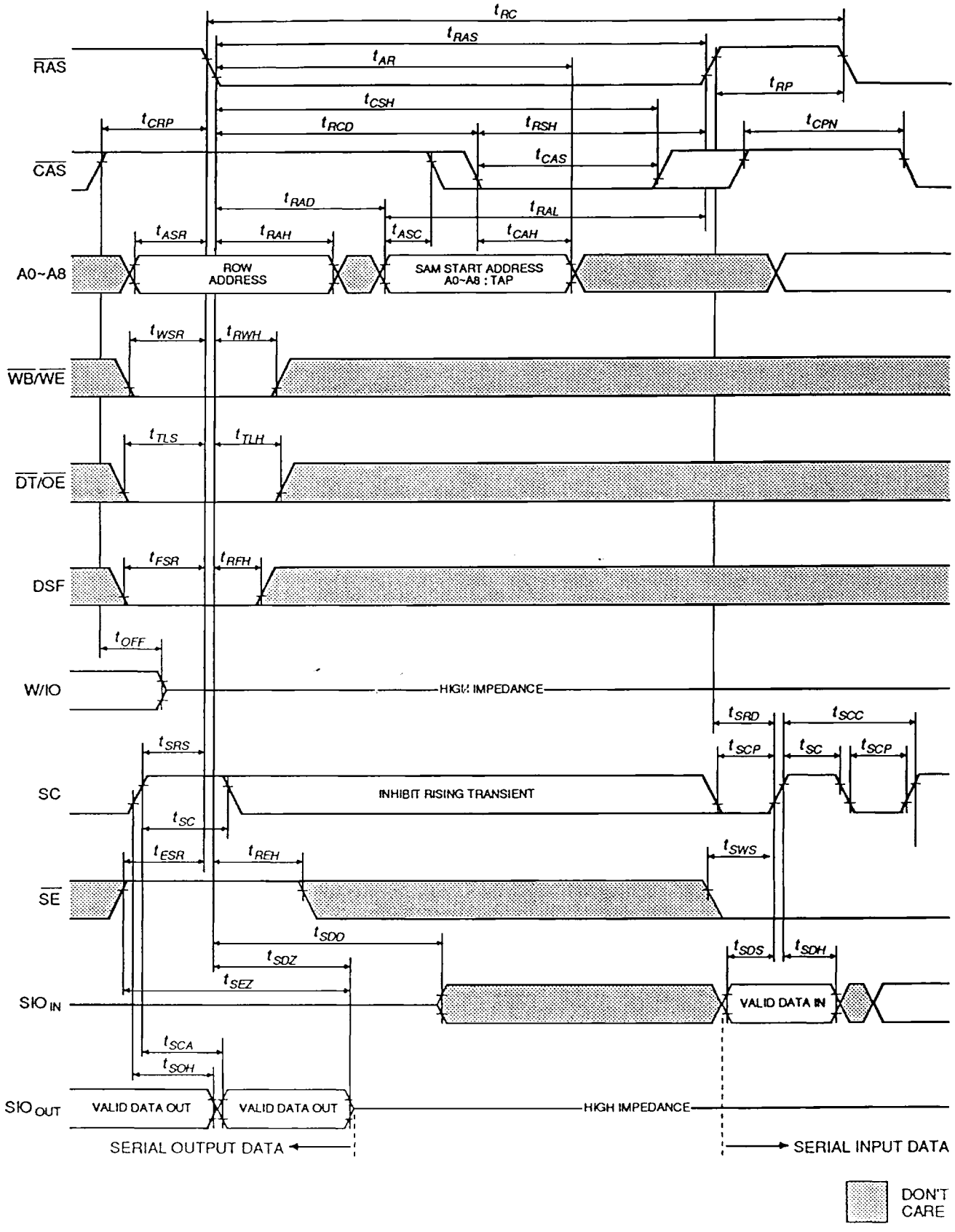
Real Time Read Transfer Cycle Timing



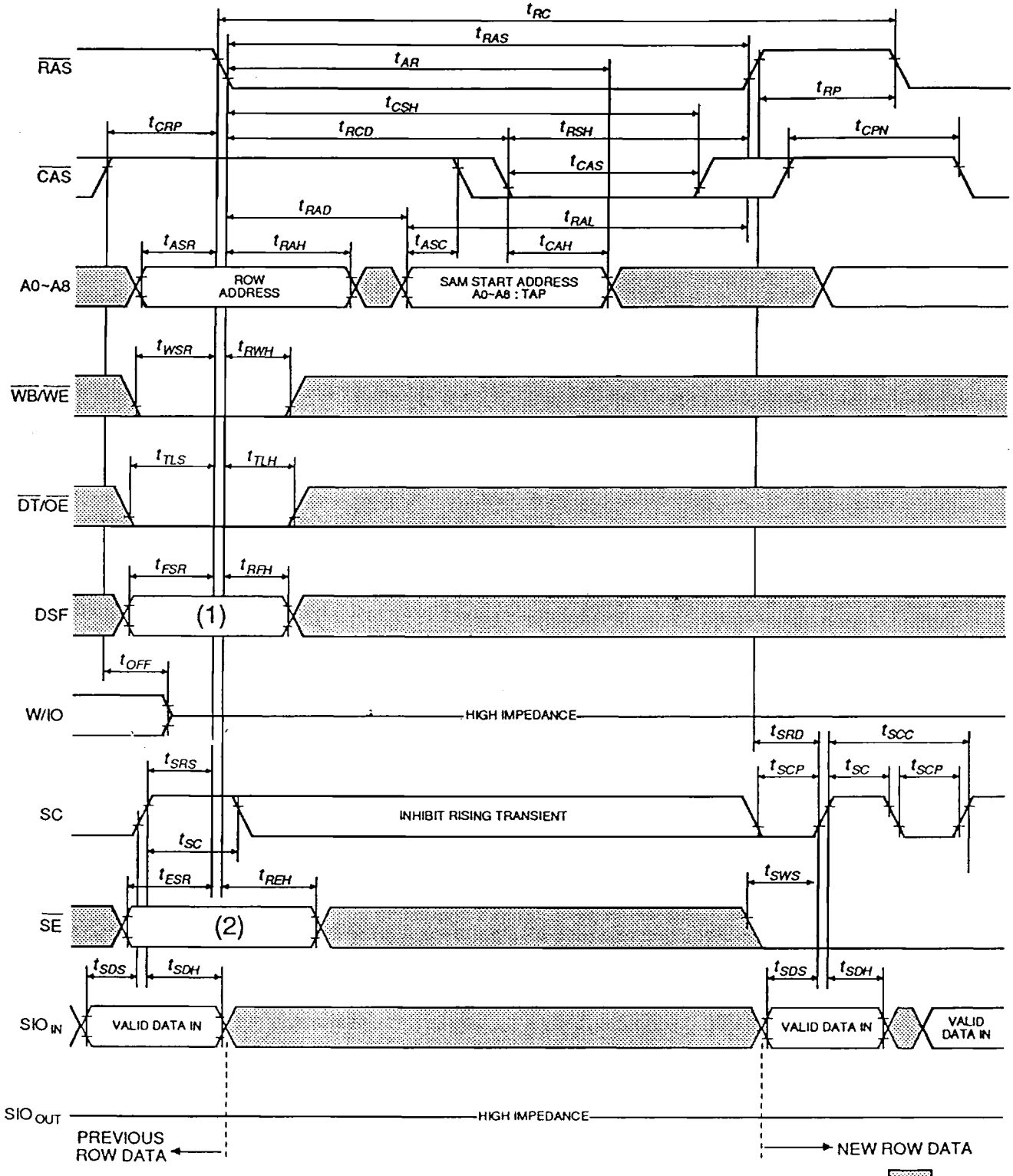
Split Read Transfer Cycle Timing



Pseudo Write Transfer Cycle Timing



Write Transfer Cycle Timing



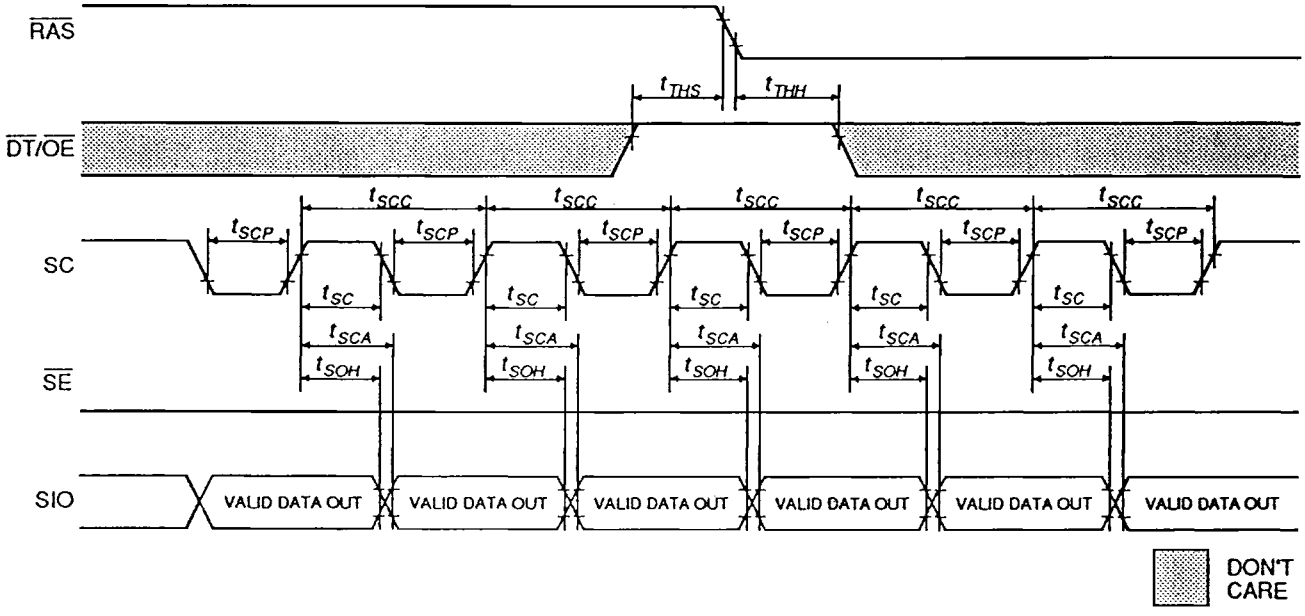
WRITE TRANSFER STATE TABLE

	STATE	
CYCLE	1	2
Write Transfer	L	L
Write Transfer	H	X

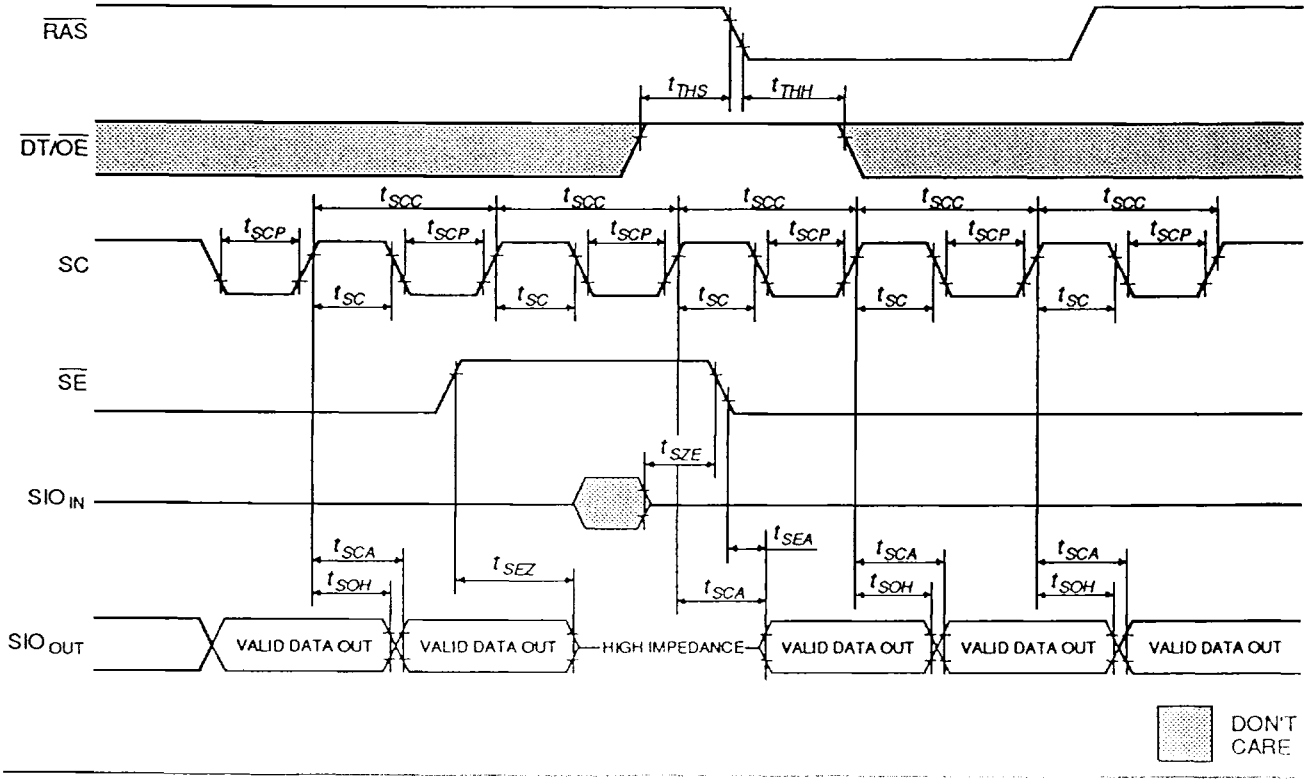
Serial Data In Timing

The serial data in cycles are used to input serial data into the SAM. Before data can be written into the SAM, the MVM4259 must be placed onto the write mode by performing a write mode control (pseudo transfer) or any transfer write cycle. A transfer read cycle is the only cycle which will take the MVM4259 out of this write mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle. While accessing data in the SAM, the state of the $\overline{DT/OE}$ is a Don't Care as long as $\overline{DT/OE}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between RAM and SAM.

Serial Read Cycle Timing ($\overline{SE}$=V_{IL})



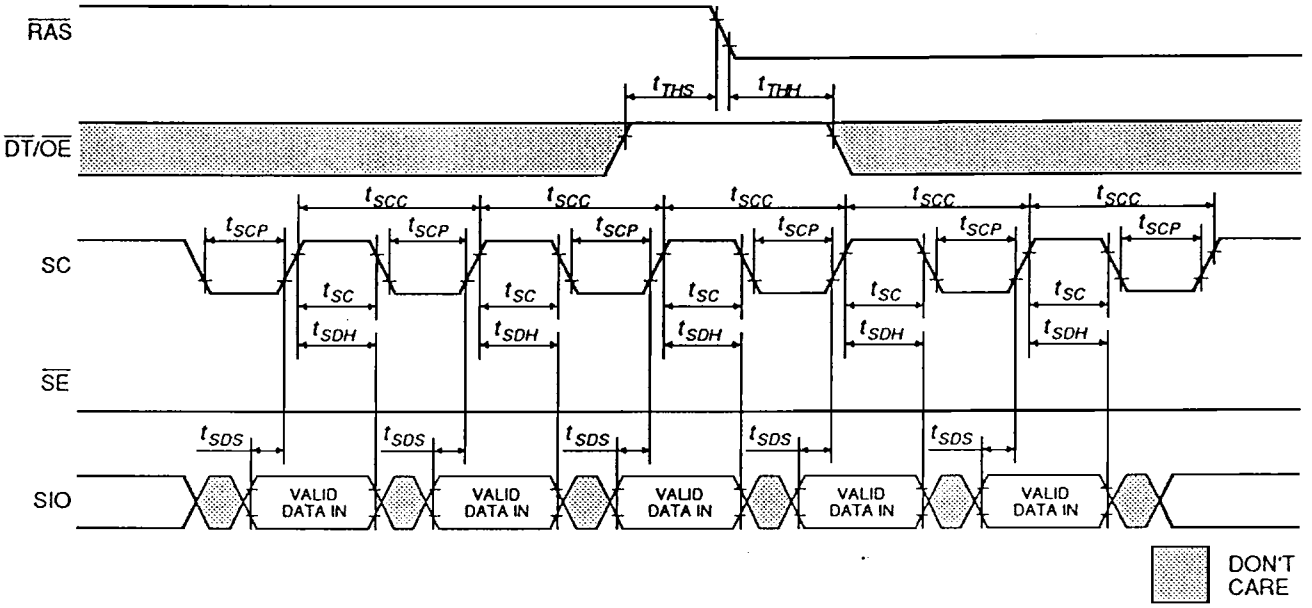
Serial Read Cycle Timing ($\overline{SE}$ Controlled Outputs))



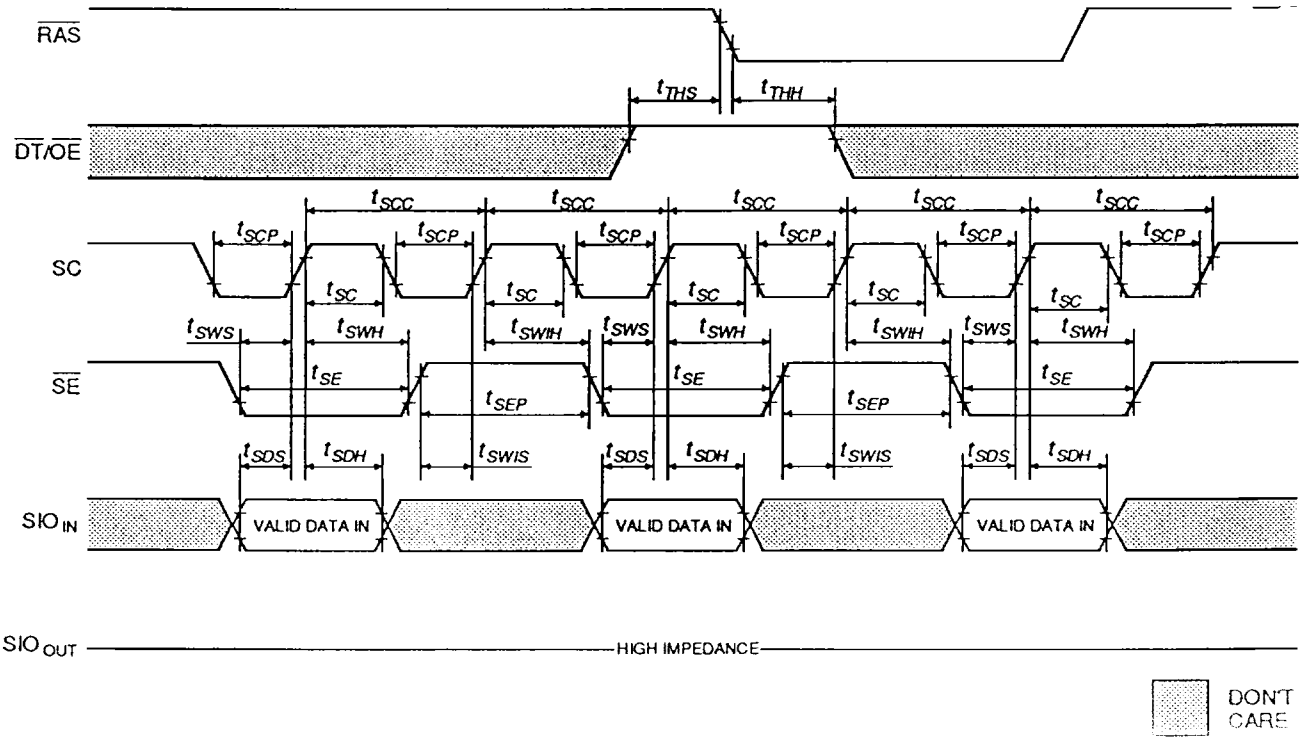
Serial Data Out Timing

The serial data out cycle is used to output serial data out of the SAM. Before data can be read via SIO, the MVM4259 must be placed into the read mode by performing a transfer read cycle.

Serial Write Cycle Timing ($\overline{SE}$=V_{IL})

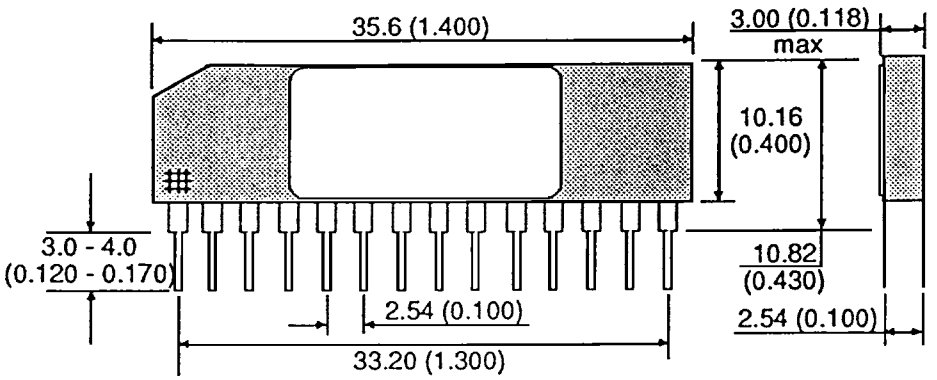


Serial Write Cycle Timing ($\overline{SE}$ Controlled Inputs)

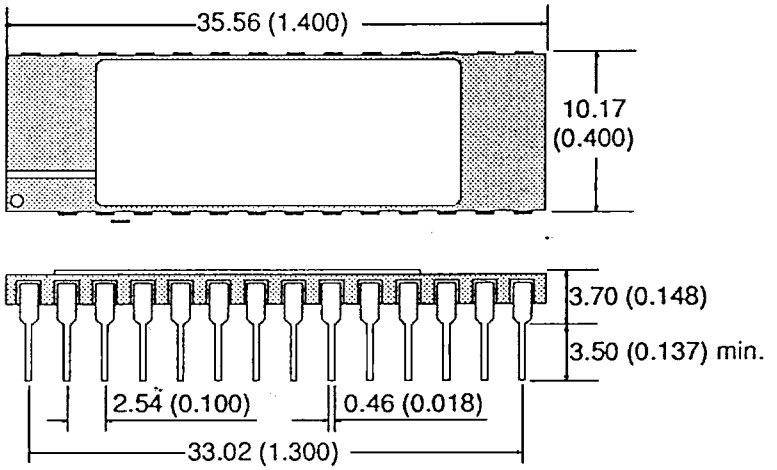


Package Details Dimensions in inches(mm). Tolerance on all dimensions ±.010(±0.254).

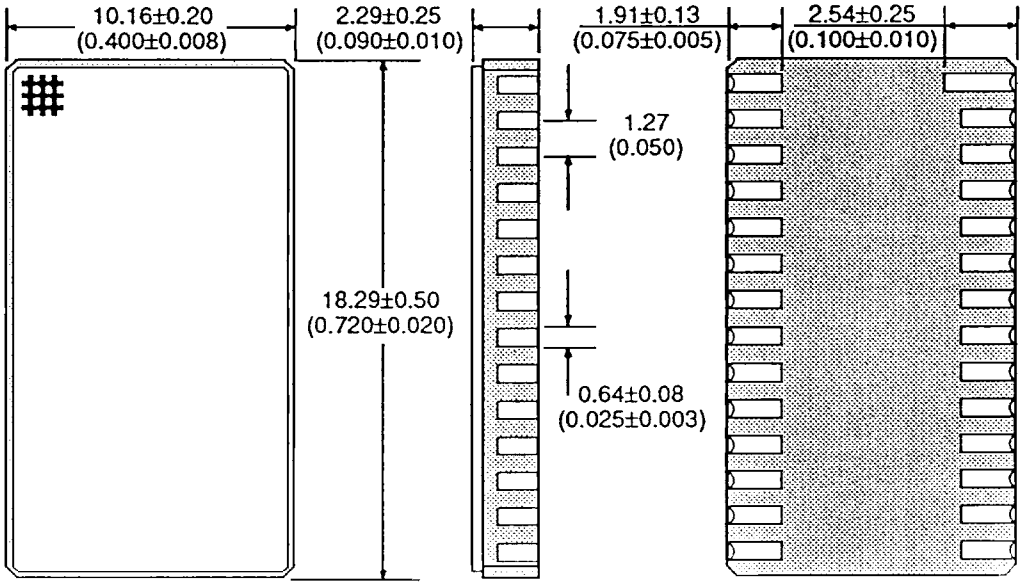
28 Pin Vertical-In-Line (VIL™) ('V' Package)



28 Pin 0.4" Dual-In-Line (DIL) ('K' Package)



28 Pin Ceramic Leadless Chip Carrier (LCC) 'WX' Package



Military Screening Procedure

Component Screening Flow for high reliability non compliant product in accordance with MIL-STD883D method 5004 is detailed below:

MB COMPONENT SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ +150°C)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MVM4259VMB-10

- **Speed**
  - 10 = 100 ns
  - 12 = 120 ns
- **Temp. range/screening**
  - Blank = Commercial Temperature
  - I = Industrial Temperature
  - M = Military Temperature
  - MB = Processed to MIL-STD883D Method 5004, non compliant
- **Package**
  - V = 28 Pin 0.1" Vertical-in-Line (VIL™)
  - K = 28 Pin 0.4" Dual-in-Line (DIL)
  - WX = 28 Pad 0.4" Leadless Chip Carrier
- **Memory Type**
  - MVM4259 = 256K x 4 Full Featured Video RAM (256K x 4 DRAM + 512 x 4 SAM)

mosaic