silicon systems™
INNOVATORS IN INTEGRATION

SSI 580
Port Expander
Floppy Disk Drive

Preliminary Data Sheet

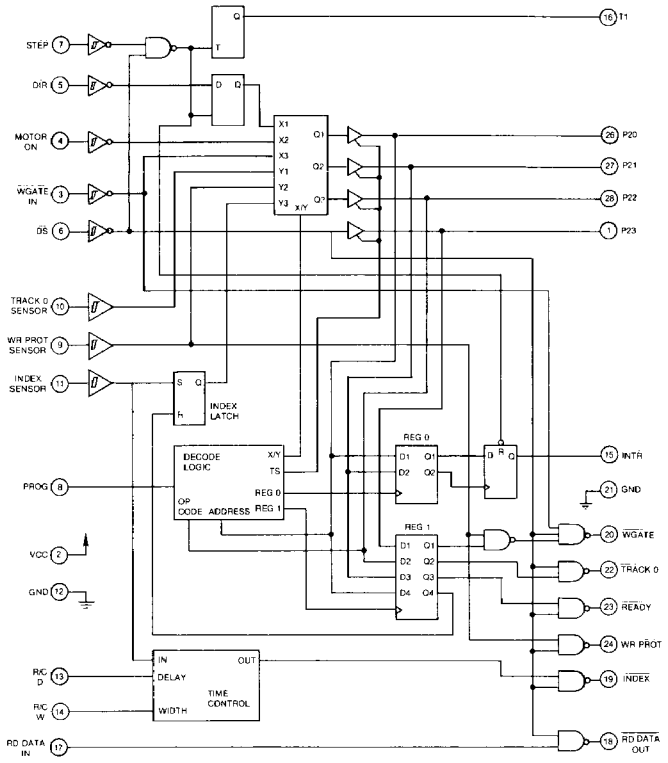
DESCRIPTION

The SSi 580 device is a bipolar integrated circuit that serves as an input/output port expander for an 8048 type microprocessor based floppy disk drive system. The device consolidates functions normally performed by a variety of LSTTL, SSI, and MSI devices. The combination of an SSI 570 (read, write, and erase device), an 8048 type microprocessor, and the SSI 580 provides the majority of electronics required for a SA400 type floppy disk drive system, including host interface bus driver and receiver. In addition to its port expansion function, the SSI 580 processes system data and provides both pulse width and delay control (adjustable by external elements) for the INDEX SENSOR input. The device requires a single +5 V power supply and is available in a 28-pin package.

FEATURES

- **Reduces package count in flexible disk drive systems**
- **Replaces bus interface and combinational logic devices between the SSI 570, on board microprocessor and mechanical interfaces.**
- **Surface mount available for further real estate reduction.**
- **Provides drive capability for mechanical and system interfaces**

SSI 580 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

PIN ASSIGNMENT DESCRIPTIONS

Pin Name	Description
P20-P23	4-bit bidirectional port, referred to as Port 2.
$\overline{\text{WGATE IN}}$	This input command to write is asserted by the host interface bus.
$\overline{\text{MOTOR ON}}$	This input command to turn on the spindle motor comes from the host interface bus.
$\overline{\text{DIR}}$	Input from the host interface bus selecting the direction in which the stepper motor should move the head.
$\overline{\text{DS}}$	Drive select
INDEX SENSOR	Input from the photodiode that indicates the index marker in the diskette.
WR PROT SENSOR	Input from the photodiode that indicates if the diskette is write protected.
TRACK 0 SENSOR	Input from the photodiode that detects when the head is positioned over track 0.
$\overline{\text{STEP}}$	Input from the host interface bus indicating that the head should be moved.
T1	This pin changes state when a $\overline{\text{STEP}}$ command is received from the host interface bus.
RD DATA IN and $\overline{\text{RD DATA OUT}}$	Read data path
$\overline{\text{WGATE}}$	Output to the disk drive's read/write circuitry.
$\overline{\text{INDEX}}$	Output to the host interface bus indicating index sensor status.
$\overline{\text{TRACK 0}}$	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{READY}}$	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{WR PROT}}$	Output to the host interface bus indicating write protect sensor status.
PROG	Input from the 8048 microprocessor for I/O control of the 580.
$\overline{\text{INTR}}$	Output to the interrupt pin of the 8048 microprocessor.
R/C D and R/C W	The external resistor and capacitor networks tied to these pins determines the delay and width of the output pulse to the $\overline{\text{INDEX}}$ pin.
Vcc	+5 V supply
GND	Ground

Table 1

CIRCUIT OPERATION

PORTS

The SSI 580 has two 4-bit input ports, Port A and Port B. Port a receives data from the host interface bus for conveyance to the drive's read/write circuitry and to the microprocessor. Three sensors report the status of the drive to the 580 via Port B. Common to both ports is a drive select ($\overline{\text{DS}}$) signal from the host interface bus. This allows the host to address separate disk drives. There is also a 4-bit bidirectional port on the SSI 580. This is port 2 and it can be used by the microprocessor to write to or read from the 580.

READ MODE

Ports A and B can be read by a microprocessor via Port 2. This allows the microprocessor to obtain data from the host interface bus and the status sensors. The PROG signal from the microprocessor provides the timing for the operation. First an OP code and a port address must be placed on Port 2 (see Table 2), then latched in on the falling edge of PROG. When the OP code and addresses have been decoded, the desired input port is selected and output on Port 2. The operation is terminated by the rising edge PROG, which returns Port 2 to the input mode.

WRITE MODE

In the write mode the microprocessor passes system parameters to the SSI 580 for logic processing and outputting. Table 3 shows how each bit of Port 2 affects the 580. A logic one on the zero bit of Port 2 will reset the index latch. P21, qualified by the $\overline{\text{DS}}$ signal, sends a "this drive ready" signal from the microprocessor to the host interface bus. Similarly P22 is $\overline{\text{DS}}$ qualified and sent to the host as a signal that the head is positioned over track 0. P23 is used in the logic that sends a R/$\overline{\text{W}}$ signal to the drive's read/write circuitry. The write mode occurs when the proper OP code and address is placed on Port 2 and latched in on the falling edge of PROG (see Table 3). The microprocessor writes in the data on PROG's rising edge.

INDEX PULSE

An optical sensor connected to the INDEX SENSOR pin detects the diskette's index marker. The state of the index sensor is latched into the 580 and is available to be read by the microprocessor on P22. The latch may be reset by writing a one to P20 from the microprocessor. The pulse received from the sensor also drives the host interface signal $\overline{\text{INDEX}}$, the width and delay of which can be controlled by external R/C circuits. The time constant attached to the R/C D pin determines the delay from the INDEX SENSOR input to the $\overline{\text{INDEX}}$ signal on the host interface bus. The equation for the delay is Td = 0.59Rd x Cd (seconds). The width of the $\overline{\text{INDEX}}$ signal is determined by the circuit attached to the R/C W pin and the equation Tw = 0.59Rw x Cw (seconds).

INTERRUPT

The $\overline{\text{INTR}}$ signal is asserted every time a step command is issued to the drive on the host interface bus. Thus when $\overline{\text{INTR}}$ is tied to the interrupt pin of 8048 type

microprocessor, an interrupt service routine will be executed on each step command. This routine typically obtains information on the direction the heads should move and the status of the track 0 sensor to use for generating the stepper motor control signals. The interrupt signal is cleared (set high) by first placing the proper OP code and address on Port 2 (see Table 3). This is latched in on the falling edge of PROG, then on its rising edge logic ones on P20 and P21 will be latched in to set $\overline{INTR}$ back to a high state. Note that an indeterminate operation will result from holding the INDEX SENSOR latch reset (holding P20 high).

T1 PIN

This signal changes state with the $\overline{STEP}$ command of the host interface bus when the drive is selected. It drives the T1 pin on an 8048 type microprocessor which is an input to a counter. The 8048 can use this count and the DIR signal read from Port 2 of the SSI 580 to monitor the head position and issue a CB (current boost) command to the SSI 570 when a specific track is reached.

TABLE 2. READ MODE

Input to Port 2		Read From Port 2				4-Bit Input Port
OP Code P22	Addr. P20	P23	P22	P21	P20	
0	0	$\overline{DS}$	Index Sensor Latch	WR Sensor	Track 0 Sensor	B
0	1	$\overline{DS}$	$\overline{WGATE}$ IN	$\overline{MOTOR}$ ON	$\overline{DIR}$	A

TABLE 3. WRITE MODE

Input to Port 2		Data processed from Port 2				
OP Code P22	Addr. P20	$\overline{WGATE}$	$\overline{TRACK0}$	$\overline{READY}$	$\overline{INTR}$	Index Latch Reset
1	0	Z	(P22*DS)	(P21*DS)	—	P20
1	1	—	—	—	See Text	—

Where Z = (P23 * WR PROT SENSOR) + ($\overline{DS}$ * $\overline{WGATE\ IN}$)

Absolute Maximum Ratings (All voltages referred to GND)

Parameter	Symbol	Value	Units
DC Supply	Vcc	+7	VDC
Voltage Range (any pin to GND)	V_m	−0.4 to +7	VDC
Power Dissipation	P_{max}	700	mW
Storage Temperature	Tstg	−40 to +125	°C
Lead Temperature (10 sec soldering)	—	260	°C

ELECTRICAL CHARACTERISTICS Unless otherwise specified, 4.75 ≤ Vcc ≤ 5.25 VDC; 0 °C < Ta < 70 °C.

Parameter	Test Conditions	Min.	Max.	Units
Totem pole outputs (P20 – P23, $\overline{INTR}$, T1)				
Output High Voltage	104 = −400 A	2.5	—	V
Output Low Voltage	IoL = 2mA	—	0.5	V
Open collector outputs ($\overline{RD\ DATA\ OUT}$, $\overline{INDEX}$, $\overline{WGATE}$, $\overline{TRACK\ 0}$, $\overline{READY}$, $\overline{WR\ PROT}$)				
Output High Current	VOH = 5.25 V.	—	250	μA
Output Low Voltage	IoL = 48 mA	—	0.5 V	V
Inputs (P20 – P23, PROG, RD DATA IN)				
Input High Voltage	—	2.0	—	V
Input Low Voltage	—	—	0.8	V
Input Low Current	VIL = 0.5 V	—	−0.8	mA
Input High Current	VIL = 2.4 V	—	40	μA
Input Current	Vin = 7.0 V	—	0.1	mA
Schmitt - Trigger Inputs ($\overline{WGATE\ IN}$, $\overline{MOTOR\ ON}$, $\overline{DIR}$, $\overline{DS}$, $\overline{STEP}$)				
Threshold Voltage	Positive Going, Vcc = 5.0 V	1.3	2.0	V
	Negative Going, Vcc = 5.0 V	0.6	1.1	V

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Test Conditions	Min.	Max.	Units
Hysteresis	Vcc = 5.0 V	0.4	—	V
Input High Current	VIH = 2.4 V	—	40	μA
Input Low Current	VIL = 0.5 V	—	−0.4	mA
Input Current	VIN = 7.0 V	—	0.1	mA
High Impedance Inputs with Hysteresis (WR PROT SENSOR, TRACK 0 SENSOR, INDEX SENSOR)				
Input High Voltage	—	—	2.0	V
Input Low Voltage	—	0.8	—	V
Hysteresis	—	0.2	—	V
Input Current	Vin = 0 to Vcc	—	−0.25	mA

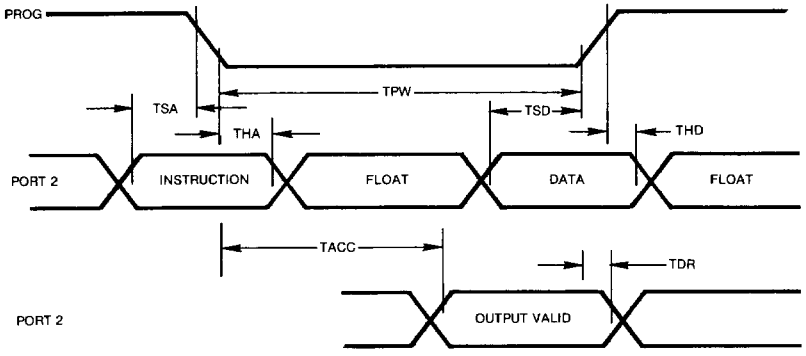
TIMING CHARACTERISTICS Unless otherwise specified; Ta = 25°C; 4.75 V ≤Vcc≤5.25 V; CL = 15 pf.

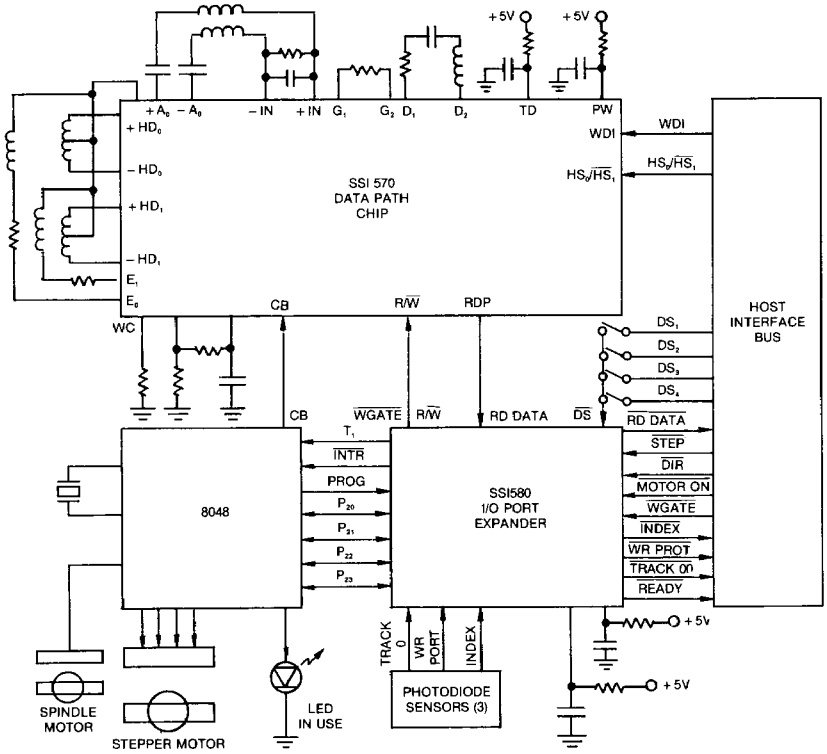
PARAMETER	CONDITION	MIN.	MAX.	UNITS
Propagation Delay Time	RD DATA IN to $\overline{\text{RD DATA OUT}}$	—	35	nS
	$\overline{\text{DS}}$ to $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$, $\overline{\text{READY}}$, $\overline{\text{WR PROT}}$, $\overline{\text{RD DATA}}$, $\overline{\text{INDEX}}$	—	80	nS
	PROG to $\overline{\text{INTR}}$, $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$ (Rising edge) $\overline{\text{READY}}$, $\overline{\text{WR PROT}}$	—	100	nS
	WR PROT to $\overline{\text{WGATE}}$, $\overline{\text{WR PROT SENSOR}}$	—	250	nS
	$\overline{\text{WGATE}}$ IN to $\overline{\text{WGATE}}$	—	80	nS
	$\overline{\text{STEP}}$ to T1, P20	—	80	nS
	TRACK 0 SENSOR WR PROT SENSOR to Port 2 INDEX SENSOR	—	250	nS
	$\overline{\text{MOTOR ON}}$ $\overline{\text{WGATE IN}}$ to Port 2 $\overline{\text{DS}}$	—	80	nS
Data Setup Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	50	—	nS
Data Hold Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	0	—	nS
Delay Accuracy (Pin 13)	$T_D = 0.59\ R_D \times C_D$ R_D = 3.9k to 10k C_D = 75pf to 300pf	0.8Td	1.2Td	sec
Pulse Width Accuracy (Pin 14)	$T_W = 0.59\ R_W \times C_W$ R_W = 3.9k to 10k C_W = 75pf to 300pf	0.8Tw	1.2Tw	sec

PORT 2 (P20 – P23) TIMING (Timing Referenced to PROG signal, Figure 2.)

Symbol	Name-Description	Min	Max	Units
TSA	Addr. setup time	100	—	nS
THA	Addr. hold time	80	—	nS
TSD	Data in setup time	100	—	nS
THD	Data-in hold time	80	—	nS
TACC	Data-out access time	—	700	nS
TDR	Data-out release time	—	200	nS
TPW	PROG pulse width	1500	—	nS

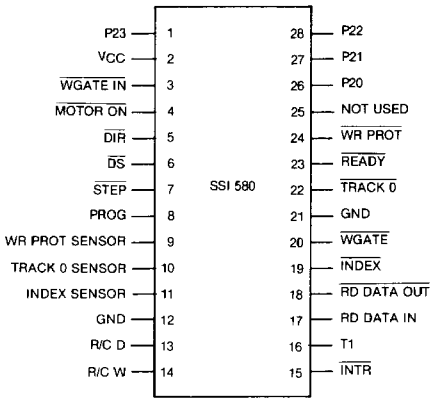
Figure 2. Timing Diagram



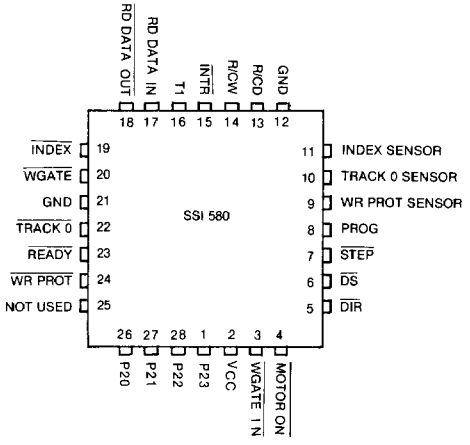


silicon systems
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

PIN CONFIGURATION



28-LEAD PDIP
(Top View)



28-Lead Quad
(Top View)