NEW EDO DRAM

DRAM

16 MEG x 4 DRAM

3.3V, EDO PAGE MODE

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x4 pinout, timing, functions and packages
- 13 row-addresses, 11 column-addresses (G3) or 12 row-addresses, 12 column-addresses (H9)
- High-performance CMOS silicon-gate process
- All inputs and outputs are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- 4,096-cycle $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH distributed across 64ms

OPTIONS — MARKING

- Timing
  - 50ns access — -5
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Plastic SOJ (500 mil) — DW
  - Plastic TSOP (500 mil) — TW
- Part Number Example: MT4LC16M4G3DW-7

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-5	90ns	50ns	20ns	25ns	13ns	8ns
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

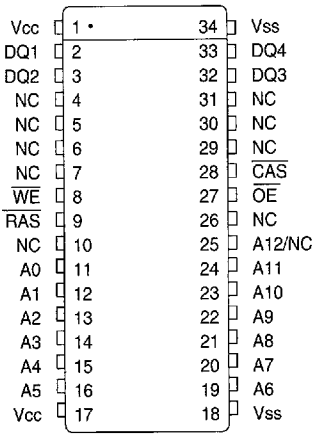
GENERAL DESCRIPTION

The MT4LC16M4G3 and MT4LC16M4H9 are high-speed CMOS dynamic random access memory devices containing 67,108,864 bits, and designed to operate from 3.0V to 3.6V. The MT4LC16M4G3 and MT4LC16M4H9 are functionally organized as 16,777,216 locations containing 4 bits each. The 16,777,216 memory locations are arranged in 8,192 rows by 2,048 columns for the MT4LC16M4G3 or 4,096 rows by 4,096 columns for the MT4LC16M4H9. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the $\overline{RAS}$ signal, then the column address by $\overline{CAS}$. Both devices provide EDO PAGE MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

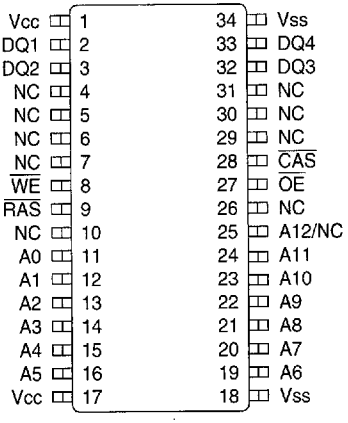
The MT4LC16M4G3 and MT4LC16M4H9 must be refreshed periodically in order to retain stored data.

PIN ASSIGNMENT (Top View)

34-Pin SOJ (DA-6)

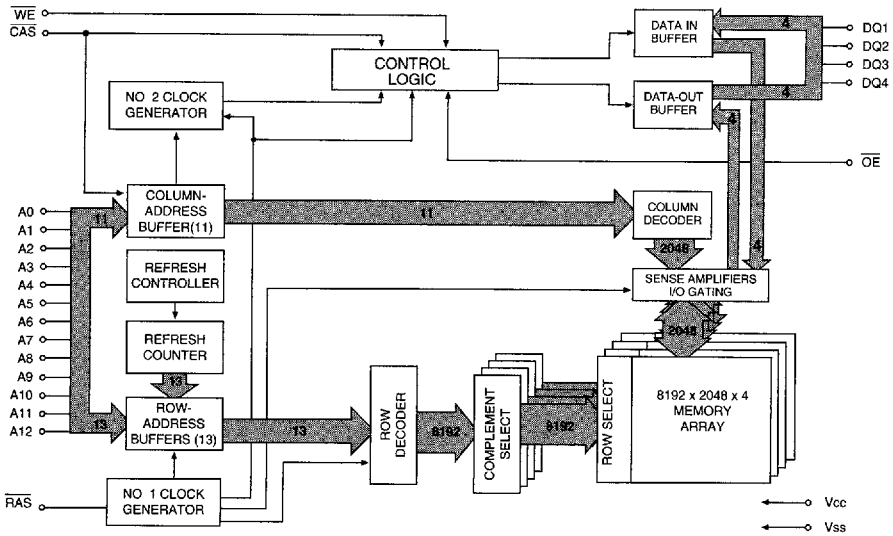


34-Pin TSOP*

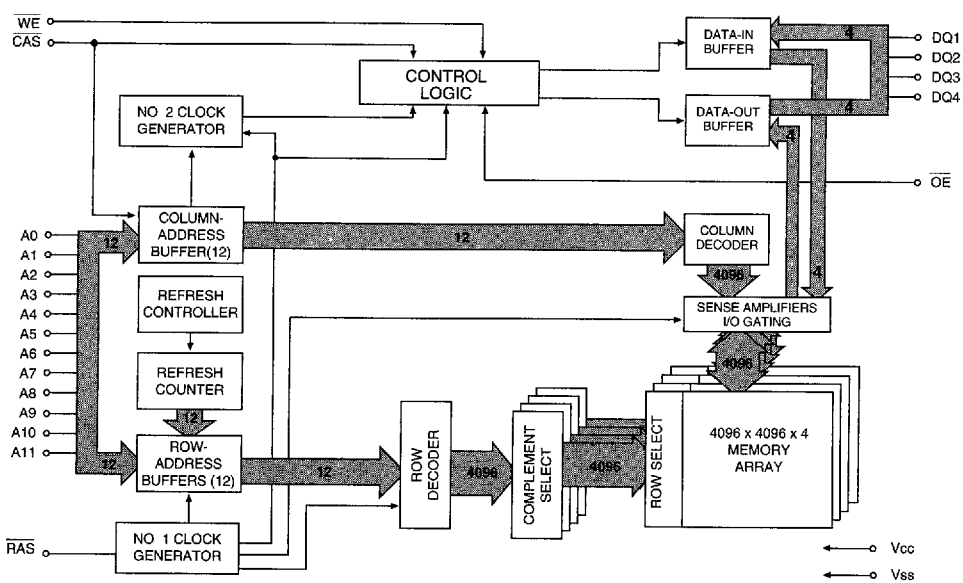


*Consult factory for dimensions and availability.

FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4G3 (13 row-addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4H9 (12 row-addresses)



FUNCTIONAL DESCRIPTION

The functional description for the MT4LC16M4G3 and MT4LC16M4H9 is divided into the two areas described below (DRAM access and DRAM refresh). Relevant timing diagrams are included in this data sheet, following the timing specifications tables.

DRAM ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the four I/O pins (DQ1-4). The $\overline{WE}$ signal must be activated to execute a write operation, otherwise a read operation will be performed. The $\overline{OE}$ signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ went HIGH, and $\overline{OE}$ was LOW (active), the output buffers would be disabled. The MT4LC16M4G3 and MT4LC16M4H9 offer an accelerated PAGE MODE cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called EDO and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ and $\overline{OE}$ are held LOW and $\overline{WE}$ is held HIGH. $\overline{OE}$ can be brought LOW or HIGH while $\overline{CAS}$ and $\overline{RAS}$ are LOW, and the DQs will transition between valid data and High-Z. Using $\overline{OE}$, there are two methods to disable the outputs and keep them disabled during the $\overline{CAS}$ HIGH time. The first method is to have $\overline{OE}$ HIGH when $\overline{CAS}$ transitions HIGH and keep $\overline{OE}$ HIGH for ^tOEHC thereafter. This will disable the DQs and they will remain disabled (regardless of the state of $\overline{OE}$ after that point) until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ LOW when $\overline{CAS}$ transitions HIGH. Then bringing $\overline{OE}$ HIGH for a minimum of ^tOEP anytime during the $\overline{CAS}$ HIGH period will disable the DQs; the DQs will remain disabled (regardless of the state of $\overline{OE}$ after that point) until $\overline{CAS}$ falls again (please refer to Figure 1). During other cycles, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH, or ^tWHZ after $\overline{WE}$ transitions LOW. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

EDO PAGE MODE operations are always initiated with a row-address strobed-in by the $\overline{RAS}$ signal, followed by a column-address strobed-in by $\overline{CAS}$, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling $\overline{CAS}$ while holding $\overline{RAS}$ LOW, and entering new column addresses with each $\overline{CAS}$ cycle. Returning $\overline{RAS}$ HIGH terminates the EDO PAGE MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (G3) or all 4,096 rows (H9) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC16M4G3 internally refreshes two rows for every CBR cycle, whereas the MT4LC16M4H9 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. Alternatively, $\overline{RAS}$-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time, so for the MT4LC16M4G3, 8,192 $\overline{RAS}$-ONLY REFRESH cycles must be executed every 64ms to cover all rows.

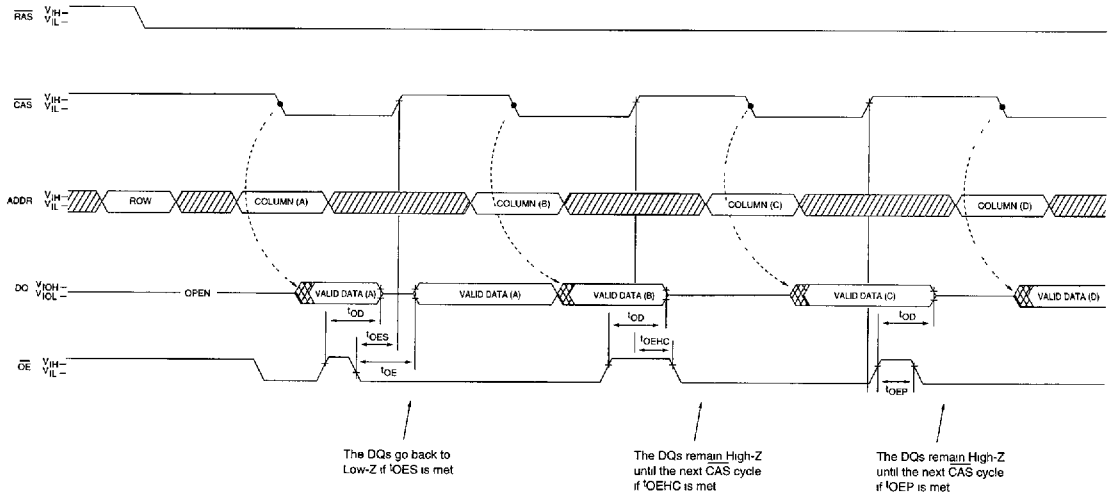


Figure 1
$\overline{OE}$ CONTROL OF DQs

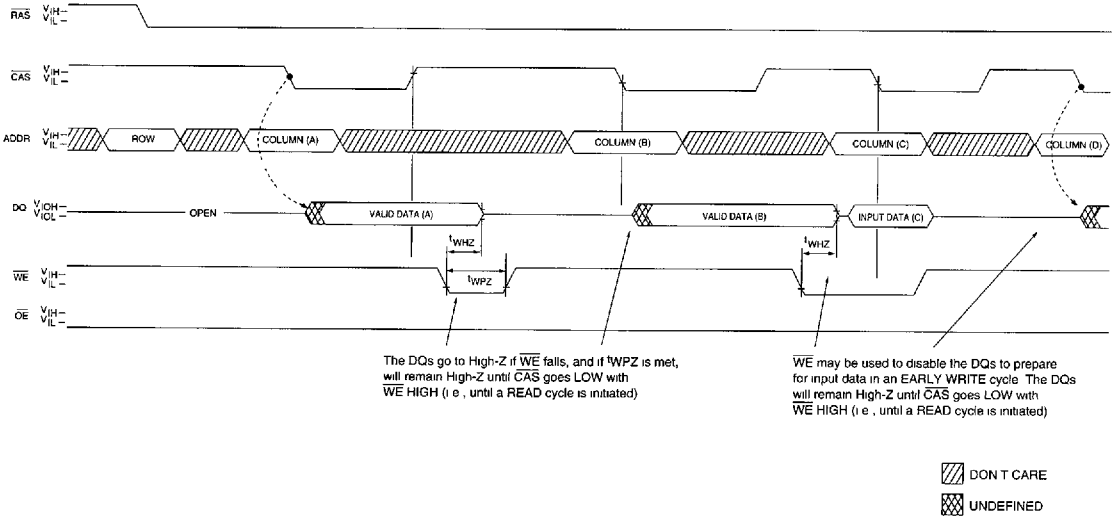


Figure 2
$\overline{WE}$ CONTROL OF DQs

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS} ..... -1.0V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} ..... -1.0V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -5	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MT4LC16M4G3	I_{CC1}	1	1	1	mA	
	MT4LC16M4H9	I_{CC1}	1	1	1		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} -0.2V, DQs may be left open, Other inputs: V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V)	MT4LC16M4G3	I_{CC2}	500	500	500	µA	
	MT4LC16M4H9	I_{CC2}	500	500	500		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	MT4LC16M4G3	I_{CC3}	130	120	110	mA	3, 4, 29
	MT4LC16M4H9	I_{CC3}	170	160	150		
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	MT4LC16M4G3	I_{CC4}	150	120	100	mA	3, 4, 29
	MT4LC16M4H9	I_{CC4}	150	120	100		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	MT4LC16M4G3	I_{CC5}	130	120	110	mA	3, 26
	MT4LC16M4H9	I_{CC5}	170	160	150		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	MT4LC16M4G3	I_{CC6}	140	130	120	mA	3, 5
	MT4LC16M4H9	I_{CC6}	170	160	150		

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		25		30		35	ns	
Column-address set-up to $\overline{CAS}$ going HIGH during WRITE	^tACH	15		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	40		45		55		ns	
Column-address setup time	^tASC	0		0		0		ns	
Row-address setup time	^tASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	48		55		65		ns	21
Access time from $\overline{CAS}$	^tCAC		13		15		20	ns	15
Column-address hold time	^tCAH	8		10		12		ns	
$\overline{CAS}$ pulse width	^tCAS	8	10,000	10	10,000	12	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	8		10		12		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		5		5		ns	
$\overline{CAS}$ precharge time	^tCP	8		10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		28		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
$\overline{CAS}$ hold time	^tCSH	44		50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	30		35		40		ns	21
Write command to $\overline{CAS}$ lead time	^tCWL	8		15		15		ns	
Data-in hold time	^tDH	8		10		12		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	40		45		55		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Output disable	^tOD	0	13	0	15	0	15	ns	27, 28
Output Enable time	^tOE		13		15		15	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	8		10		12		ns	28
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^tOEHC	7		10		10		ns	
$\overline{OE}$ HIGH pulse width	^tOEP	7		10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	4		5		5		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

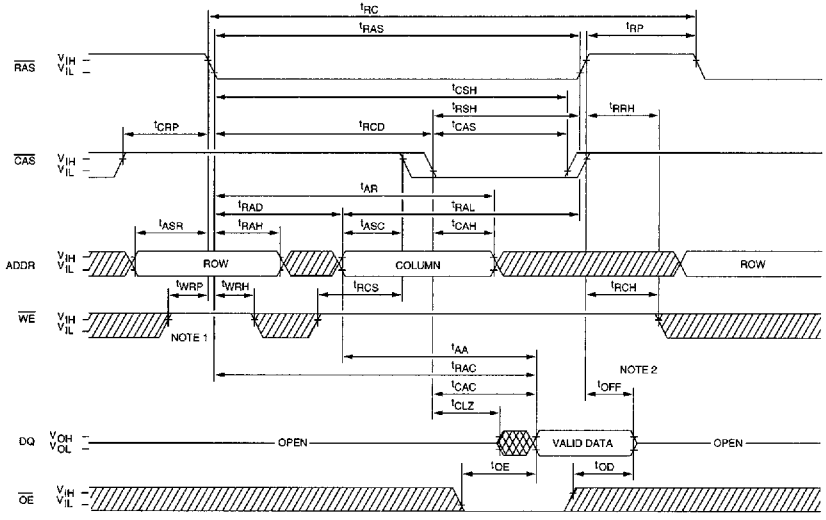
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	13	0	15	0	15	ns	20, 27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	tPC	20		25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	71		75		85		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	14
$\overline{RAS}$ to column-address delay time	tRAD	9	25	12	30	12	35	ns	18
Row-address hold time	tRAH	8		10		10		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	tRASP	50	125,000	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	tRC	90		110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	11	37	14	45	14	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command setup time	tRCS	0		0		0		ns	
Refresh period	tREF		64		64		64	ms	26
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{RAS}$ hold time	tRSH	8		10		12		ns	
READ WRITE cycle time	tRWC	126		150		177		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	73		80		90		ns	21
Write command to $\overline{RAS}$ lead time	tRWL	8		15		15		ns	
Transition time (rise or fall)	tT	1	50	2	50	2	50	ns	
Write command hold time	tWCH	8		10		12		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	40		45		55		ns	
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21
$\overline{WE}$ to outputs in High-Z	tWHZ		10		13		15	ns	
Write command pulse width	tWP	7		10		12		ns	
$\overline{WE}$ pulse width to disable outputs	tWPZ	7		10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	8		10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	8		10		10		ns	25

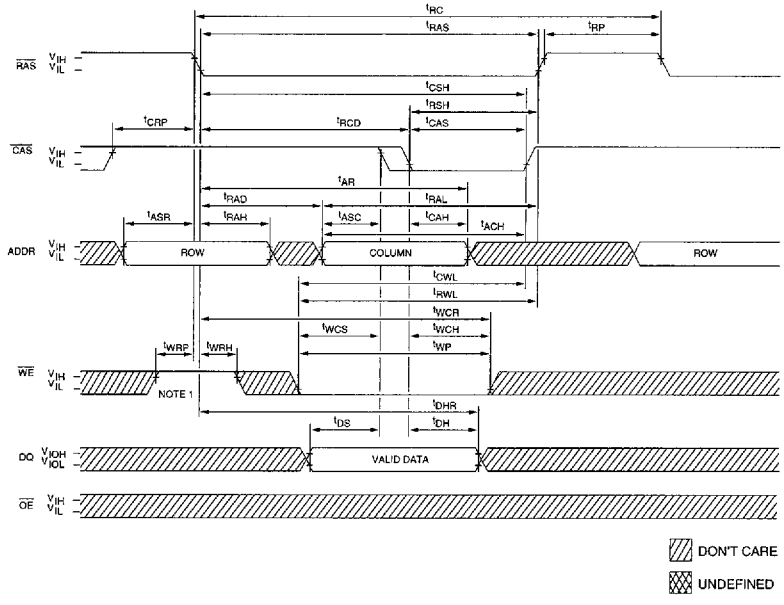
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}Tof 2ns for -5 and 2.5ns for -6 and -7.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. If ^{t}WCS > ^{t}WCS MIN, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ^{t}RWD, ^{t}AWD and ^{t}CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. $\overline{RAS}$-ONLY REFRESH requires that all 8,192 rows of the MT4LC16M4G3, or all 4,096 rows of the MT4LC16M4H9, be refreshed at least once every 64ms. CBR REFRESH, for either device, requires that at least 4,096 cycles be completed every 64ms.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
29. Column-address changed once each cycle.

READ CYCLE



EARLY WRITE CYCLE

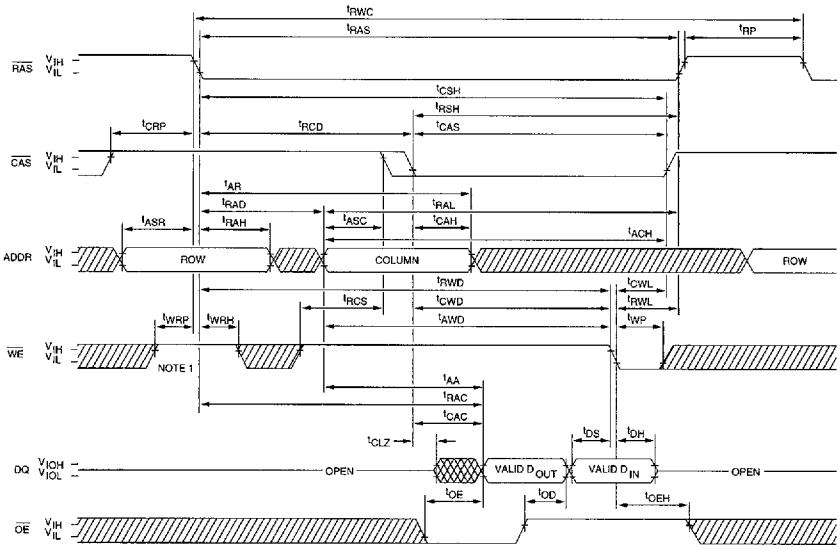


NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

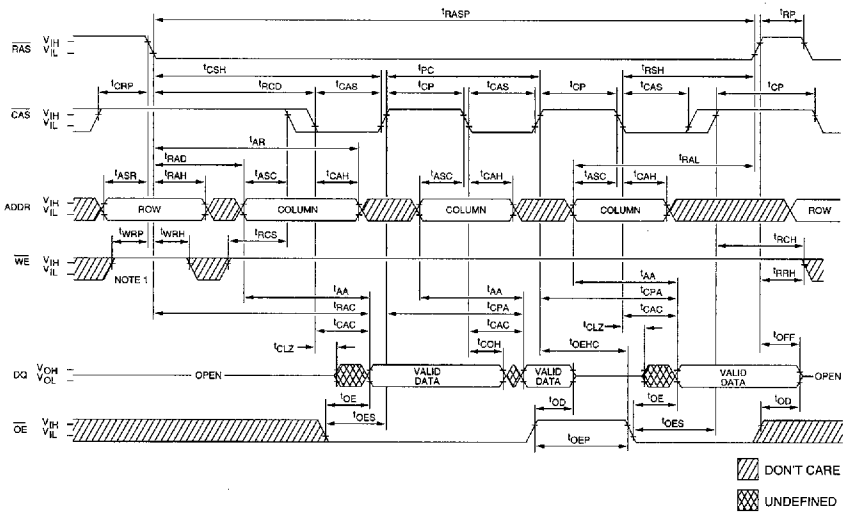
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

READ WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)

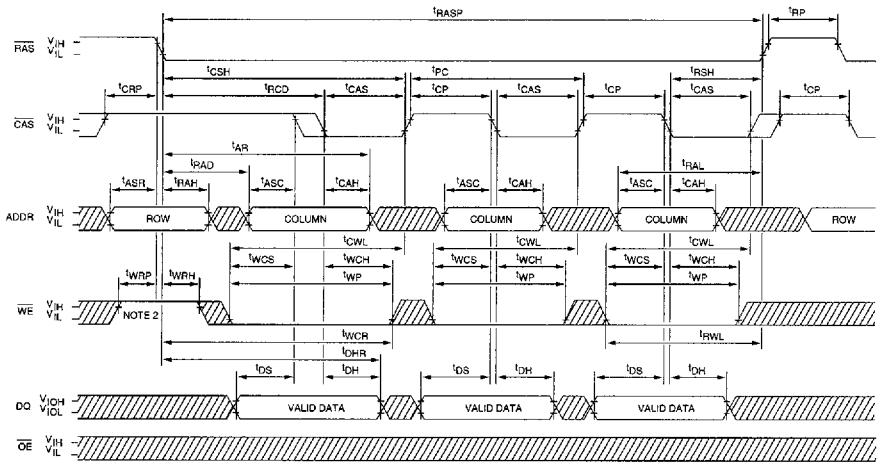


EDO-PAGE-MODE READ CYCLE



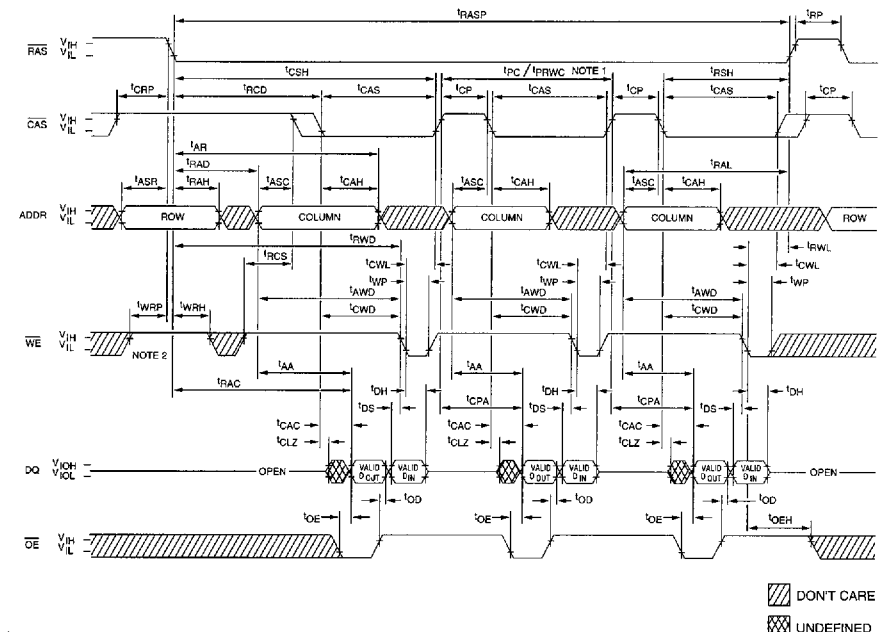
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE

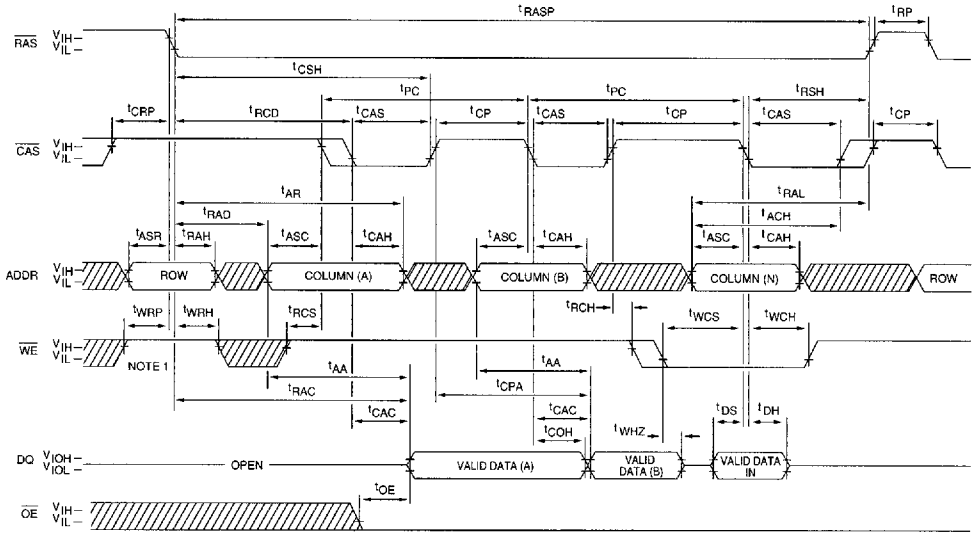
(LATE WRITE and READ-MODIFY-WRITE cycles)



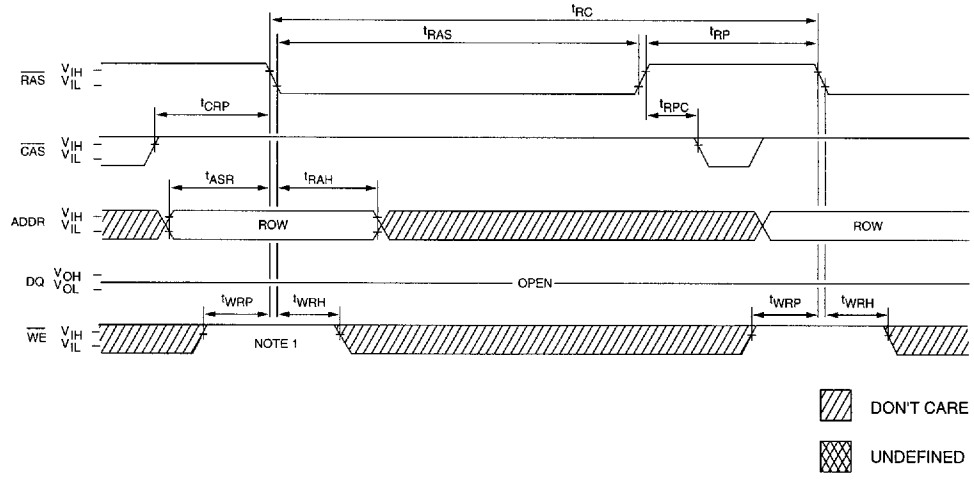
NOTE: 1. tPC is for LATE WRITE cycles only.

2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



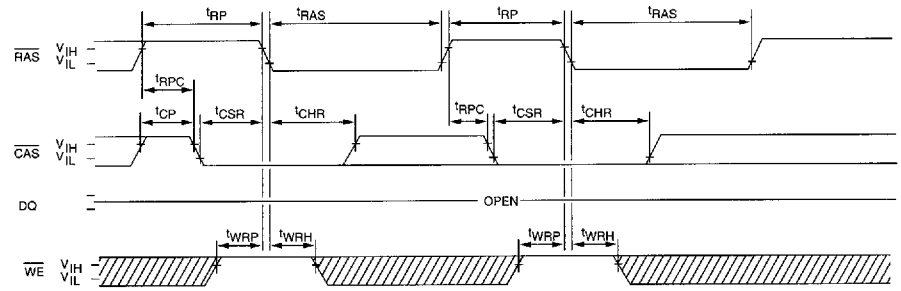
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

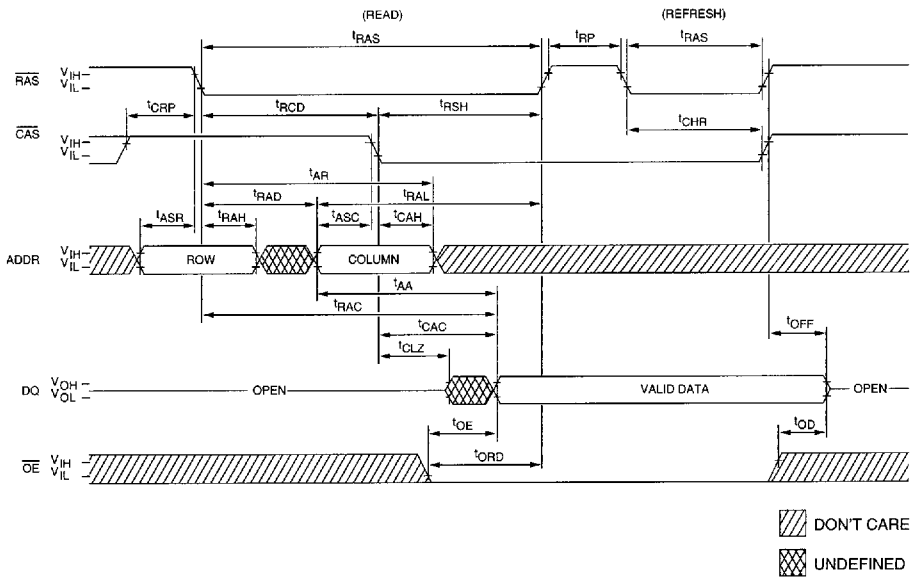
CBR REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)

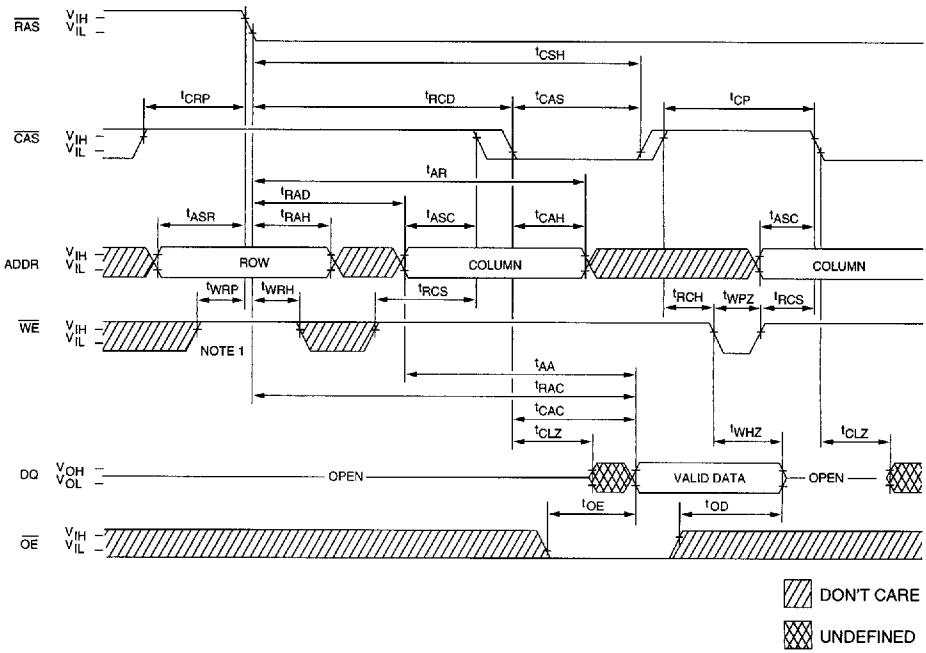


HIDDEN REFRESH CYCLE [24]

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.