

MOS INTEGRATED CIRCUIT

MC-422000A32, 422000A36 SERIES

2 M-WORD BY 32-BIT, 2 M-WORD BY 36-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-422000A32 series is a 2 097 152 words by 32 bits dynamic RAM module on which 16 pieces of 4 M DRAM (μ PD424400) are assembled.

The MC-422000A36 series is a 2 097 152 words by 36 bits dynamic RAM module on which 16 pieces of 4 M DRAM (μ PD424400) and 8 pieces of 1 M DRAM (μ PD421000) are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2 097 152 words by 32 bits organization (MC-422000A32 series)
- 2 097 152 words by 36 bits organization (MC-422000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	120 ns	5 355 mW	84 mW
MC-422000A32-70	70 ns	140 ns	4 515 mW	
MC-422000A32-80	80 ns	160 ns	4 095 mW	
MC-422000A32-10	100 ns	190 ns	3 675 mW	
MC-422000A36-70	70 ns	140 ns	6 195 mW	126 mW
MC-422000A36-80	80 ns	160 ns	5 565 mW	
MC-422000A36-10	100 ns	190 ns	4 935 mW	

- 1 024 refresh cycles/16 ms
- Three refresh modes are available: $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- All inputs and outputs are TTL compatible
- Single +5.0 V \pm 5 % power supply
- Access time can be distinguished with characteristics of PD-pins(PD0 to PD3)

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	16 pieces of μ PD424400LA (300 mil SOJ) [Double side]
MC-422000A32B-70	70 ns		
MC-422000A32B-80	80 ns		
MC-422000A32B-10	100 ns		
MC-422000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-422000A32F-70	70 ns		
MC-422000A32F-80	80 ns		
MC-422000A32F-10	100 ns		
		72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	
MC-422000A36BJ-70	70 ns		
MC-422000A36BJ-80	80 ns		
MC-422000A36BJ-10	100 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	8 pieces of μ PD421000LA (300 mil SOJ) [Double side]
MC-422000A36FJ-70	70 ns		
MC-422000A36FJ-80	80 ns		
MC-422000A36FJ-10	100 ns		

Quality Grade

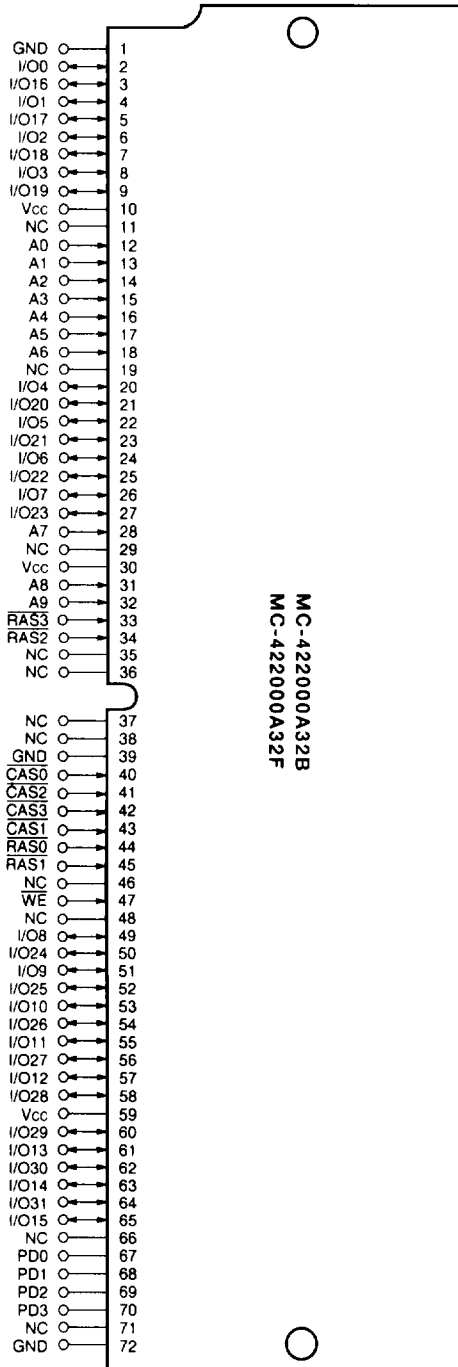
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Front view)

[MC-422000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



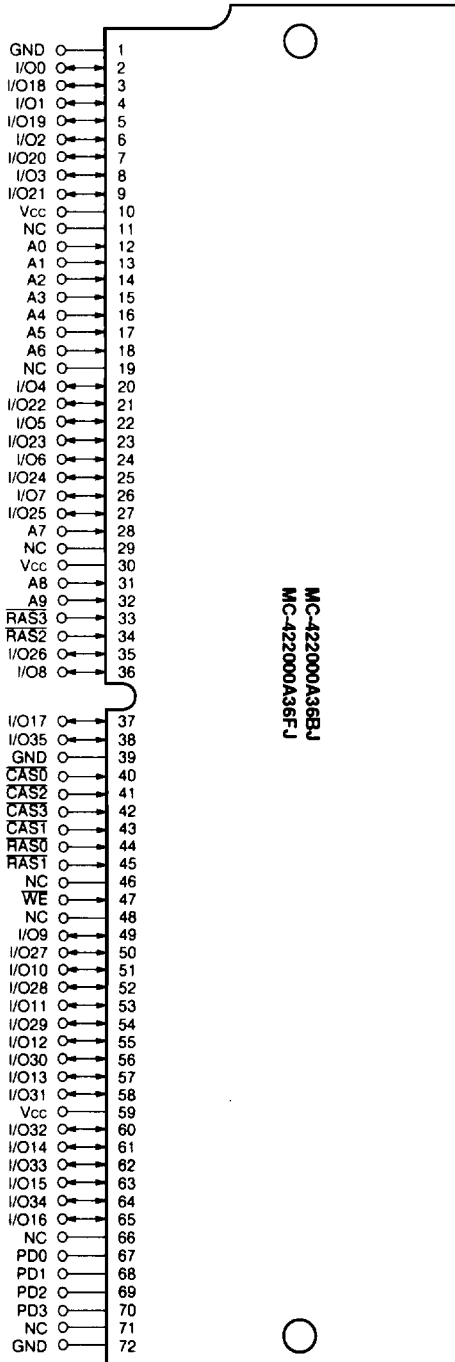
- A0-A9 : Address Inputs
- I/O0-I/O31 : Data Inputs/Outputs
- CAS0-CAS3 : Column Address Strobe
- RAS0-RAS3 : Row Address Strobe
- WE : Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

[MC-422000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



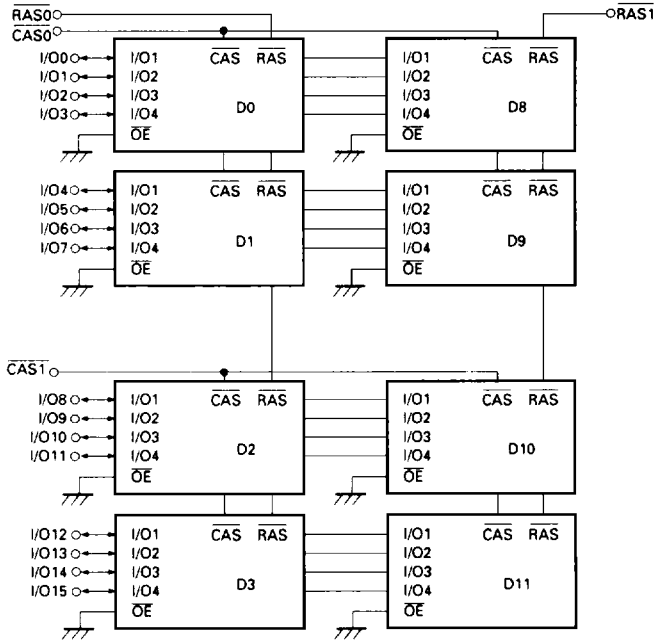
- A0-A9 : Address Inputs
- I/O0-I/O35 : Data Inputs/Outputs
- CAS0-CAS3 : Column Address Strobe
- RAS0-RAS3 : Row Address Strobe
- WE : Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

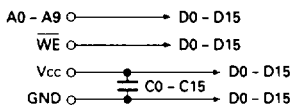
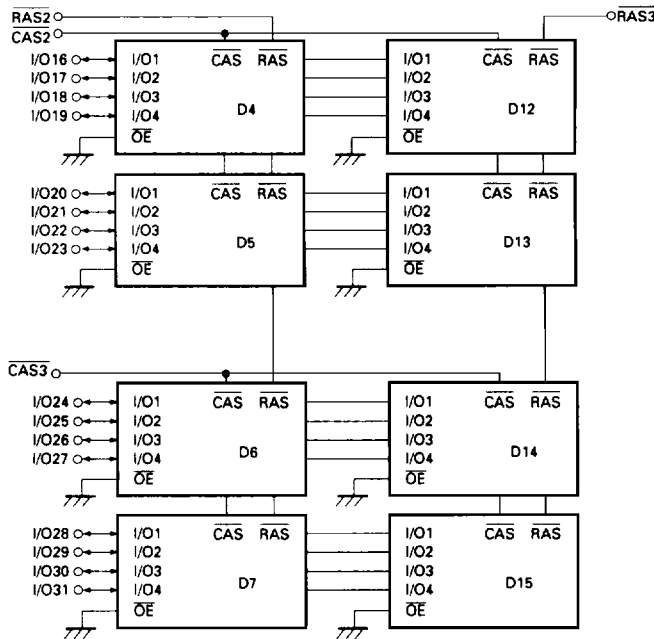
Pin Name	Pin No.	Access Time			
		70 ns	80 ns	100 ns	
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagrams

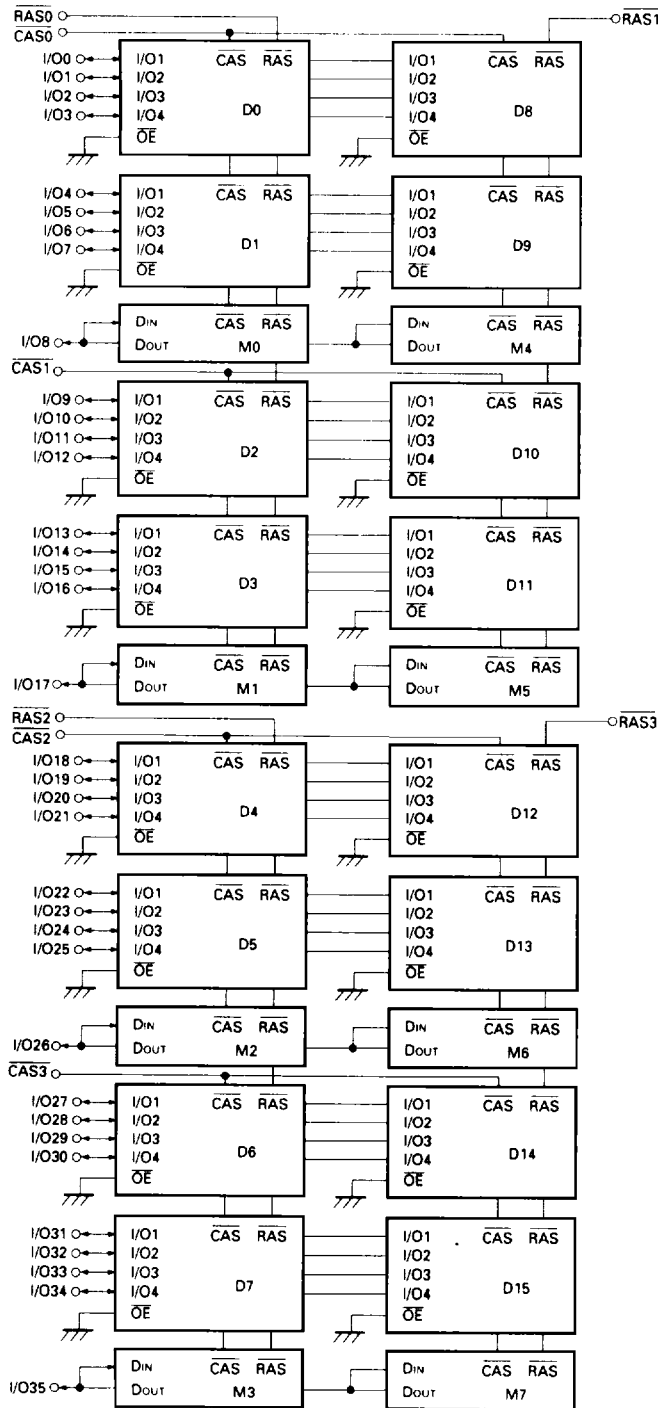
[MC-422000A32 series]



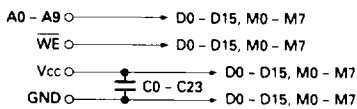
Remark D0-D15 : μ PD424400



[MC-422000A36 series]



Remark D0-D15 : μ PD424400
M0-M7 : μ PD421000



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-422000A32	16	W
		MC-422000A36	24	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ °C}$, $f = 1\text{ MHz}$)

[MC-422000A32 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			121	pF
	C_{I2}	\overline{WE}			137	
	C_{I3}	$\overline{RAS0} - \overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

[MC-422000A36 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			161	pF
	C_{I2}	\overline{WE}			193	
	C_{I3}	$\overline{RAS0} - \overline{RAS3}$			62	
	C_{I4}	$\overline{CAS0} - \overline{CAS3}$			62	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			39	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)
[MC-422000A32 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 020	mA	3,4,7
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	780		
			$t_{\text{RAC}} = 100 \text{ ns}$	700		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$ $I_o = 0 \text{ mA}$		32	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ $I_o = 0 \text{ mA}$		16		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$ $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 020	mA	3,4,5,7
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	780		
			$t_{\text{RAC}} = 100 \text{ ns}$	700		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}, \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	780	mA	3,4,6
			$t_{\text{RAC}} = 70 \text{ ns}$	700		
			$t_{\text{RAC}} = 80 \text{ ns}$	620		
			$t_{\text{RAC}} = 100 \text{ ns}$	540		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	1 020	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	860		
			$t_{\text{RAC}} = 80 \text{ ns}$	780		
			$t_{\text{RAC}} = 100 \text{ ns}$	700		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	I/O0 to I/O31 is disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

[MC-422000A36 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	1 180	mA	3,4,7
			$t_{\text{RAC}} = 80 \text{ ns}$	1 060		
			$t_{\text{RAC}} = 100 \text{ ns}$	940		
Standby current	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$	$I_o = 0 \text{ mA}$	48	mA	
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$I_o = 0 \text{ mA}$	24		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}} \geq V_{\text{IH(MIN.)}}$ $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	1 180	mA	3,4,5,7
			$t_{\text{RAC}} = 80 \text{ ns}$	1 060		
			$t_{\text{RAC}} = 100 \text{ ns}$	940		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}, \overline{\text{CAS}}$ Cycling $t_{\text{PC}} = t_{\text{PC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	980	mA	3,4,6
			$t_{\text{RAC}} = 80 \text{ ns}$	860		
			$t_{\text{RAC}} = 100 \text{ ns}$	740		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	1 180	mA	3,4
			$t_{\text{RAC}} = 80 \text{ ns}$	1 060		
			$t_{\text{RAC}} = 100 \text{ ns}$	940		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	$I/O0 \text{ to } I/O35 \text{ is disabled (Hi-Z)}$ $V_o = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

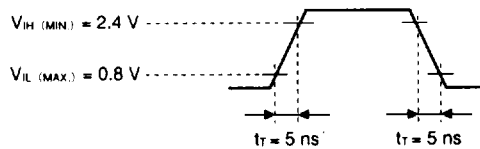
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9, 18

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	
Access Time from RAS	t _{RAC}		60		70		80		100	ns	10,11
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	MC-422000A32 t _{CAC}		15		20		20		25	ns	10,11
	MC-422000A36										
Access Time from Column Address	t _{AA}		30		35		40		50	ns	10,11
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45		55	ns	11
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	10
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	50		60		70		80		ns	
RAS Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
RAS Hold Time	t _{RSH}	20		20		20		25		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60		70		80		100		ns	
RAS to $\overline{\text{CAS}}$ Delay Time	MC-422000A32 t _{RCD}	20	40	20	50	25	60	25	90	ns	10
	MC-422000A36								75		
CAS to RAS Precharge Time	t _{CRP}	10		10		10		10		ns	13
CAS Precharge Time	t _{CPN}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
RAS Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		10		ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	MC-422000A32 t _{CAH}	15		15		15		20		ns	
	MC-422000A36			17		20					
Column Address Lead Time Referenced to RAS	t _{RAL}	30		35		40		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	10		10		10		10		ns	14
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		20		ns	15
Data-in Setup Time	t _{DS}	0		0		0		0		ns	16
Data-in Hold Time	MC-422000A32 t _{DH}	15		15		15		20		ns	16
	MC-422000A36					20					
Write Command Setup Time	t _{WCS}	0		0		0		0		ns	17
CAS Setup Time for $\overline{\text{CAS}}$ before RAS Refresh	t _{CSR}	10		10		10		10		ns	
CAS Hold Time for $\overline{\text{CAS}}$ before RAS Refresh	t _{CHR}	15		15		15		20		ns	
WE Setup Time	t _{WSR}	10		10		10		10		ns	
WE Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

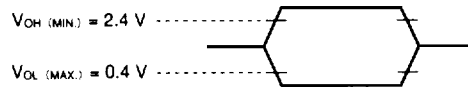
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. t_{CC1} , t_{CC3} , t_{CC4} and t_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. t_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. t_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. t_{CC1} and t_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{IL(\text{MAX.})}$ and $\overline{\text{CAS}} \geq V_{IH(\text{MIN.})}$.
8. AC measurements assume $t_T = 5$ ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD(\text{MAX.})}$, $t_{RCD} \leq t_{RCD(\text{MAX.})}$	$t_{RAC(\text{MAX.})}$	$t_{RAC(\text{MAX.})}$
$t_{RAD} > t_{RAD(\text{MAX.})}$, $t_{RCD} \leq t_{RCD(\text{MAX.})}$	$t_{AA(\text{MAX.})}$	$t_{RAD} + t_{AA(\text{MAX.})}$
$t_{RCD} > t_{RCD(\text{MAX.})}$	$t_{CAC(\text{MAX.})}$	$t_{RCD} + t_{CAC(\text{MAX.})}$

$t_{RAD(\text{MAX.})}$ and $t_{RCD(\text{MAX.})}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(\text{MAX.})}$ and $t_{RCD} \geq t_{RCD(\text{MAX.})}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF(\text{MAX.})}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL} .
13. $t_{CRP(\text{MIN.})}$ requirement should be applied for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycles.
14. Either $t_{RCH(\text{MIN.})}$ or $t_{RRH(\text{MIN.})}$ should be met in read cycles.
15. In early write cycles, $t_{WCH(\text{MIN.})}$ should be met.
16. $t_{DS(\text{MIN.})}$ and $t_{DH(\text{MIN.})}$ are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS(\text{MIN.})}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
18. The column "trac = 60 ns" is not applicable to MC-422000A36.

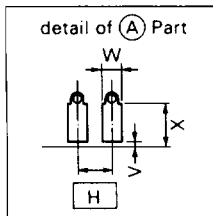
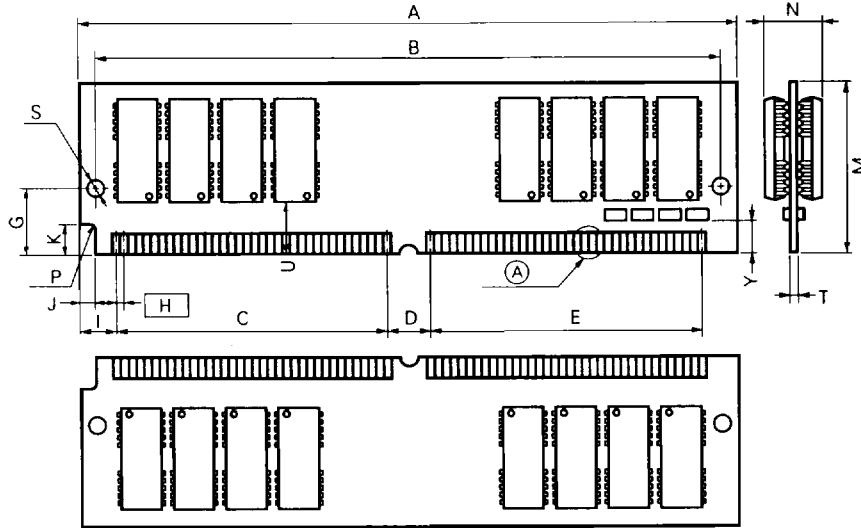
Timing Chart

Please refer to Timing Chart 2, page 375.

Package Drawings

MC-422000A32B, 422000A32F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

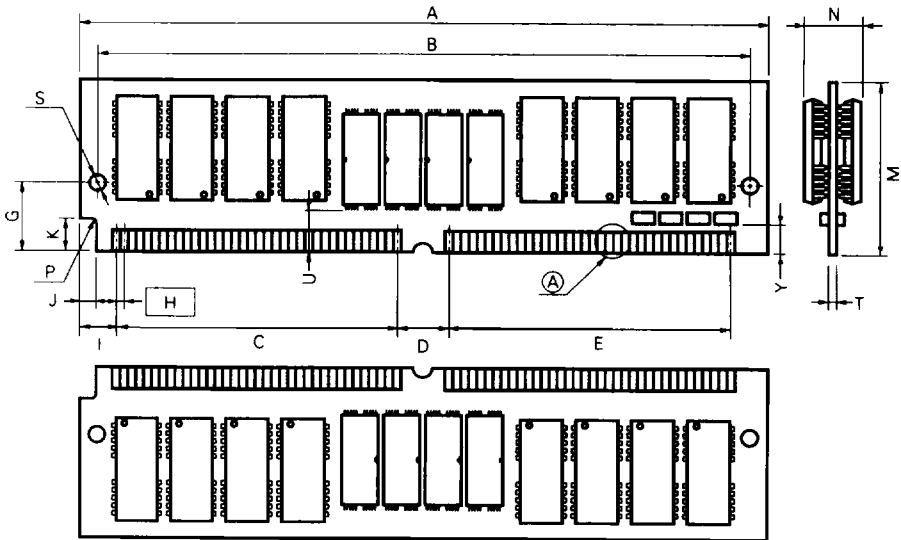


M72B-50A22-1

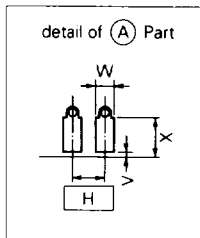
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 2.0	R 0.079
S	∅3.18	∅0.125
T	1.27 ^{+0.01} _{-0.08}	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

(Not Applicable)

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



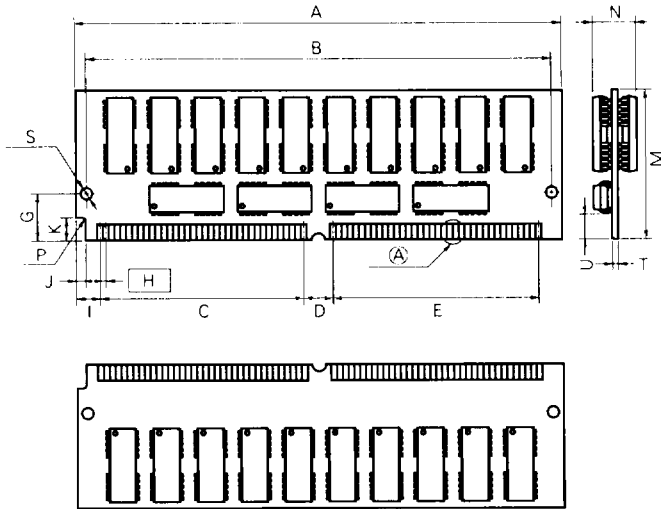
M72B-50A20-1



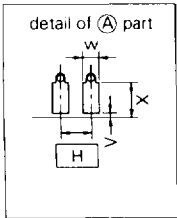
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.354 MAX.
P	R 2.0	R 0.079
S	∅3.18	∅0.125
T	1.27 ^{+0.08} ₀	0.050±0.004
U	5.32 MIN.	0.209 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

MC-422000A36BJ, 422000A36FJ

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M72B-50A44



ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	1.27 ^{+0.01} _{-0.02}	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.