MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW9002-1
MHW9002-2
MHW9002-3
MHW9002-4

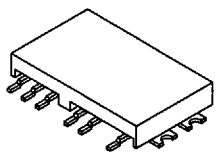
Motorola Preferred Devices

The RF Line
UHF GaAs FET Power Amplifiers

Designed for use in a wide variety of telecommunications equipment, including portable cellular applications, satellite cellular applications, gateways and satellite stations. All MHW9002 Series modules are capable of wide power range control (30 dB typical), operate from a 5.8 volt supply and require only 5 mW of RF input power.

- High Efficiency
- Specified 5.8 Volt Characteristics:
  RF Input Power — 5.0 mW (7 dBm)
  RF Output Power — 1.41 W (31.5 dBm)
  Minimum Gain — 24.5 dB
  Minimum Efficiency – 55%
  Harmonics — –30 dBc Max @ 2 f_o
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Epoxy Glass Substrate Eliminates Possibility of Substrate Fracture

31.5 dBm
824 to 925 MHz
HIGH EFFICIENCY
RF POWER
AMPLIFIERS



CASE 420A, STYLE 1

MAXIMUM RATINGS (Range Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD2}	10	Vdc
DC Bias Voltage	$V_{GG1, 2}$	–6	Vdc
DC Control Voltage	V_{DD1}	10	Vdc
RF Input Power	P_{in}	15	dBm
RF Output Power (V_S = 9 Vdc)	P_{out}	33	dBm
Operating Case Temperature Range	T_C	–30 to +100	°C
Storage Temperature Range	T_{stg}	–30 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{DD1} \leq 5.8$ Vdc, V_{DD2} = 5.8 Vdc, $V_{GG1} = V_{GG2}$ = –4.0 Vdc, P_{out} = 31.5 dBm for MHW9002-1, -2, -4; $V_{DD1} \leq 6.0$ Vdc, V_{DD2} = 6.0 Vdc, $V_{GG1} = V_{GG2}$ = –4.0 Vdc, P_{out} = 32 dBm for MHW9002-3; P_{in} = 7 dBm; T_C = +25°C, 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range MHW9002-1 MHW9002-2 MHW9002-3 MHW9002-4	BW	824 870 890 898		849 905 915 925	MHz
Output Power, Low Voltage (T_C = –30 to +80°C, $V_{DD1} = V_{DD2}$ = 5.0 Vdc)	P_{out1}	29.3	30	—	dBm
Output Power, Zero Control Voltage (V_{DD1} = 0 Vdc; P_{in} = 7 dBm)	P_{out2}	—	—	6	dBm
Gate Current (1)	I_{GG}	—	—	5	mA
Efficiency (1)	η	55	60		%
Input VSWR (1)	$VSWR_{in}$		—	3.0:1	—
Harmonics (1) $2f_o$ to $4f_o$				–30	dBc

NOTE:
1. Adjust V_{DD1} for Specified P_{out}, V_{DD1} = 5.8 Vdc Max for MHW9002-1, -2, & -4. V_{DD1} = 6.0 Vdc Max for MHW9002-3.

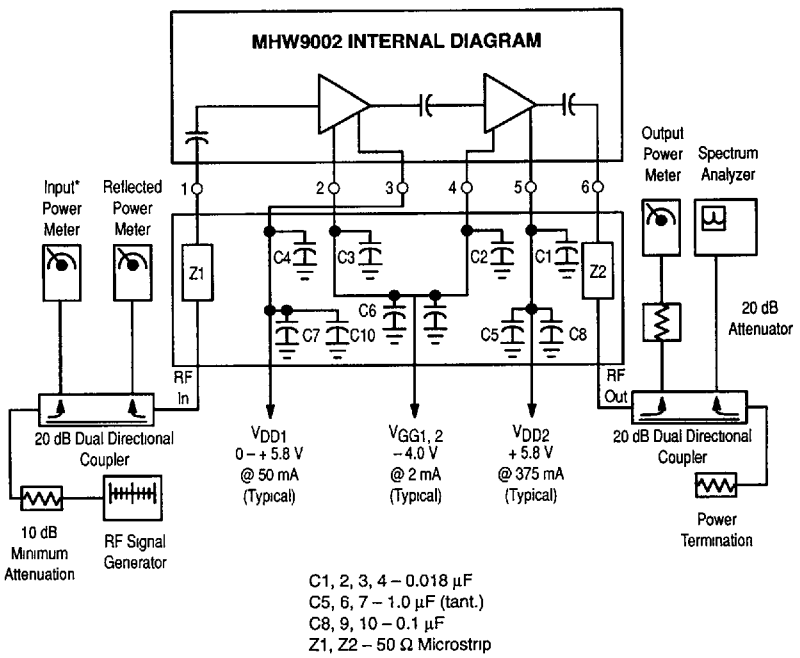
(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS — continued ($V_{DD1} \leq 5.8$ Vdc, $V_{DD2} = 5.8$ Vdc, $V_{GG1} = V_{GG2} = -4.0$ Vdc, $P_{out} = 31.5$ dBm for MHW9002-1, -2, -4; $V_{DD1} \leq 6.0$ Vdc, $V_{DD2} = 6.0$ Vdc, $V_{GG1} = V_{GG2} = -4.0$ Vdc, $P_{out} = 32$ dBm for MHW9002-3; $P_{in} = 7$ dBm; $T_C = +25°C$, 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Noise Power (In 20 kHz Bandwidth, 45 MHz Above f_O, $V_{DD2} = 5$ to 7 Vdc, $V_{DD1} = 0$ to 5.8 Vdc)	P_{N1}	—	—	−95	dBm
Noise Power (In 20 kHz Bandwidth, 45 MHz Above f_O, $V_{DD2} = 5$ to 7 Vdc, $V_{DD1} = 0$ to 5.8 Vdc, $T_C = -30°C$ to $T_C = +80°C$)	P_{N2}	—	—	−92	dBm
Stability ($V_{DD1} = 0$ to 7 Vdc, $P_{in} = 4$ to 10 dBm, $V_{DD2} = 4.5$ to 8 Vdc, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	—	All Spurious Outputs more than 60 dB Below Desired Signal			
Load Mismatch Stress ($V_{DD2} = 8$ Vdc, $P_{out} = 31.5$ dB Load VSWR = 20:1, All Phase Angles at Frequency of Test) (2)	ψ	No Degradation in Output Power Before and After Test			

NOTE:
2. Adjust V_{DD1} for Specified P_{out}, $V_{DD1} = 8.0$ Vdc Max for MHW9002-1, -2, -3, & -4.



C1, 2, 3, 4 – 0.018 µF
C5, 6, 7 – 1.0 µF (tant.)
C8, 9, 10 – 0.1 µF
Z1, Z2 – 50 Ω Microstrip

*Module input power is forward power as sampled by the directional coupler and read on the input power meter.

Figure 1. UHF Power Module Test Circuit Diagram

TYPICAL CHARACTERISTICS

MHW9002-1

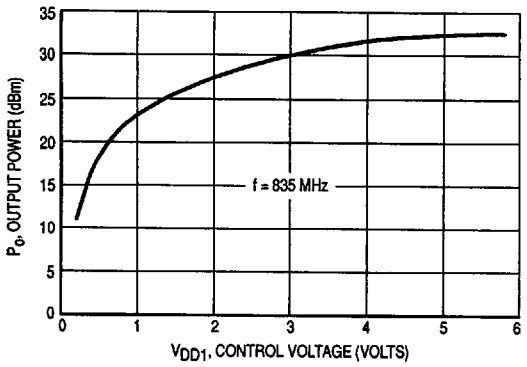


Figure 2. Output Power versus Control Voltage

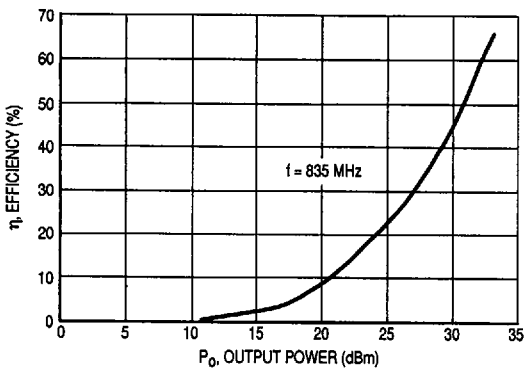


Figure 3. Efficiency versus Output Power

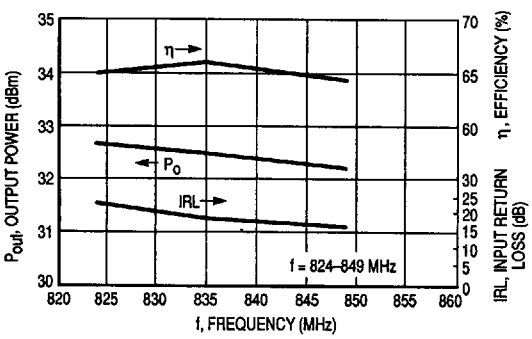


Figure 4. Output Power, Efficiency, Input Return Loss versus Frequency

MHW9002-2

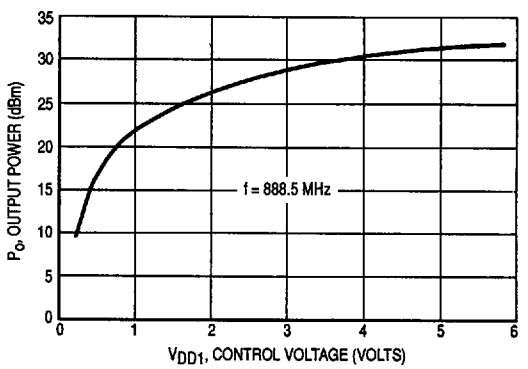


Figure 5. Output Power versus Control Voltage

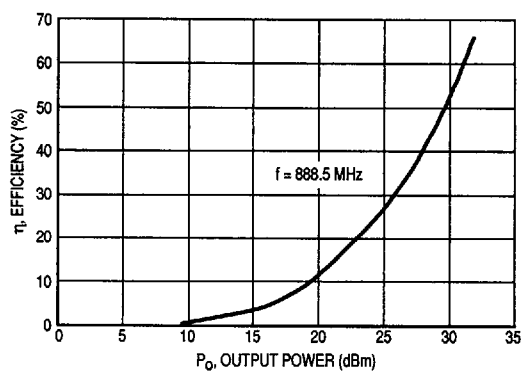


Figure 6. Efficiency versus Output Power

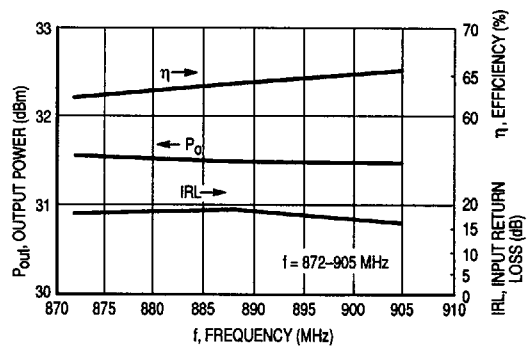


Figure 7. Output Power, Efficiency, Input Return Loss versus Frequency

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TYPICAL CHARACTERISTICS

MHW9002-3

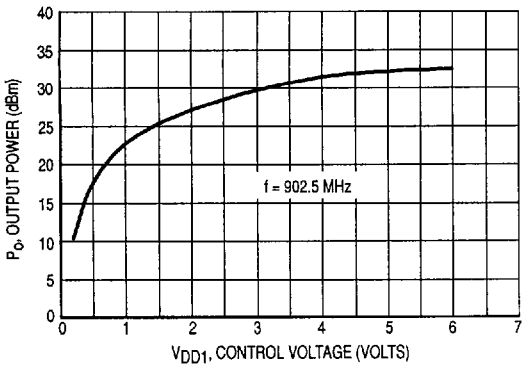

Figure 8. Output Power versus Control Voltage

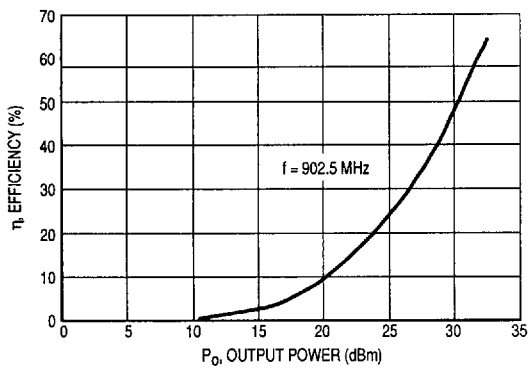

Figure 9. Efficiency versus Output Power

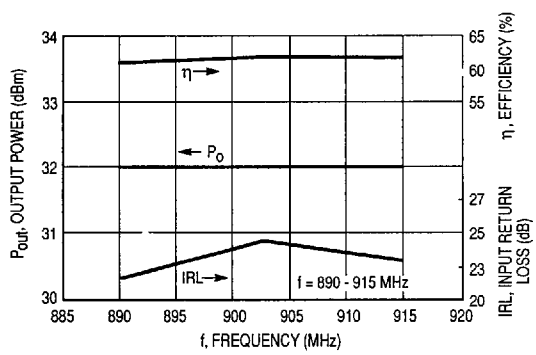

Figure 10. Output Power, Efficiency, Input Return Loss versus Frequency

MHW9002-4

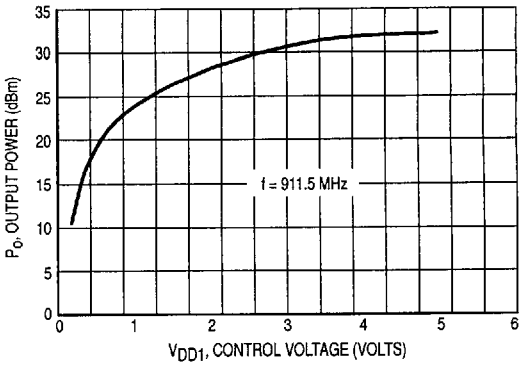

Figure 11. Output Power versus Control Voltage

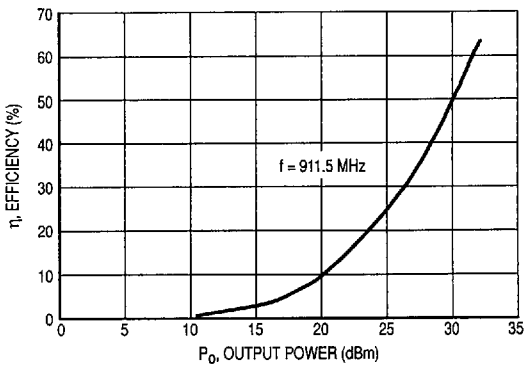

Figure 12. Efficiency versus Output Power

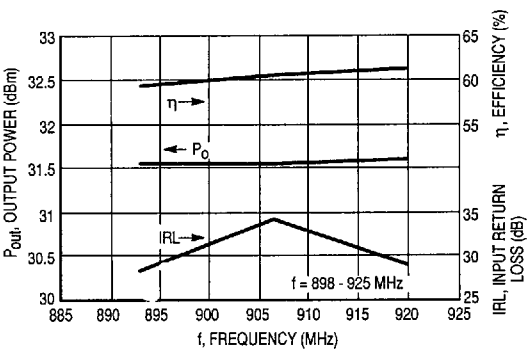

Figure 13. Output Power, Efficiency, Input Return Loss versus Frequency

APPLICATIONS INFORMATION

Mounting Considerations

For the MHW9002 Series module, mounting is done by soldering the four "feet" to a suitable heatsink. This can be done with a low temperature solder such as 52% In, 48% Sn and type "R" flux which liquifies below 150°C. Under no circumstances should the MHW9002 Series modules be heated to a temperature greater than 165°C (temperature of the flange proper). Internal construction of the module has been achieved using 36% tin, 62% lead, and 2% silver solder which liquifies at about 180°C. Also, remember that the modules are NOT hermetic.

Nominal Operation

All electrical specifications are based on the nominal conditions of $V_{DD1} \leq 5.8$ Vdc, $V_{DD2} = 5.8$ Vdc, $V_{GG1,2} = -4$ Vdc, and P_{out} equal to 31.5 dBm ($V_{DD2} = 6.0$ Vdc, $V_{DD1} \leq 6.0$ Vdc, $V_{GG1,2} = -4$ Vdc and P_{out} equal to 32.0 dBm for the MHW9002-3). While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the published specifications is not recommended unless prior communications regarding intended use have been made with a factory representative.

Gain Control

The module output power should be limited to specified value. The preferred method of power control is to fix $V_{DD2} = 5.8$ Vdc (Pin 5) (6.0 Vdc for the MHW9002-3) and $V_{GG1,2} = -4$ Vdc (Pins 2, 4), P_{in} (Pin 1) at 5 mW, and vary V_{DD1} (Pin 3) voltage.

Decoupling

External decoupling networks are recommended to ensure stable operation of the device. Pins 2, 3, 4, and 5 are internally bypassed with a 1000 pF chip capacitor. Additional external decoupling is recommended as shown in Figure 1. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

Handling Considerations

GaAs FETs are more sensitive to electrostatic discharge (ESD) than Si bipolar transistors. Therefore, steps should be taken in handling GaAs products to prevent damage. The use of ground straps, grounded breakers and test equipment is strongly recommended.

Soldering Leads

Be sure the soldering iron is grounded. Temperature of the iron should not exceed 350°C. Apply heat to a lead to be soldered for not more than 5 seconds.

Load Mismatch

During final test each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{DD2} = 8.0$ Vdc and $V_{GG1,2} = -4$ Vdc, P_{in} at 5 mW, and V_{DD1} set for 31.5 dBm output power (32.0 dBm for the MHW9002-3), and VSWR equal to 20:1.

Biasing and Use Considerations

In all cases, RF input power should not be applied until the bias voltages have been applied, and RF input power should be turned off prior to removing the bias voltages. Bias application should be timed such that gate voltage ($V_{GG1,2}$) is always applied before the drain voltages (V_{DD}), and, when returning to the standby mode, gate voltage should only be removed once the drain voltages have been removed.

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