4-TRACK PCM-MELODY WITH VOICE SYNTHESIZER (BandDirector™ Series)

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1. GENERAL DESCRIPTION

The W561xxx is one of the derivatives of the BandDirector™ familiy. It consists of a 4-bit μC, two voice synthesizers, one 4-track PCM-Melody generator, and one shared ROM.

The muti-tasking operation for voice synthesis and 4-track PCM-Melody generation is implemented by dedicated H/W that can output the speech voice in parallel with the background music. With the 4 bit kernel, which can execute instructions of up to 12 KIPS (Kilo-Instructions Per Second), and high quality dual speaker output, you will be amazed at the possible applications. W561xxx provides you with a total solution in one chip.

In addition, the W561xxx's user-friendly development environment can effectively reduce your design period and help you easily tool your projects by yourself with the ICE and emulation kit.

There are 10 kinds of W561xxx IC bodies (see table below).

PART NO.	W561S15	W561S20	W561S25	W561S30	W561S40
Duration	15 sec	20 sec	25 sec	30 sec	40 sec
Main ROM size	640 Kbit	768 Kbit	896 Kbit	1024 Kbit	1472 Kbit
PART NO.	**W561S50**	**W561S60**	**W561S80**	**W561S99**	**W561M02**
Duration	50 sec	60 sec	80 sec	100 sec	120 sec
Main ROM size	1760 Kbit	1920 Kbit	3072 kbit	3520 Kbit	3968 Kbit

Note: The voice durations are estimated by 8.0 KHz sampling rate

Possible applications are:

- Programmed voice synthesis with background music or speech
- I/O interactive voice synthesis to accompany background music or speech
- Demo of music songs with possible dynamic timbre/tempo changes during playback
- Q&A games
- Edutainment toys

2. FEATURES

- Multi-engine processor parallel management with μC, speech and PCM Melody
  - μC // (Synthesizer1 or 4-track PCM-Melody) // Synthesizer2 (//: in parallel)
  - μC, with basic ALU, 64-nibble RAM (including 8 working registers) and an 8-bit timer

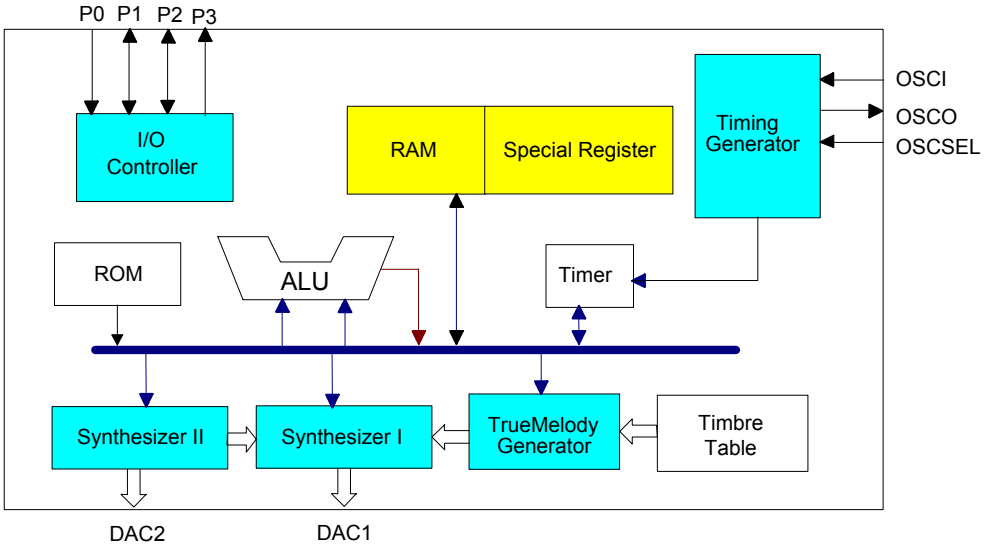
    The W561&W562 user RAM initialization value is not constant. It is random. So, user must initial constant value.
  - Synthesizer1 capable of voice syntheses with Sample rate @4.8/6/8/12 KHz
  - Synthesizer2, same as synthesizer1
  - 4-track PCM-Melody with total 16 Kbyte Timbre table, which can store up to 16 kinds of timbre samples.

- The on-chip ROM is shared among program, voices and melody notes
- ICE & ROM chips use different Rosc. Rosc for mass production should check “W561 Freq vs R.pdf” file for more details.

- Wide operating voltage range: 2.4 to 5.5 volts
- Low power consumption (V_{DD} = 5 Volt)
  - Standby current < 2 μA
  - Operating current (no load with ring oscillator) < 1 mA
- Main oscillator: Crystal/ Ring oscillation selectable by pin option
- Input/ Output port
  - Port for input only: 1 port/4 pins
  - Input/ Output ports: 2 ports/8 pins
  - Port for output only: 1 port/4 pins
  - Can offer a direct row and column matrix of up to 72 (8 × 9) keys
- Interrupts
  - Internal interrupts: Timer
  - External interrupts: TG (port 0, port1), POI (Power On Initialization)
  - Priority: POI > TG > Timer
- DAC1/2 provided for stereo voice output
- Melody + Voice output for DAC1
- TG interrupt provided
  - Shared TG interrupt for Port0/Port1 input.
  - Global TG interrupt enable controlled (bit3 of the IER register)
  - Individual interrupt enable controlled (PER0 and PER1 registers)
- Built-in 8 bit programmable down count timer
  - One of two internal clock frequencies can be selected
  - Desired Timer interval = (preset value +1) × 1/F_T
    (F_T: 32 Hz or 32 KHz dependent on the bit0 of the MODE register, at Fosc = 3 MHz)
- Powerful instruction set:
  - Arithmetic: ADD, ADDC, SUB, SUBC, INC, DEC, SETB, CLRB
  - Logic Operation: AND, OR, XOR, NOT
  - Shift & Rotate: RORC, ROLC, SHRC, SHLC
  - Date move: LD, LDR, MV
  - Branch: JP, JB0, JB1, JB2, JB3, JZ, JNZ, JC, JNC, JBZ1, JBZ2, CJNE, CJE, DJNZ, DJZ
  - Subroutine: CALL, RTN, RTI
  - Others: NOP, END, EN INT, DIS INT, PLAY CH1, STOP CH1, STOP CH2
- 8-level STACK shared by CALL, Timer, Synthesizer and TG

- Dynamic register controlled by LD instructions
  - Volume control (VOL1/VOL2 registers for DAC 1/2)
  - Melody Timbre control (Timbre0/1/2/3 registers for CH0/1/2/3)
  - Melody Speed control (Tempo register)
- 4-track PCM-Melody with
  - Timbre-based melody synthesis
  - Note number: only limited by ROM size
  - Timbre ROM size: 16 Kbyte
  - Note span: 49 notes, 4 octaves
  - 9 kinds of timbre size: 1K/2K/3K/4K/6K/8K/10K/12K/16K bytes per timbre
  - 7 kinds of loop size: one-shot /128/256/512/1K/2K/4K bytes per timbre
  - 6 kinds of note sustainments (1/4, 1/2, 1, 4/3, 2, 4 sec)
  - 4 kinds of envelope effect
  - User-defined timbre library to achieve various kind of instrument effects
  - Midi-conversion utility provided
- Multi-tasking operation via interrupt for automatic voice segment concatenation
  - Melody voice or Speech voice can be easily concatenated with symbol "+"
  - Example: PLAY CH1, H4 + Melody1 + Speech1 + Speech2 + Melody2 + T4
    The DAC1 of the W561xxx will play Melody1, Speech1, Speech2, and Melody2 sequentially.
- The length of the voice segment is only limited by the ROM size
- Speech section control
  - Fading effect, eight levels of volume control (0-7)
  - Sample rate control (4.8K/6K/8K/12K)
  - Example: PLAY CH2, H4 + speech1_SV + T4; S: define the sample rate, V: define the volume
- Provides ICE (In Circuit Emulation) system for easy debugging
  - Free Run
  - Stop Run
  - Program Reset
  - Step Into
  - Step Over
  - Go To Cursor
  - Break point
  - Register read/ modify

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

PARAMETER	I/O	DESCRIPTION
TEST	I	Test pin, internally pulled low
P0.0–P0.3	I	Interruptable input pins, internally pulled high.
P1.0–P1.3	I/O	I/O multiplexed port 1. The port 1 is interruptable, if selected as input pins
P2.0–P2.3	I/O	I/O multiplexed port 2.
P3.0–P3.3	O	Output port 3.
V_{SS}	-	Negative power supply.
$\overline{RESET}$	I	Reset all, functions as POR (Power On Reset), internally pulled high.
V_{DD}	-	Positive power supply.
OSCI	I	Connect R_{OSC} to V_{DD} or Crystal between OSCI & OSCO to generate the 3 MHz master frequency.
OSCO	O	
DAC1	O	Current output of channel 1 for driving an external speaker
DAC2	O	Current output of channel 2 for driving an external speaker
OSCSEL	I	Oscillator type selecting pin, internally kept floating. Connect to V_{DD} to select Crystal type, connect to GND to select ring oscillator type.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	V_{DD}–V_{SS}	-	-0.3 to +7.0	V
Input Voltage	V_{IN}	All Inputs	V_{SS} -0.3 to V_{DD} +0.3	V
Storage Temp.	T_{STG}	-	-55 to +150	°C
Operating Temp.	T_{OPR}	-	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 DC Characteristics

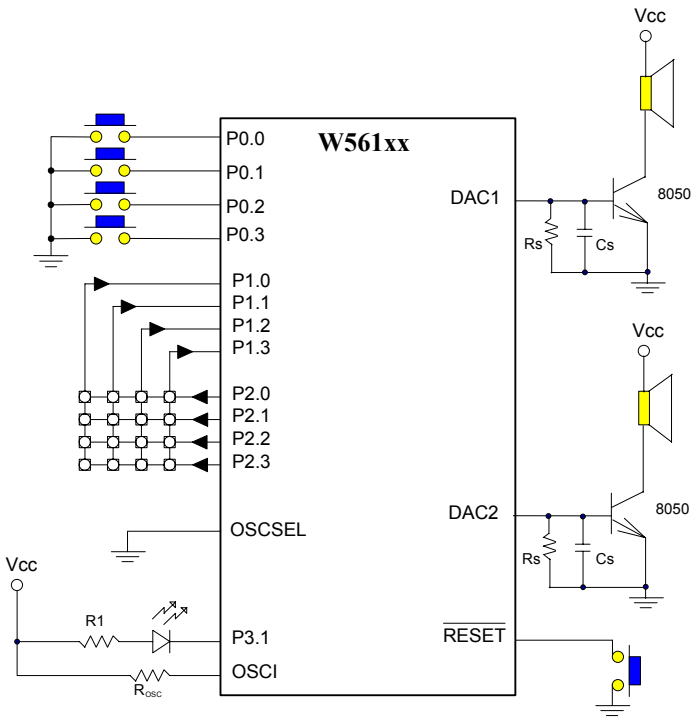
(V_{DD}–V_{SS} = 3.0V, F_M = 3 MHz, T_A = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}	-	2.4	-	5.5	V
Standby Current	I_{DD1}	No load, No Playing	-	-	2	μA
Operating Current (Crystal Type)	I_{OP1}	No load	-	-	1	mA
Operating Current (Ring Type)	I_{OP2}	No load	-	-	1	mA
Input Low Voltage	V_{IL}	All Input Pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All Input Pins	0.7 V_{DD}	-	V_{DD}	V
Input Current for P0, P1, P2	I_{IN}	V_{DD} = 3V, V_{IN} = 0V	-	-	-6	μA
Input Current for $\overline{\text{RESET}}$	I_{IN1}	V_{DD} = 3V, V_{IN} = 0V	-	-	-6	μA
Output Current of P1, P2, P3	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	5	-	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.7V	-3	-	-	mA
DAC1/2 (D/A full Scale)	I_{DAC}	V_{DD} = 4.5V, R_L = 100Ω	-4.0	-5.0	-6.0	mA
Pull-low Resistor	R_{PL}	TEST, OSCSEL Pins	100	-	-	KΩ

5.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main-clock Frequency	FM	Ring type, ROSC = 1.2 MΩ	2.7	3	3.3	MHz
		Crystal type	-	3	-	
Frequency Deviation by Voltage Drop for Ring Type Oscillator	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$	-	-	10	%
Machine Cycle Time	TINS	One machine cycle	1/12	-	1/6	mS
POR Pulse Width	TPOR	-	1	-	-	μS

6. APPLICATION CIRCUIT



* R1 = 220 Ω, Rs = 330 - 680 Ω, Rosc = 1.2MΩ, Cs = 0.1 μF

* It is suggested to add 0.1uF capacitor between V_{DD} and V_{SS} for increasing the stability on Power-On-Rest condition.

7. REVISION HISTORY

REVISION	DATE	DESCRIPTION
A1	Oct-1998	Preliminary release.
A2	Dec-1998	Add BandDirector trade mark
A3	Feb-1999	Remove the 'preliminary' mark
A4	Jan-2001	In page 1, add statement "The W561&W562 user RAM initialization value is not constant. It is random."
A5	June 3, 2003	In page 2, add statement "ICE & ROM chips use different Rosc. Rosc for mass production should check "W561 Freq vs R.pdf" file for more details."

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