MITEL
SEMICONDUCTOR

SL2030

High Performance Broadband Mixer Oscillator

Preliminary Information

DS5116 Issue 2.1 October 1999

Features

- Single Chip Broadband Solution
- Wide Dynamic Range RF Input
- Low Phase Noise Balanced Internal Local Oscillator
- Wide Frequency Range: 50 to 860 MHz
- ESD Protection 2kV min., MIL-STD-883B Method 3015 Cat.1 (Normal ESD handling procedures should be observed)

Applications

- Double Conversion Tuners
- Digital Terrestrial Tuners
- Data Transmit Systems
- Data Communications Systems

The SL2030 is a bipolar, broadband wide dynamic range mixer oscillator, optimised for applications as an upconverter in double conversion tuner systems. It also has application in any system where a wide dynamic range broadband frequency converter is required.

The SL2030 is a single chip solution containing all necessary active circuitry and simply requires an external tuneable resonant network for the local oscillator. The block diagram is shown in Figure 1 and pin connections are shown in Figure 2.

In normal application the high IF output is interfaced through appropriate impedance matching to the high IF filter. The RF input preamplifier of the device is designed for low noise figure within the operating region and for high intermodulation distortion intercept so offering good signal to noise plus composite distortion spurious performance.

The preamplifier also provides gain to the mixer section and back isolation from the local oscillator section. The approximate model of the RF input is shown in Figure 3.

Ordering Information

SL2030/IG/MP1S (Tubes)
SL2030/IG/MP1T (Tape and Reel)

The output of the preamplifier is fed to the mixer section which is optimised for low radiation application. In this stage the RF signal is mixed with the local oscillator frequency, which is generated by an on-chip oscillator. The oscillator block uses an external tuneable network and is optimised for low phase noise. A typical application is shown in Figure 6 and the typical phase noise performance in Figure 5. This block also contains a buffer-amplifier to interface with an external PLL to allow for frequency synthesis of the local oscillator.

The IF output must be loaded differentially in order to get best intermodulation performance. The approximate model of the IF output is shown in Figure 4.

In application care should be taken to achieve symmetric balance to the IF outputs to maximise intermodulation performance.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0·3V to +7V
RF differential input voltage	2·5V
All I/O port DC offset	−0·3 to V_{CC} +0·3V
Storage temperature	−55°C to +150°C
Junction temperature	+150°C
Package thermal resistance	
Chip to ambient, θ_{JA}	20°C/W
Chip to case, θ_{JC}	80°C/W

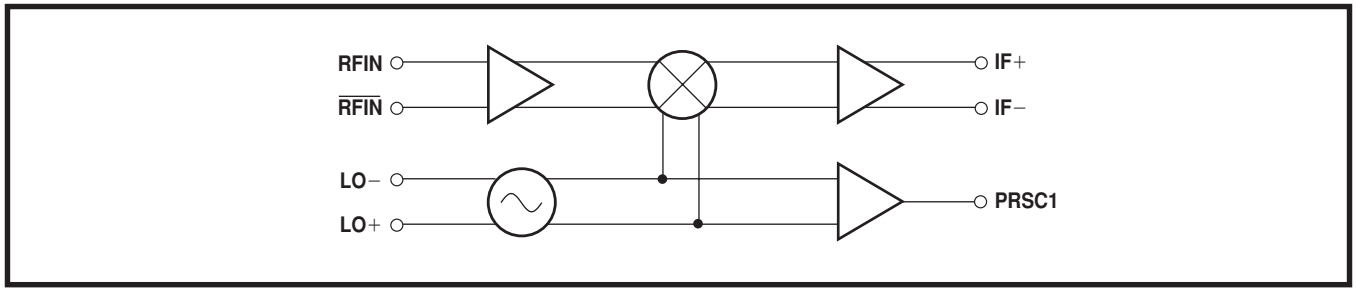


Figure 1 SL2030 block diagram

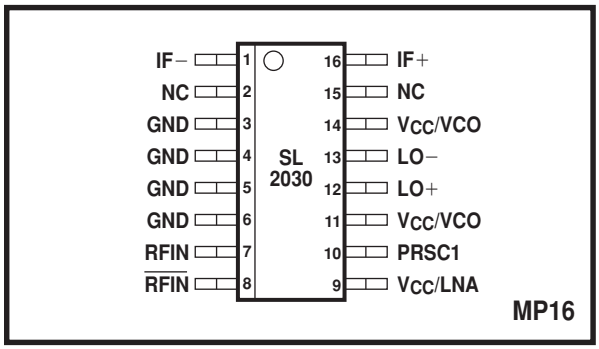


Figure 2 Pin connections - top view

Quick Reference Data

All data applies with circuit component values given in Table 1

Characteristic	Value	Units
RF input operating frequency range	50-860	MHz
Input noise Figure, SSB, 50 to 860MHz	8	dB
Conversion gain 50 to 860MHz	8	dB
IIP3 input referred	121	dBμV
CTB (fully loaded matrix)	<-64	dBc
P1dB input referred	104	dBμV
IIP2 input referred	145	dBμV
Composite 2nd order (fully loaded matrix)	<-62	dBc
LO phase noise at10 kHz offset, f_{RF} 50 to 860MHz, application as in Figure 6	<-85,see Figure 5	dBc/Hz
LO leak to RF input Fundamental Second harmonic	 72 92	 dBμV dBμV

Electrical Characteristics

Tamb = −40°C to +85°C, V_{CC} = 5V ±5%, V_{EE} = 0V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	9,11,14			99	mA	IF output pins 1 and 16 will be nominally connected to V_{CC} through the differential balun load as in Figure 6
Input frequency range	7,8	50		860	MHz	
Composite peak input signal	7,8		97		dBμV	Operating condition only
Input impedance	7,8					See Figure 3
Input return loss	7,8	−5		−25	dB	
Conversion gain		8	10	11	dB	Differential voltage gain to 50Ω load on output of impedance transformer as in Figure 6.
Gain variation across operating range		−1		+1		50-860MHz
Gain variation within channel				0·5	dB	Channel bandwidth 8MHz within operating frequency range
Through gain				−20	dB	45-865MHz
Noise figure		6·5	8	10		

cont…

Electrical Characteristics (continued)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
IIP2		139	145	153	dBμV	Two tones at 92dBμV
IIP3		117	121	126	dBμV	Two tones at 92dBμV
Composite 2nd order			−62		dBc	128 channels at 62dBμV
LO operating range	12,13	1·0		2·1	GHz	Maximum tuning range 0·9GHz within band, application as in Figure 6
LO phase noise, SSB at 10kHz offset		−94	−87	−85	dBc/Hz	Application as Figure 6. See Figure 5 for a typical device
IF output frequency range	1,16	1		1·3	GHz	
LO and harmonic leakage to RF input						
Fundamental	7,8			72	dBμV	To device input
2nd harmonic	7,8			92	dBμV	To device input
LO Prescaler output swing	10	95			dBμV	Into 50Ω load
LO Prescaler output impedance	10	25		75	Ω	
IF output impedance	1,16					See Figure 4

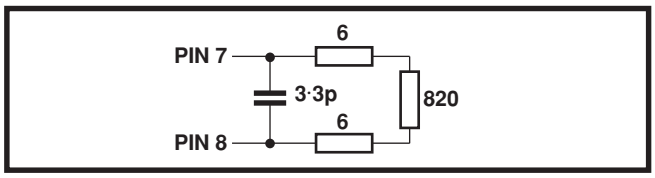


Figure 3 Approximate model of RF input

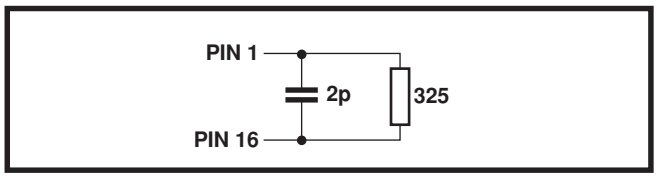


Figure 4 Approximate model of IF output

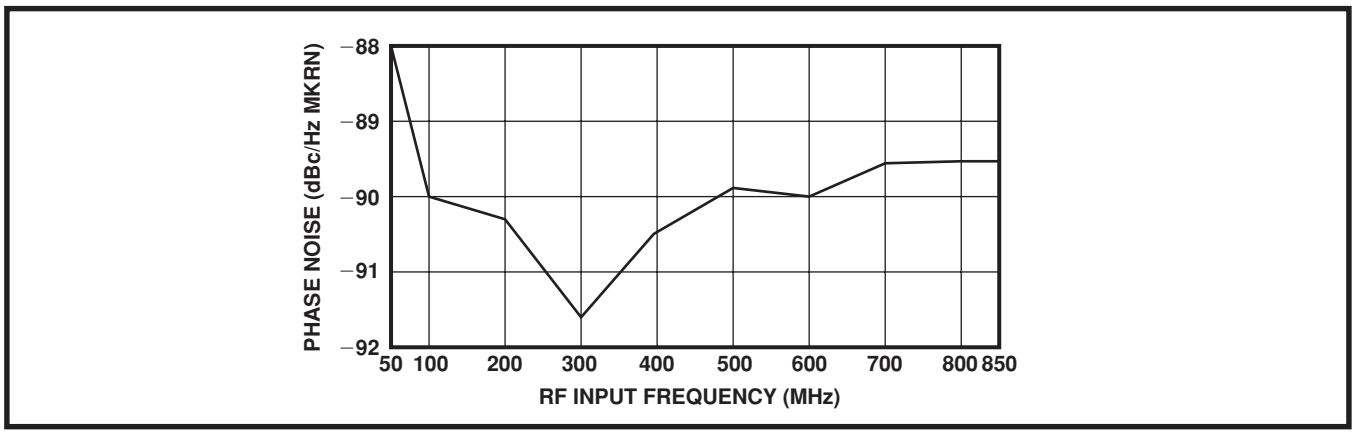


Figure 5 Phase noise performance

Application Notes

Figure 6 shows the SL2030 in a typical upconverter application. The network connected to RF input pin 7 and pin 8 is to improve the matching between the device input and the source. The source would normally be from a cable, via passive LPF and PIN-diode attenuator all designed for 75Ω characteristic impedance.

The network connected to the IF output pin 1 and pin 16 is a broadband tuned balun centred typically on 1·1 GHz. This matches the device output impedance of nominally 400Ω (balanced) to 50Ω (unbalanced).

The network connected to the LO pin 12 and pin 13 is a varactor diode loaded resonant microstrip line resonator. Fine adjustment of the tuning range can be achieved by shortening the line (top end) or by physically moving C19 (see Figure 6) closer to the LO pins. This extends the bottom end of the tuning range.

It is important to provide good decoupling on the 5V supplies and to use a layout which provides some isolation between the RF, IF and LO ports.

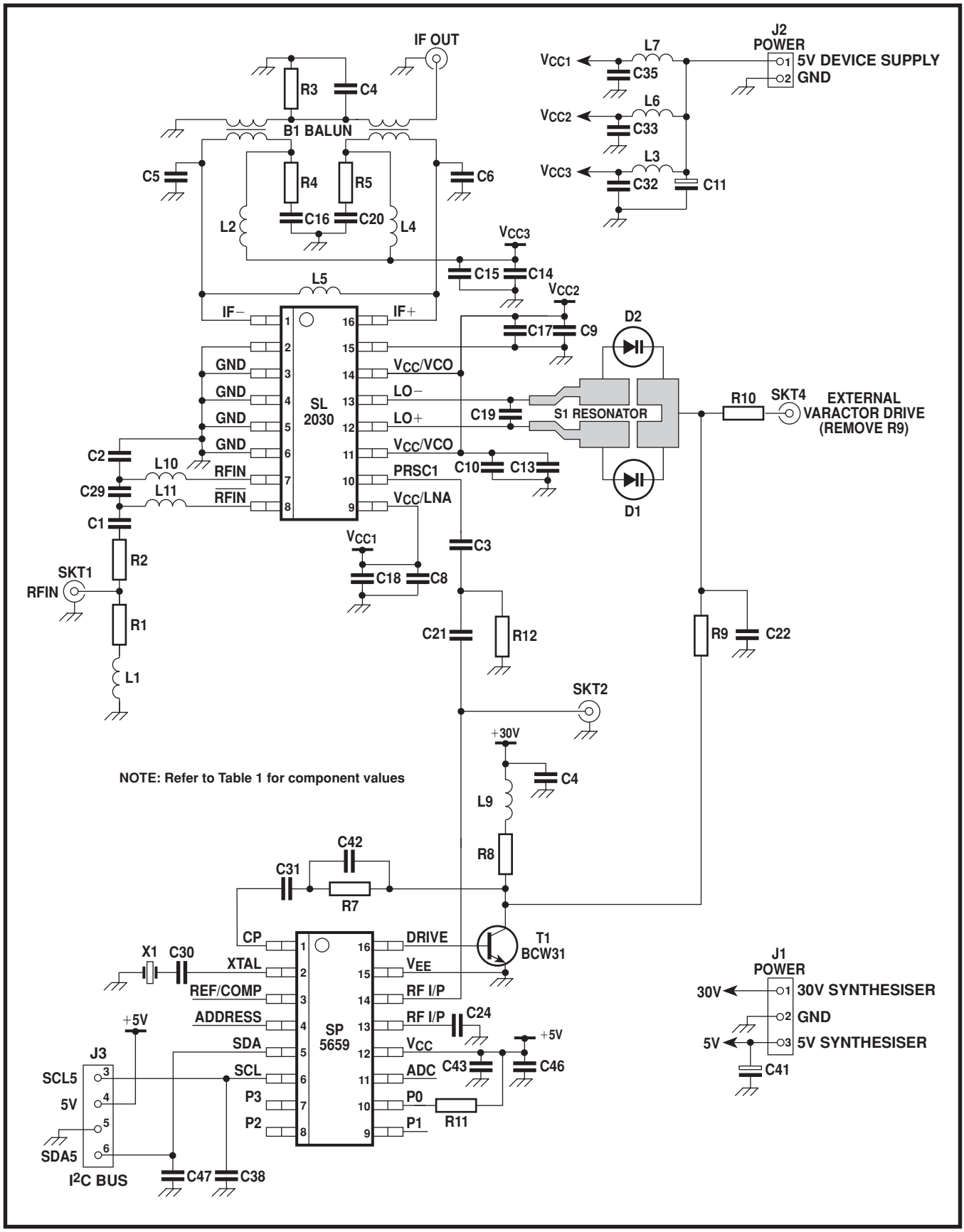


Figure 6 SL2030 upconverter application

Component	Value/type	Component	Value/type	Component	Value/type
C1	1nF	C26		L2	18nH
C2	1nF	C27		L3	220nH
C3	1 nF	C28		L4	18nH
C4	1·5pF	C29	1·5pF	L5	
C5	1pF	C30	18pF	L6	220nH
C6	1pF	C31	330nF	L7	220nH
C7		C32	1nF	L8	
C8	100pF	C33	1nF	L9	220nH
C9	100pF	C34	100nF	L10	6·8nH
C10	100pF	C35	1nF	L11	6·8nH
C11	10μF	C36		R1	220Ω
C12		C37		R2	20Ω
C13	100nF	C38	100pF	R3	1kΩ
C14	100nF	C39		R4	120Ω
C15	100pF	C40		R5	120Ω
C16	100pF	C41	4·7μF	R6	
C17	100nF	C42	3·3nF	R7	15kΩ
C18	100nF	C43	100nF	R8	22kΩ
C19	2pF	C44		R9	15kΩ
C20	100pF	C45		R10	1kΩ
C21	1nF	C46	100nF	R11	4·7kΩ
C22	33nF	C47	100pF	R12	50Ω
C23		D1	IT402	S1	Resonator (Figure 7)
C24	1nF	D2	IT402	T1	BCW31
C25		L1	100nH	X1	4MHz crystal

Table 1 Component values for Figure 6

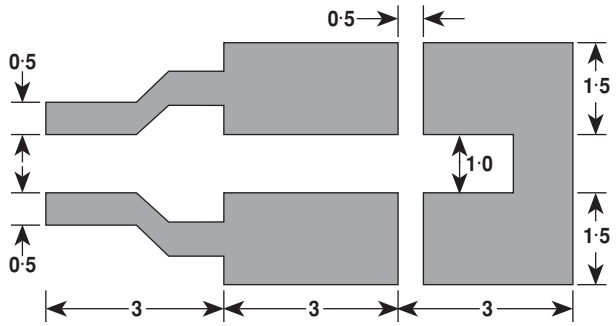
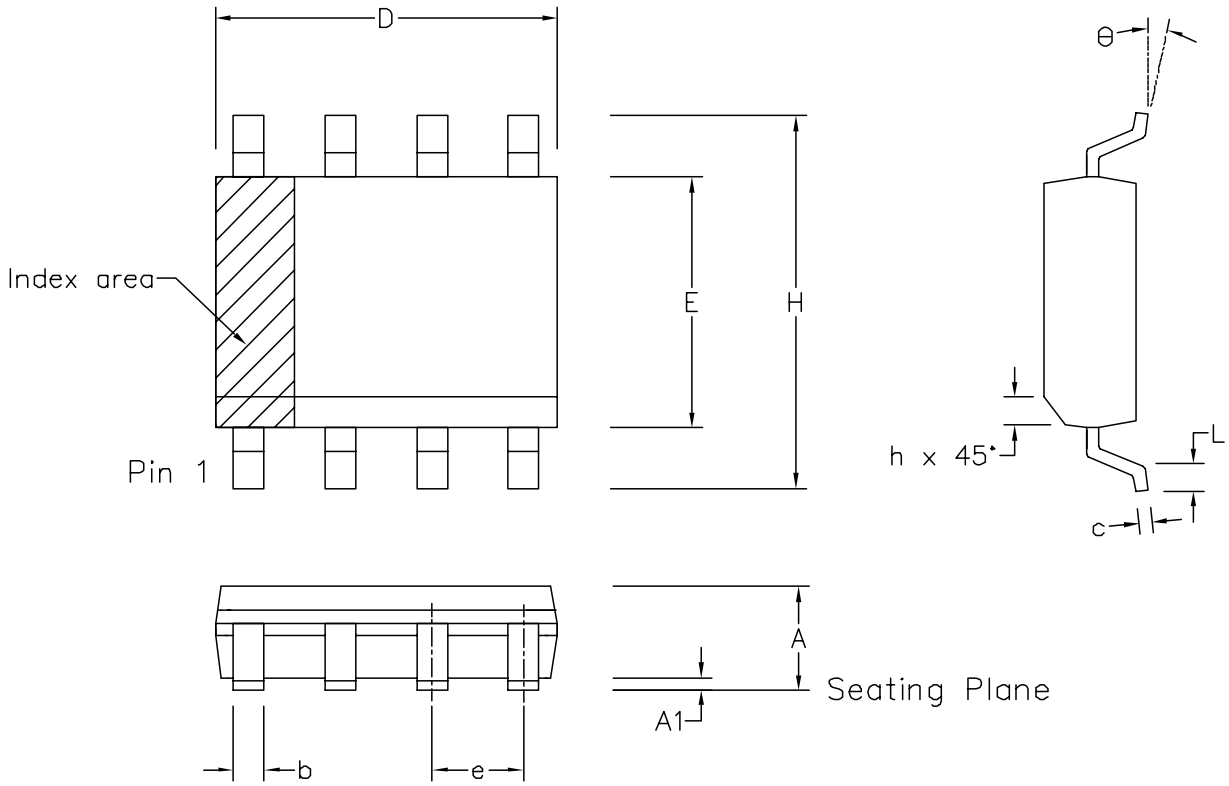


Figure 7 Microstrip resonator (dimensions are in mm)



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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APPROVED					

MITEL SEMICONDUCTOR

Title: Package Outline Drawing for 16 lds SOIC(N)-0.150" Body Width (MP)

Drawing Number
GPD00012

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