PLESSEY
Semiconductors

SP1650

DUAL A/D COMPARATOR

The SP1650 is a very high speed comparator utilising differential amplifier inputs to sense analogue signals above or below a reference level. An output latch provides a unique sample-hold feature.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock iinputs ($\overline{C_a}$ and $\overline{C_b}$) operate from ECL III or ECL 10,000 digital levels. When $\overline{C_a}$ is at a logic high level, Q_a will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q_a}$ is the logic complement of Q_a. When the clock in to a low logic level, the outputs are latched in their present state.

FEATURES

- P_D = 330mW typ/pkg (No Load)
- t_{pd} = 3.5ns typ.
- Input Slew Rate = 350V/us
- Differential Input Voltage: -5.0V to +5.0V (-30°C to +85°C)
- Common Mode Range: -2.5V to +3.0V (-30°C to +85°C)
- Resolution: ≤20mV (-30°C to +85°C)
- Drives 50 ohm lines

TRUTH TABLE

$\overline{C}$	V_1 V_2	Qn + 1	$\overline{Qn}$ + 1
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	Q_n	$\overline{Q_n}$

ϕ = Don't Care

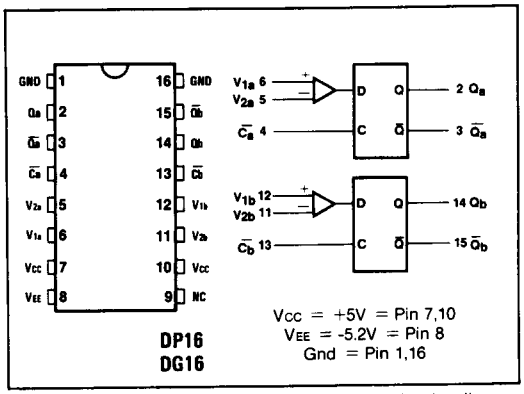


Fig.1(a) Pin connections (top view) Fig.1(b) Logic diagram

Operating temperature range:
-30°C to +85°C (Ceramic)
0°C to +75°C (Plastic)

ORDERING INFORMATION

SP1650DG (Industrial - Ceramic DIL package)
SP1650BB DG (Plessey High Reliability Ceramic DIL package)
SP1650 DP (Industrial - Plastic DIL package)
SP1650 BC DG (Military - Ceramic DIL package)

NOTE:
The BC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

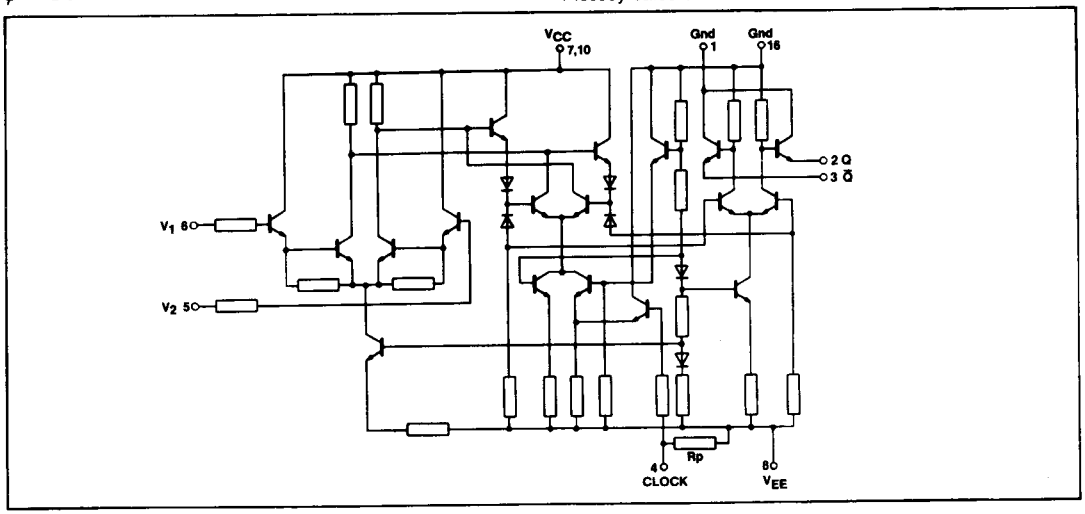


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} (3)	V_{EE} (3)
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note (4)				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin under test	SP1650 Test Limits (1) -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} (3)	V_{EE} (3)	Gnd
POWER SUPPLY																						
Drain current																						
Positive	I_{CC}	7,10	-	-	-	25*	-	-	mAdc	-	4,13	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
Negative	I_E	8	-	-	-	55*	-	-	mAdc	4,13	-	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
Input current	I_{IN}	6	-	-	-	10	-	-	μAdc	4	13	-	-	12	-	6	-	-	-	7,10	8	1,5,11,16
Input leakage current	I_R	6	-	-	-	7	-	-	μAdc	4	13	-	-	12	-	-	-	6	-	7,10	8	1,5,11,16
Input clock current	I_{INH}	4	-	-	-	350	-	-	μAdc	4	13	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
	I_{INL}	4	-	-	0.5	-	-	-	μAdc	-	13	-	-	6,12	-	-	-	-	-	7,10	4,8	1,5,11,16
Logic '1' output voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	-	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
		2									-	-	-	-	5,11	-	-	-	-			1,6,12,16
		2									-	-	-	-	-	6,12	5,11	-	-			1,16
		2									-	-	-	-	-	-	-	5,11	6,12			1,16
		3									-	-	-	-	6,12	-	-	-	-			1,5,11,16
		3									-	-	-	5,11	-	-	-	-	-			1,6,12,16
		3									-	-	-	-	-	5,11	6,12	-	-			1,16
		3									-	-	-	-	-	-	-	6,12	5,11			1,16
Logic '0' output voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	-	-	-	-	6,12	-	-	-	-	7,10	8	1,5,11,16
		2									-	-	-	5,11	-	-	-	-	-			1,6,12,16
		2									-	-	-	-	-	5,11	6,12	-	-			1,16
		2									-	-	-	-	-	-	-	6,12	5,11			1,16
		3									-	-	-	6,12	-	-	-	-	-			1,5,11,16
		3									-	-	-	-	5,11	-	-	-	-			1,16,12,16
		3									-	-	-	-	-	6,12	5,11	-	-			1,16
		3									-	-	-	-	-	-	-	6,12	5,11			1,16
Logic '0' threshold voltage (2)	V_{OHA}	1																				
		2	-1.065	-	-0.980	-	-0.910	-	Vdc	-	13	4	-	6	-	-	-	-	-	7,10	8	1,5,16
		2										-	4	-	6	-	-	-	-			
		3										4	-	-	6	-	-	-	-			
		3										-	4	6	-	-	-	-	-			
		4																				
Logic '0' threshold voltage (2)	V_{OLA}	1																				
		2	-	-1.630	-	-1.600	-	-1.555	Vdc	-	13	4	-	6	-	-	-	-	-	7,10	8	1,5,16
		3										-	4	-	6	-	-	-	-			
		2										4	-	-	6	-	-	-	-			
		4										-	4	6	-	-	-	-	-			

NOTES
1. All data is for ½ SP1650 except data marked (*) which refers to the entire package.
2. These tests done in order indicated. See Figure 6.
3. Maximum Power Supply Voltages (beyond which device life may be impaired): $|V_{EE}| + |V_{CC}| < 12V$ dc.
4. At all temperatures, $V_{A3} = +3.000V$, $V_{A4} = +2.980V$, $V_{A5} = -2.500V$ and $V_{A6} = -2.480V$.

Test temp.	TEST VOLTAGE (V) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} (1)	V_{EE} (1)	
-30°C	+2.000	See Note (4)		+1.040	+2.00	+7.00	-3.20	See Figure 4
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20	
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20	

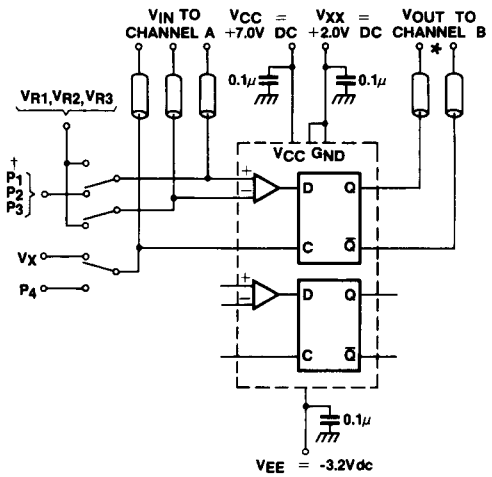
Characteristic	Symbol	Pin under test	SP1650 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} (1)	V_{EE} (1)	P1	P2	P3	P4
SWITCHING TIMES	$t_{6\cdot2\cdot}$	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
Propagation delay	$t_{6\cdot2\cdot}$	2								-	5	-					-	6	-	-
(50% to 50%)	$t_{6\cdot2\cdot}$	2								-	-	5					-	-	6	-
V-input to output	$t_{6\cdot3\cdot}$	3								5	-	-					6	-	-	-
	$t_{6\cdot3\cdot}$	3								-	5	-					-	6	-	-
	$t_{6\cdot3\cdot}$	3								-	-	5					-	-	6	-
	$t_{6\cdot2\cdot}$	2								5	-	-					6	-	-	-
	$t_{6\cdot2\cdot}$	2								-	5	-					-	6	-	-
	$t_{6\cdot2\cdot}$	2								-	-	5					-	-	6	-
	$t_{6\cdot3\cdot}$	3								5	-	-					6	-	-	-
	$t_{6\cdot3\cdot}$	3								-	5	-					-	6	-	-
	$t_{6\cdot3\cdot}$	3								-	-	5					-	-	6	-
Clock to output (2)	$t_{4\cdot2\cdot}$	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	-	-	-	1,11,16	7,10	8	6	-	-	4
	$t_{4\cdot2\cdot}$	2								6	-	-	-				5	-	-	
	$t_{4\cdot3\cdot}$	3								6	-	-	-				5	-	-	
	$t_{4\cdot3\cdot}$	3								5	-	-	-				6	-	-	
Clock enable time (3)	t_{setup}	6	-	-	2.5	-	-	-	ns	5	-	-	-	1,11,16	7,10	8	6	-	-	4
Clock aperture time (3)	t_{ap}	6	-	-	1.5	-	-	-	ns	5	-	-	-	1,11,16	7,10	8	6	-	-	4
Rise time	$t_{2\cdot}$	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
(10% to 90%)	$t_{3\cdot}$	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
Fall time	$t_{2\cdot}$	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
(10% to 90%)	$t_{3\cdot}$	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-

NOTES AND MAXIMUM RATINGS

1. Maximum power supply voltages (beyond which device life may be impaired):
   $|V_{CC}| + |V_{EE}| = 12VDC$
2. Unused clock inputs may be tied to ground.
3. See Fig. 10.
4. At all temperatures, $V_{R2} = +4.9000V$ and $V_{R3} = -0.400V$.
5. Storage temperature: -65°C to +150°C
6. Operating junction temperature <175°C

Thermal characteristics

$\theta_{JA} = 110°$ C/W
$\theta_{JC} = 33°$ C/W



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

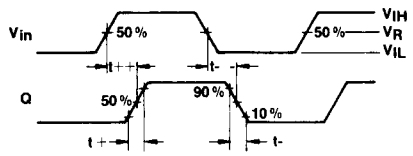
†Refer to Fig.4 for input pulse definitions.

*Complement of output under test should always be loaded with 50-ohms to ground.

Fig.3 Switching time test circuit at +25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V - INPUT TO OUTPUT

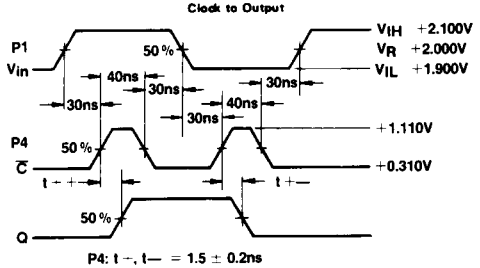


Test Pulses:
t+, t- = 1.5 ± 0.2ns (10% to 90%)
f = 5.0MHz
50% DUTY CYCLE
VIH IS APPLIED TO $\overline{C}$ DURING TESTS

TEST PULSE LEVELS

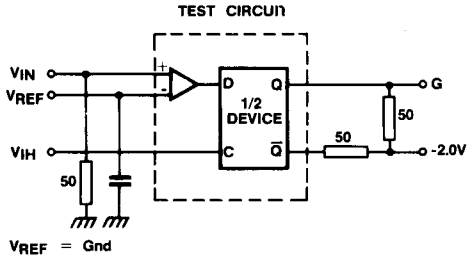
	Pulse 1	Pulse 2	Pulse 3
V_{IH}	+2.100V	+5.000V	-0.300V
V_R	+2.000V	+4.900V	-0.400V
V_{IL}	+1.900V	+4.800V	-0.500V

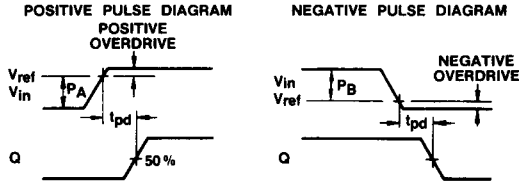
Clock to Output



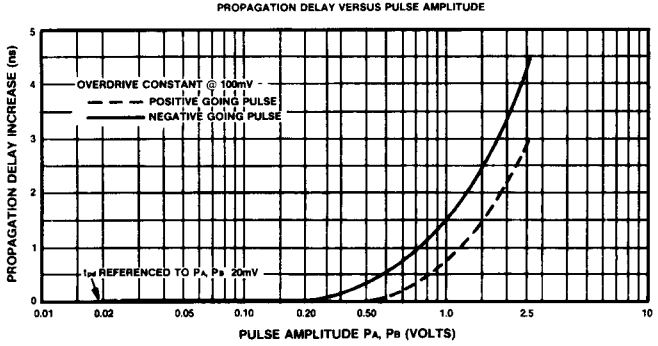
P4: t+-, t-+ = 1.5 ± 0.2ns

Fig.4 Switching and propagation waveforms @ 25°C





INPUT SWITCH TIME IS CONSTANT
AT 1.5ns (10% TO 90%).



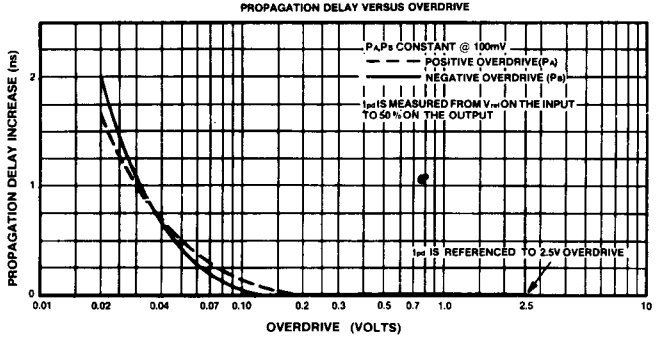


Fig.5 Propagation delay (tpd) v. input pulse amplitude and constant overdrive

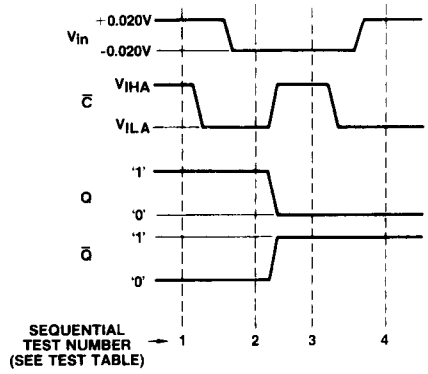
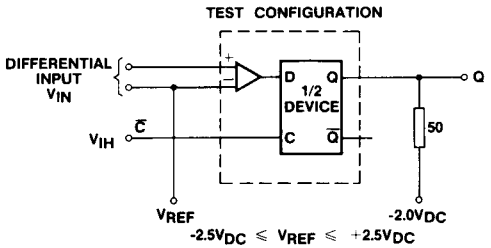


Fig.6 Logic threshold tests (waveform sequence diagram)



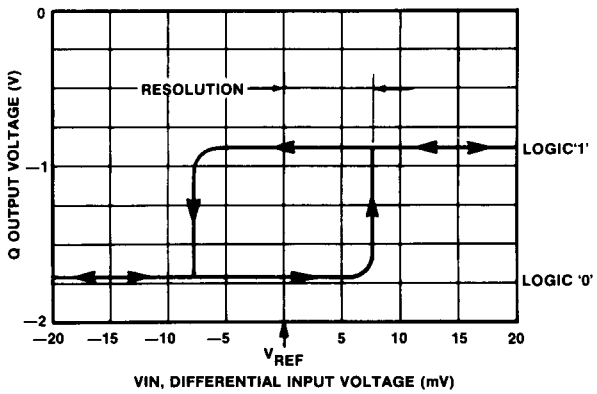


Fig.7 Transfer characteristics (Q v. Vin)

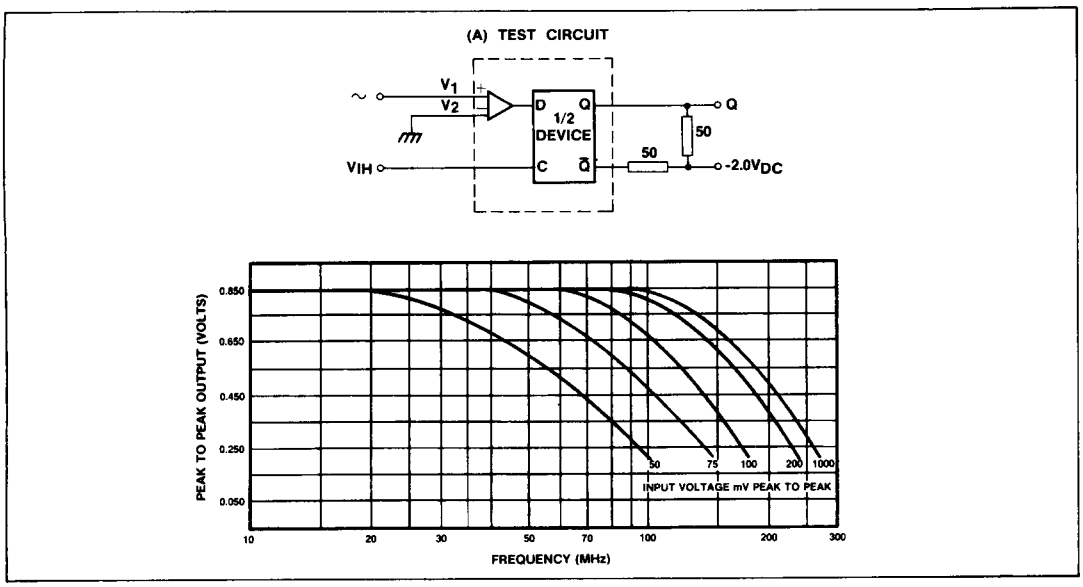


Fig.8 Output voltage swing v. frequency

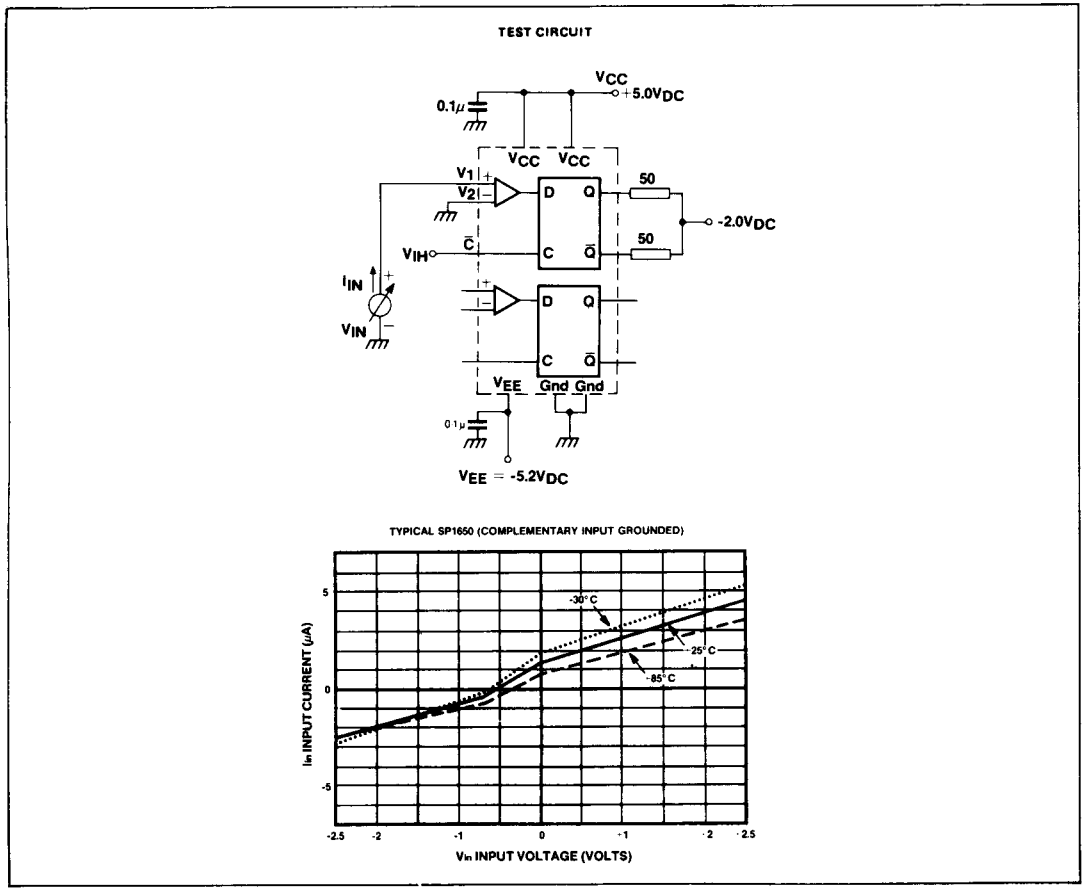
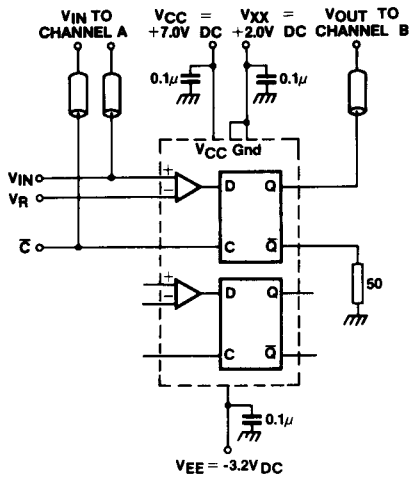


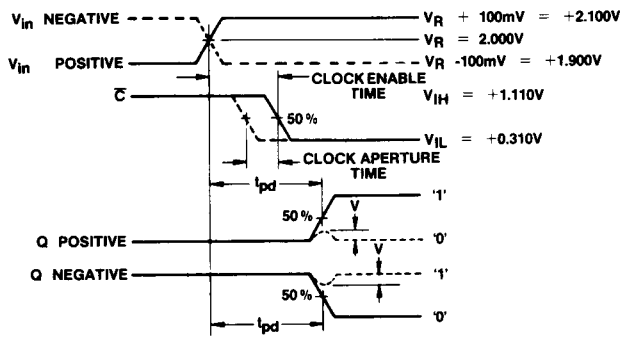
Fig.9 Input current v. input voltage



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

ANALOG SIGNAL POSITIVE AND NEGATIVE SLEW CASE



—— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200ps.

---- Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150mV.

Fig.10 Clock enable and aperture time test circuit and waveforms @ 25° C