MOTOROLA

MC68HC53

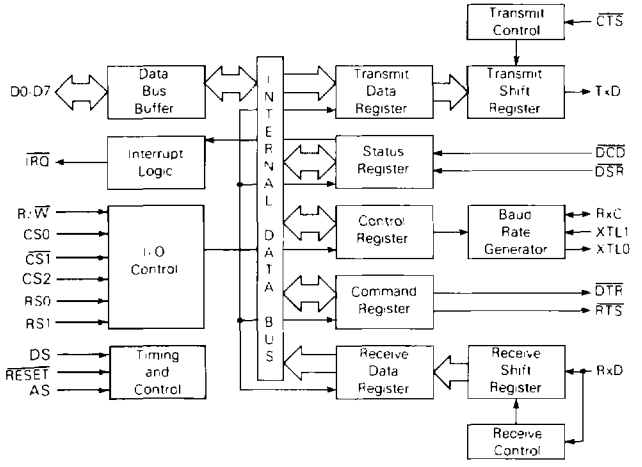
Product Preview

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

The MC68HC53 ACIA provides a program-controlled interface between 8-bit, microprocessor-based systems, serial communication data sets, and modems. An on-chip crystal oscillator and a baud-rate generator allow the ACIA to transmit at 15 different program-selected rates, ranging from 50 to 19,200 baud. The MC68HC53 can receive at either the transmit rate or at 16 times an external clock rate. A MOTEL (MOTorola - IntEL) bus compatible circuit, is incorporated in the MC68HC53. This circuit allows the device to directly interface with many types of microprocessors.

- Compatible With 8-Bit Microprocessors
- Full-Duplex or Half-Duplex Operation With Buffered Receiver and Transmitter
- Fifteen Programmable Baud Rates (50 to 19,200)
- Receiver Data Rate May Be Identical to Baud Rate or May Be 16 Times the External Clock Input
- Data Set/Modem Control Functions
- Programmable Word Lengths, Number of Stop Bits, and Parity Bit Generation and Detection
- Programmable Interrupt Control
- Software Reset
- Program-Selectable Serial Echo Mode
- Two Chip Selects
- 2 MHz or 1 MHz Clock Rate
- Single +5 Volt ±5% Power Supply
- Full TTL Compatibility
- MOTEL Read/Write Control Circuit

FIGURE 1 — BLOCK DIAGRAM



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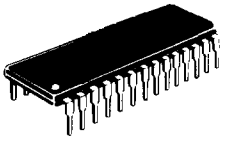
HCMOS

(HIGH DENSITY CMOS SILICON-GATE)

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT

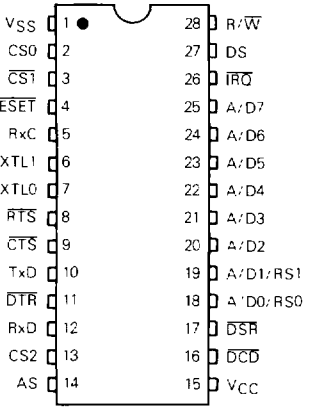
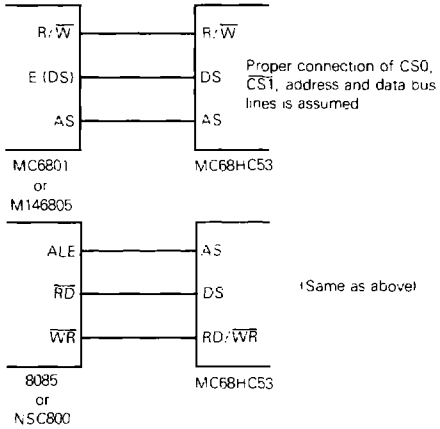


FIGURE 2 – INTERFACE REQUIREMENTS DIAGRAM



SIGNAL DESCRIPTIONS

The following paragraphs provide a brief description of the input and output signals for the MC68HC53

RESET (RESET)

During system initialization, a low on the RESET input clears the internal registers.

ADDRESS STROBE (AS)

Address strobe indicates the presence of an address on the multiplexed bus. The negative edge latches address/data lines 0-1 and chip select 2.

DATA STROBE (DS)

This input is used to transfer data to or from the microprocessor.

READ/WRITE (R/W)

The R/W is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/W pin allows the processor to read the data supplied by the ACIA. A low on the R/W pin allows a write to the ACIA.

INTERRUPT REQUEST (IRQ)

The IRQ pin is an interrupt output from the interrupt control logic. It permits several devices to be connected to the common IRQ microprocessor input. Normally a high level, IRQ goes low when an interrupt occurs

ADDRESS/DATA BUS (A/D0-A/D7)

The A/D0-A/D7 pins are the eight data lines used to transfer data and addresses These lines are bidirectional and are normally in the high-impedance state, except during read cycles when the ACIA is selected. D0 and D1 are dual-purpose register selects and data lines They are demultiplexed by AS as follows:

D1/RS1	D0/RS0	Write	Read
0	0	Transmit Data Register	Received Data Register
0	0	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

DATA SET READY (DSR)

The DSR input pin is used to indicate to the ACIA the status of the modem. A low indicates the "ready" state and a high "not-ready" DSR is a high-impedance input, and must be connected. If unused, it should be driven high or low but not switched

DATA CARRIER DETECT (DCD)

The DCD input pin is used to indicate to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high that it is not. Like DSR, DCD is a high-impedance input and must be connected.

REQUEST TO SEND (RTS)

The RTS output pin is used to control the modem from the processor. The state of the RTS pin is determined by the contents of the command register.

CLEAR TO SEND (CTS)

The CTS input pin is used to control the transmitter operation. The enable state is with CTS low The transmitter is automatically disabled if CTS is high.

DATA TERMINAL READY (DTR)

This output pin is used to indicate the status of the ACIA to the modem. A low on DTR indicates the ACIA is enabled and a high indicates it is disabled The processor controls this pin via bit 0 of the command register.

CHIP SELECTS 0, 1, AND 2 (CS0, CS1, AND CS2)

These three chip-select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high, CS1 is low, and CS2 is high CS2 is latched by AS.

CRYSTAL PINS (XTL1, XTL0)

These pins are normally directly connnected to the external crystal (1.8432 megahertz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTL1 pin in which case the XTL0 pin must float. XTL1 is the input pin for the transmit clock.

TRANSMIT DATA (TxD)

The TxD output line is used to transfer serial non-return-to-zero (NRZ) data to the modem. The least significant bit

(LSB) of the transmit data register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected, or under control of an external clock (as selected by the control register)

RECEIVE DATA (RxD)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock (as selected by the control register).

RECEIVE CLOCK (RxC)

The RxC is a bidirectional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud-rate generator is selected for receiver data clocking.

3

MOTEL CIRCUIT

The MOTEL circuit is a new concept that permits the MC68HC53 to be directly interfaced with many types of microprocessors. No external logic is needed to adapt to the differences in bus control signals from common multiplexed bus microprocessors.

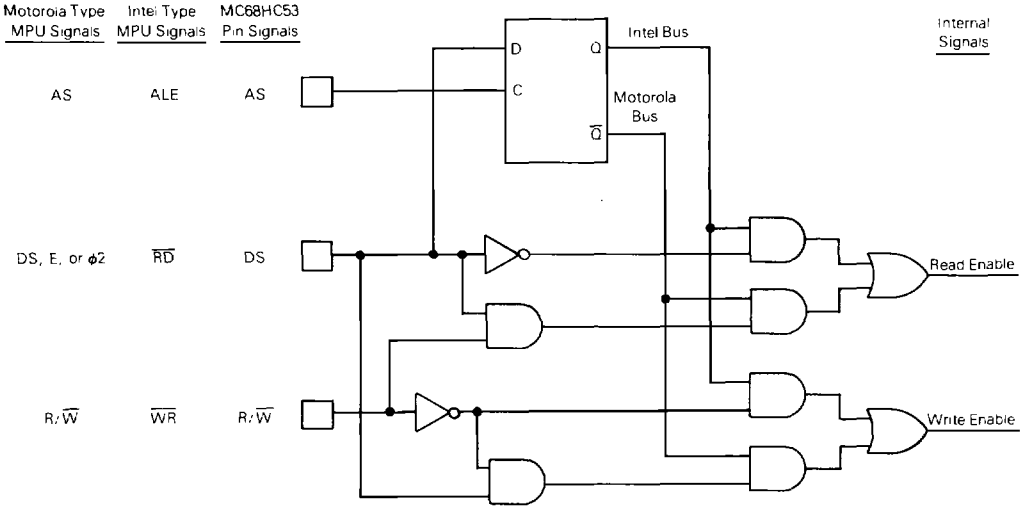
Practically all microprocessors interface with one of two synchronous bus structures. One bus was originated for the Motorola MC6800 and the other for the Intel 8080 and its companion part, the 8228.

The MOTEL circuit (for MOTorola and intEL bus compatibility) is built into a peripheral or memory IC to permit direct connection to either type of bus. An industry standard bus structure is now available. The MOTEL concept is shown logically in Figure 3.

MOTEL selects one of the two interpretations of two pins. In the Motorola case, DS and R/$\overline{W}$ are gated together to produce the internal read enable. The internal write enable is a similar gating of the inverse of R/$\overline{W}$. With competitor buses, the inversion of $\overline{RD}$ and $\overline{WR}$ create functionally identical internal read and write enable signals.

The MC68HC53 automatically selects the processor type by using AS/ALE to latch the state of the DS/$\overline{RD}$ pin. Since DS is always low and $\overline{RD}$ is always high during AS and ALE, the latch automatically indicates which processor type is connected.

FIGURE 3 — MOTEL CIRCUIT-LOGIC DIAGRAM



MAIN DATA/CONTROL REGISTERS

A brief description of the main MC68HC53 data and control registers follows.

TRANSMIT DATA REGISTER

This 8-bit register provides temporary storage for the data to be transmitted. Bit 0 is the leading bit to be transmitted. Unused bits are the high-order bits and are "don't care" for transmission.

RECEIVE DATA REGISTER

This 8-bit register provides temporary storage for the data being received. Bit 0 is the leading bit received. Unused bits are the high-order bits and are "zeros" for the receiver. Parity bits are not contained in the receive data register but are stripped off after being used for parity checking. Thus, former parity bits become unused "zero" bits in the receive data register.

COMMAND REGISTER

This 8-bit register contains the command word received from the controlling microprocessor. The command word specifies the specific modes and functions the MC68HC53 is to assume. Included are data terminal ready, transmitter interrupt disabled, receiver echo mode, and parity disabled.

CONTROL REGISTER

This 8-bit register contains, message format information received from the microprocessor, and includes: baud rate, clock source, word length, and number of stop bits. This information is used by the MC68HC53 for synchronization and proper processing of message data.

STATUS REGISTER

This 8-bit register contains the current status of the MC68HC53 and the related modem. This register is continuously accessed by the controlling microprocessor during operation to determine if data processing is being performed properly or if errors have occurred. Status indications include: parity error, framing error, overrun, clear to send, transmit register empty, receive register full, data carrier detect, and interrupt request.