

650 V Power SiC Gen 3 Merged PIN Schottky Diode, 16 A



FEATURES

- Majority carrier diode using Schottky technology on SiC wide band gap material
- Improved V_F and efficiency by thin wafer technology
- Positive V_F temperature coefficient for easy paralleling
- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- 175 °C maximum operating junction temperature
- MPS structure for high ruggedness to forward current surge events
- Meets JESD 201 class 1A whisker test
- Solder bath temperature 275 °C maximum, 10 s per JESD 22-B106
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

LINKS TO ADDITIONAL RESOURCES



3D Models



Application Notes

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	16 A
V_R	650 V
V_F at I_F at 150 °C	1.5 V
T_J max.	175 °C
I_R at V_R at 175 °C	6.5 μ A
Q_C ($V_R = 400$ V)	44 nC
Package	TO-220AC 2L
Circuit configuration	Single

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 650 V Schottky diode, designed for high performance and ruggedness.

Optimum choice for high speed hard switching and efficient operation over a wide temperature range, it is also recommended for all applications suffering from Silicon ultrafast recovery behavior.

Typical applications include AC/DC PFC and DC/DC ultra high frequency output rectification in FBPS and LLC converters.

MECHANICAL DATA

Case: TO-220AC 2L

Molding compound meets UL 94 V-0 flammability rating
Base P/N-M3 - halogen-free, RoHS-compliant

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

Mounting torque: 10 in-lbs maximum

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C unless otherwise specified)				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}		650	V
Average rectified forward current	$I_{F(AV)}$	$T_C = 123$ °C (DC)	16	A
DC blocking voltage	V_{DC}		650	V
Repetitive peak forward current	I_{FRM}	$T_C = 25$ °C, $f = 50$ Hz, square wave, DC = 25 %	60	A
Non-repetitive peak forward surge current	I_{FSM}	$T_C = 25$ °C, $t_p = 10$ ms, half sine wave	104	A
		$T_C = 110$ °C, $t_p = 10$ ms, half sine wave	95	
Power dissipation	$P_{tot}^{(1)}$	$T_C = 25$ °C	89	W
		$T_C = 110$ °C	39	
I^2t value	$\int i^2 dt$	$T_C = 25$ °C	54	A ² s
		$T_C = 110$ °C	46	
Operating junction and storage temperatures	$T_J^{(2)}, T_{Stg}$		-55 to +175	°C

Notes

(1) Based on maximum R_{th}

(2) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{thJA}$

**ELECTRICAL SPECIFICATIONS** ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward voltage	V_F	$I_F = 16\text{ A}$	-	1.3	1.5	V
		$I_F = 16\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$	-	1.50	1.80	
		$I_F = 16\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$	-	1.58	-	
Reverse leakage current	I_R	$V_R = V_R\text{ rated}$	-	1.0	85	μA
		$V_R = V_R\text{ rated}, T_J = 150\text{ }^{\circ}\text{C}$	-	4	200	
		$V_R = V_R\text{ rated}, T_J = 175\text{ }^{\circ}\text{C}$	-	6.5	-	
Total capacitance	C	$V_R = 1\text{ V}, f = 1\text{ MHz}$	-	700	-	pF
		$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	70	-	
Total capacitive charge	Q_C	$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	44	-	nC

THERMAL - MECHANICAL SPECIFICATIONS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Thermal resistance, junction-to-case	R_{thJC}		-	1.3	1.7	$^{\circ}\text{C/W}$
Marking device				3C16ET07T		

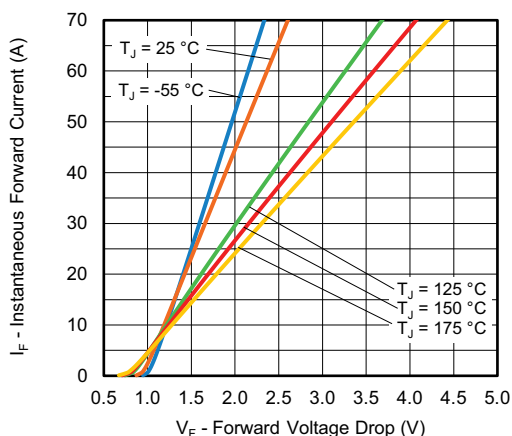


Fig. 1 - Typical Forward Voltage Drop Characteristics

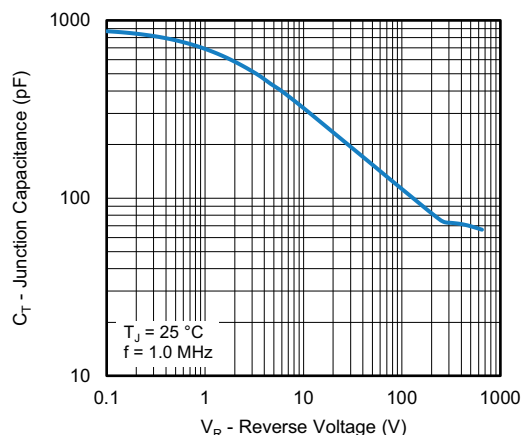


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

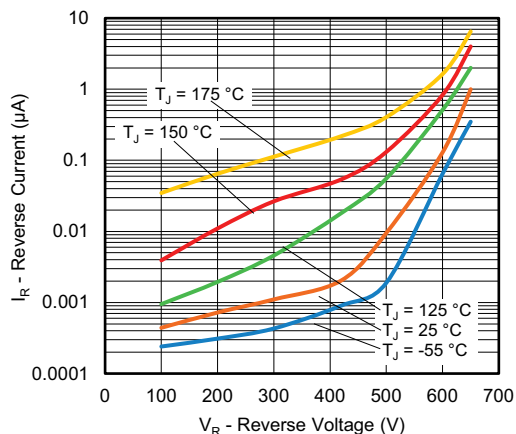


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

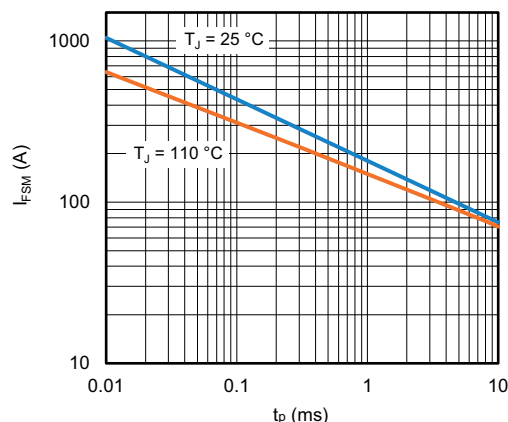


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration (Square Wave)

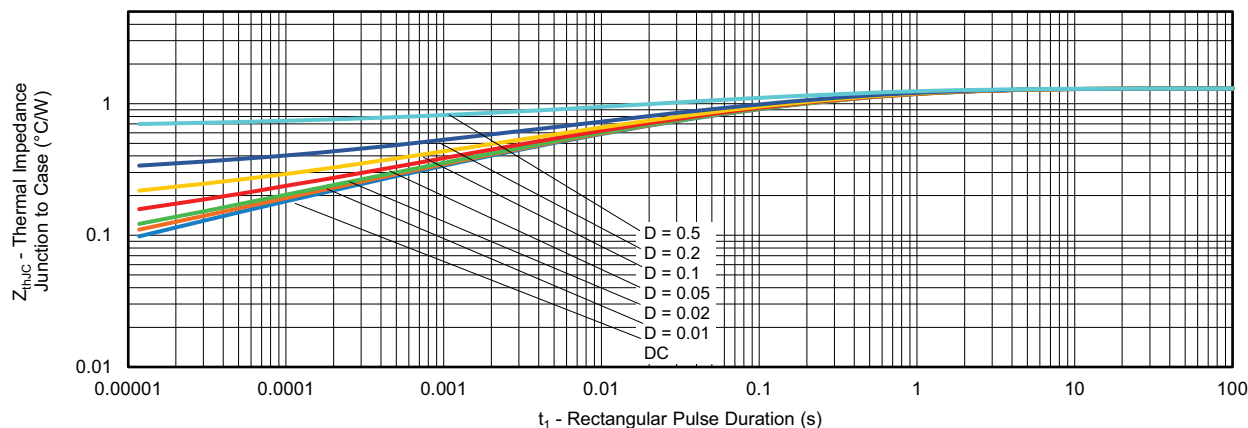
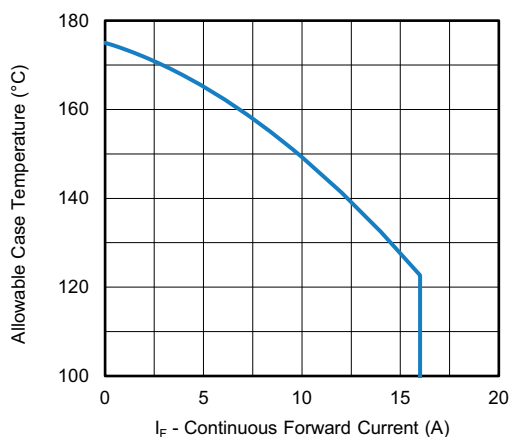

Fig. 5 - Typical Thermal Impedance Z_{thJC} Characteristics


Fig. 6 - Maximum Allowable Case Temperature vs. Average Forward Current

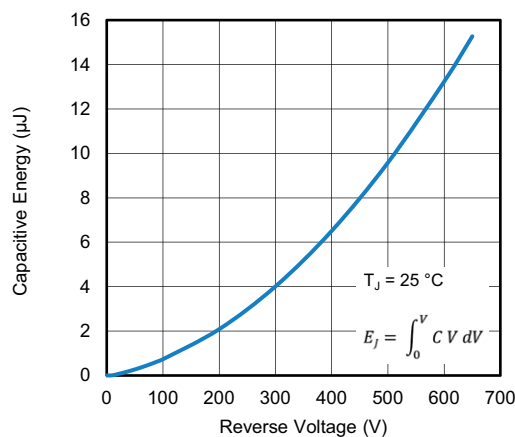


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage

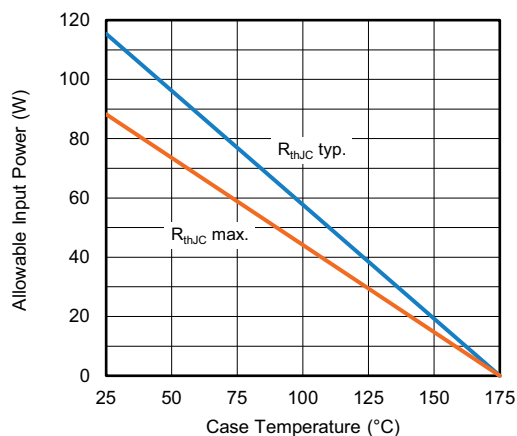


Fig. 7 - Forward Power Loss Characteristics

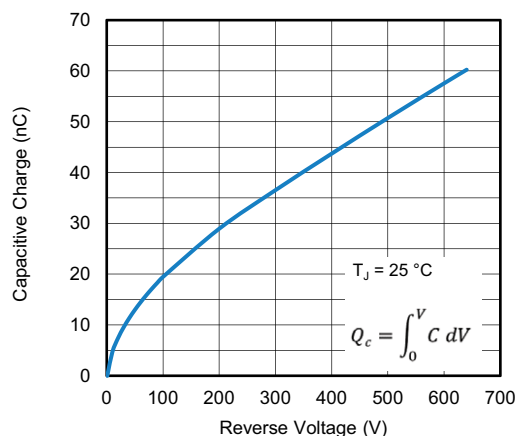


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage



ORDERING INFORMATION TABLE

Device code	VS-	3C	16	E	T	07	T	-M3
	1	2	3	4	5	6	7	8
1	Vishay Semiconductors product							
2	3C = SiC diode, Generation 3							
3	Current rating (16 = 16 A)							
4	E = single diode							
5	Package TO-220							
6	Voltage rating: (07 = 650 V)							
7	T = true 2 pin							
8	Environmental digit: -M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free							

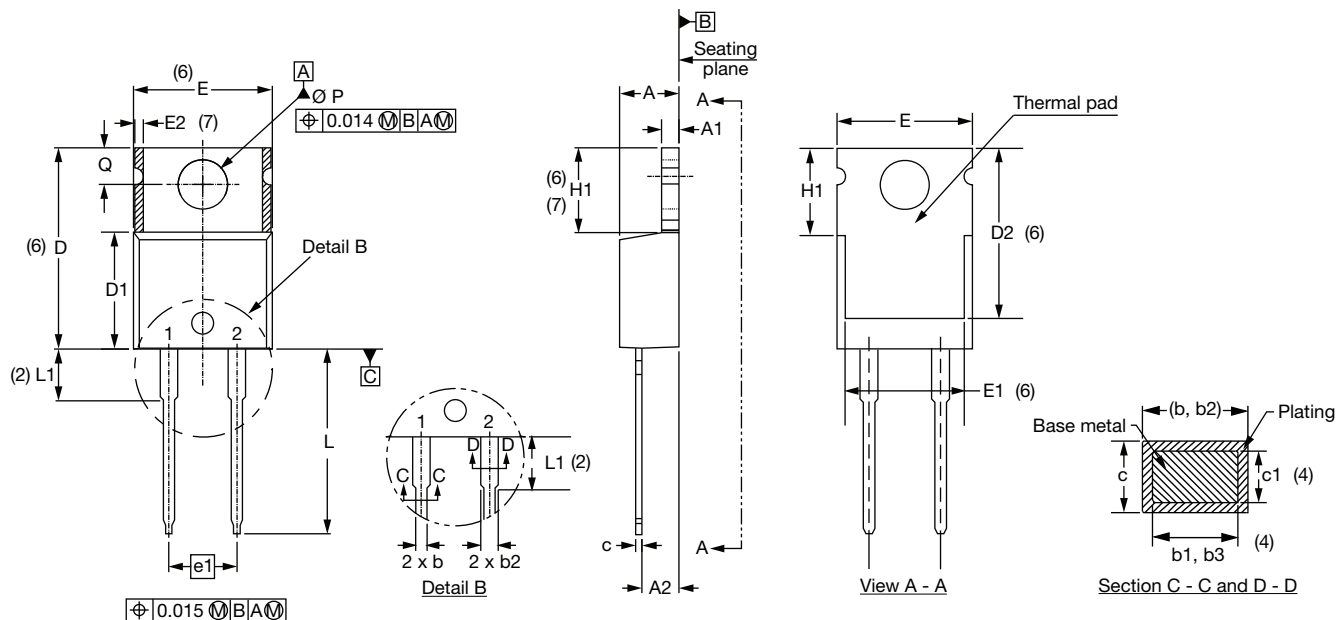
ORDERING INFORMATION		
PREFERRED P/N	BASE QUANTITY	PACKAGING DESCRIPTION
VS-3C16ET07T-M3	50/tube	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?96069
Part marking information	www.vishay.com/doc?95391



TO-220AC 2L

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
E	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e1	4.88	5.28	0.192	0.208	
H1	5.84	6.86	0.230	0.270	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC® TO-220, except D2, where JEDEC® minimum is 0.480"



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