

# MH25609J-85,-10,-12,-15/ MH25609JA-85,-10,-12,-15

PAGE MODE 262144-WORD BY 9-BIT DYNAMIC RAM

## DESCRIPTION

The MH25609J, JA is 262144 word x 9 bit dynamic RAM and consists of nine industry standard 256K x 1 dynamic RAMs in plastic leaded chip carrier.

The mounting of plastic leaded chip carrier on a single in-line package provides any application where high densities and large quantities of memory are required.

MH25609JA is a leaded type-memory module, allowing direct insertion to normal through-hole-board like DIP devices.

MH25609J is a socket type-memory module, suitable for easy interchanging or addition of modules.

## FEATURES

- High-speed

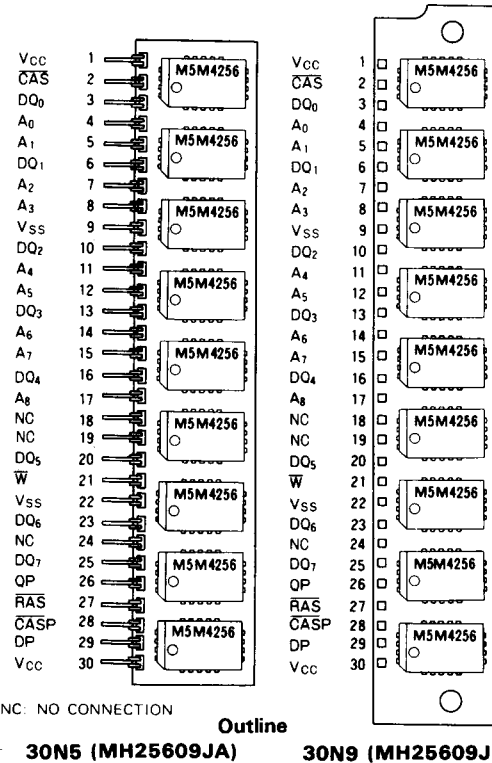
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH25609J-85 MH25609JA-85	85	160	2700
MH25609J-10 MH25609JA-10	100	190	2340
MH25609J-12 MH25609JA-12	120	220	2070
MH25609J-15 MH25609JA-15	150	260	1800

- Utilizes industry standard 256K RAMs in plastic leaded carriers
- 30 pins Single In-line Package
- Single +5V ( $\pm 10\%$ ) supply operation
- Low standby power dissipation 225mW (max)
- Low operation power dissipation.
  - MH25609J-85/MH25609JA-85 . . . . . 3.47W (max)
  - MH25609J-10/MH25609JA-10 . . . . . 3.24W (max)
  - MH25609J-12/MH25609JA-12 . . . . . 2.97W (max)
  - MH25609J-15/MH25609JA-15 . . . . . 2.75W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.15 $\mu$ F x 9) decoupling capacitors
- 256 refresh cycles every 4ms, A<sub>8</sub> Pin is not need for refresh
- Common  $\overline{\text{CAS}}$  control for eight common Data-In and Data-Out lines.
- Separate  $\overline{\text{CAS}}$  ( $\overline{\text{CASP}}$ ) control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operation to prevent contention on Data-In and Data-Out.
- Bit nine (DP, QP) controlled by  $\overline{\text{CASP}}$  is generally used for parity.

## APPLICATION

Main memory unit for computers, Microcomputer memory

## PIN CONFIGURATION (TOP VIEW)



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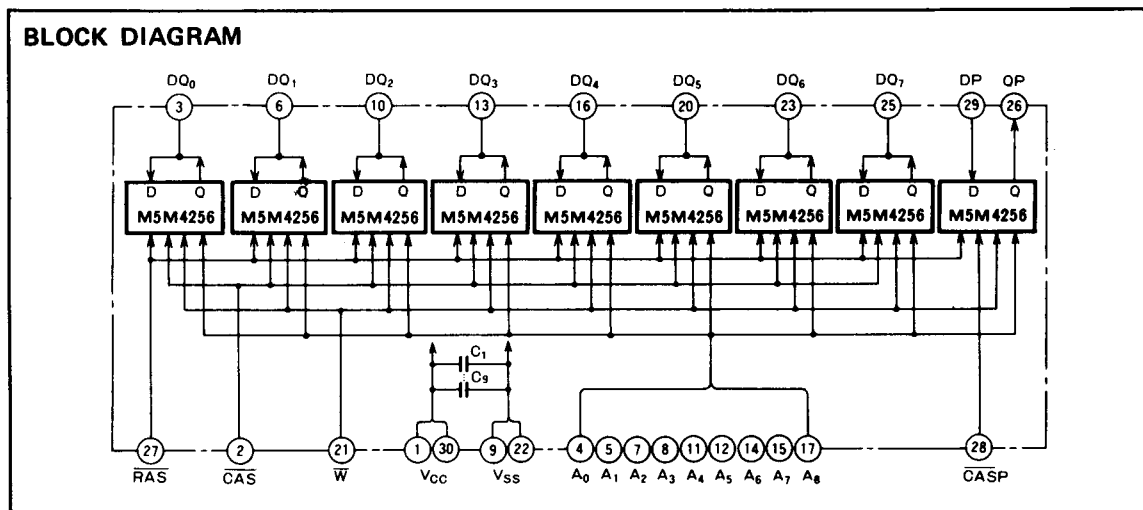
### FUNCTION

The MH25609J, JA provides, in addition to normal read and early write operations, a number of other functions, e.g., page mode, RAS-only refresh, hidden refresh and  $\overline{\text{CAS}}$  before RAS refresh. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

Operation	Inputs						Output	Refresh
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	D	Row address	Column address	Q	
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES
Early write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES
$\overline{\text{CAS}}$ before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	With respect to V <sub>SS</sub>	-1~7	V
V <sub>I</sub>	Input voltage		-1~7	V
V <sub>O</sub>	Output voltage		-1~7	V
I <sub>O</sub>	Output current	T <sub>a</sub> = 25°C	50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	9	W
T <sub>opr</sub>	Operating temperature		0~70	°C
T <sub>stg</sub>	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = 0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>SS</sub>	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	2.4		6.5	V
V <sub>IL</sub>	Low-level input voltage all inputs	-2		0.8	V

Note 1 All voltage values are with respect to V<sub>SS</sub>.

ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5mA	2.4		V <sub>CC</sub>	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2mA	0		0.4	V
I <sub>OZ</sub>	Off-state output current	Q floating 0V ≤ V <sub>OUT</sub> ≤ 5.5V	-20		20	μA
I <sub>I</sub>	Input current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> . Other input pins = 0V	-90		90	μA
I <sub>CC1</sub> (AV)	Average supply current from V <sub>CC</sub> , operating (Note 3, 4)	MH25609-85			630	mA
		MH25609-10	RAS, CAS cycling		585	
		MH25609-12	t <sub>CR</sub> = t <sub>CW</sub> = min, output open		540	
		MH25609-15			495	
I <sub>CC2</sub>	Supply current from V <sub>CC</sub> , standby	RAS = CAS = V <sub>IH</sub> output open			40.5	mA
I <sub>CC3</sub> (AV)	Average supply current from V <sub>CC</sub> , refreshing (Note 3)	MH25609-85			540	mA
		MH25609-10	RAS cycling CAS = V <sub>IH</sub>		495	
		MH25609-12	t <sub>C</sub> (RAS) = min, output open		450	
		MH25609-15			405	
I <sub>CC4</sub> (AV)	Average supply current from V <sub>CC</sub> , page mode (Note 3, 4)	MH25609-85			495	mA
		MH25609-10	RAS = V <sub>IL</sub> , CAS cycling		450	
		MH25609-12	t <sub>CPG</sub> = min, output open		405	
		MH25609-15			360	
I <sub>CC6</sub> (AV)	Average supply current from V <sub>CC</sub> , automatic refreshing (Note 3)	MH25609-85			585	mA
		MH25609-10	CAS before RAS refresh cycling		540	
		MH25609-12	t <sub>O</sub> (RAS) = min, output open		495	
		MH25609-15			450	
C <sub>I</sub> (A)	Input capacitance, address inputs				60	pF
C <sub>I</sub> (DO)	Data input/data output capacitance				17	pF
C <sub>I</sub> (W)	Input capacitance, write control input	V <sub>I</sub> = V <sub>SS</sub>			75	pF
C <sub>I</sub> (RAS)	Input capacitance, RAS input	f = 1MHz			75	pF
C <sub>I</sub> (CAS)	Input capacitance, CAS input	V <sub>I</sub> = 25mVrms			70	pF
C <sub>I</sub> (CASP)	Input capacitance, CASP input				13	pF
C <sub>I</sub> (OP)	Input capacitance				17	pF
C <sub>O</sub> (QP)	Output capacitance	V <sub>O</sub> = V <sub>SS</sub> , f = 1MHz, V <sub>I</sub> = 25mVrms			12	pF

Note 2. Current flowing into an IC is positive, out is negative.

3. I<sub>CC1</sub>(AV), I<sub>CC3</sub>(AV), I<sub>CC4</sub>(AV) and I<sub>CC6</sub>(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4. I<sub>CC1</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on output loading. Specified values are obtained with the output open.

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## TIMING REQUIREMENTS (For Read, Early Write, Refresh, and Page-Mode Cycle)

(Ta = 0 ~ 70°C, VCC = -5V ± 10%, VSS = 0V, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>CRF</sub>	Refresh cycle time	t <sub>REF</sub>		4		4		4		4	ms
t <sub>W(RASH)</sub>	RAS high pulse width	t <sub>RP</sub>	65		80		90		100		ns
t <sub>W(RASL)</sub>	RAS low pulse width	t <sub>RAS</sub>	85	10000	100	10000	120	10000	150	10000	ns
t <sub>W(CASL)</sub>	CAS low pulse width	t <sub>CAS</sub>	45	10000	50	10000	60	10000	75	10000	ns
t <sub>W(CASH)</sub>	CAS high pulse width (Note 8)	t <sub>CPN</sub>	20		20		25		25		ns
t <sub>h(RAS-CAS)</sub>	CAS hold time after RAS	t <sub>CSH</sub>	85		100		120		150		ns
t <sub>h(CAS-RAS)</sub>	RAS hold time after CAS	t <sub>RSH</sub>	45		50		60		75		ns
t <sub>d(CAS-RAS)</sub>	Delay time, CAS to RAS (Note 9)	t <sub>CRP</sub>	10		10		10		10		ns
t <sub>d(RAS-CAS)</sub>	Delay time, RAS to CAS (Note 10)	t <sub>RCD</sub>	15	40	15	50	20	60	25	75	ns
t <sub>SU(RA-RAS)</sub>	Row address setup time before RAS	t <sub>ASR</sub>	0		0		0		0		ns
t <sub>SU(CA-CAS)</sub>	Column address setup time before CAS	t <sub>ASC</sub>	-5		-5		-5		-5		ns
t <sub>h(RAS-RA)</sub>	Row address hold time after RAS	t <sub>RAH</sub>	10		10		15		20		ns
t <sub>h(CAS-CA)</sub>	Column address hold time after CAS	t <sub>CAH</sub>	15		15		20		25		ns
t <sub>h(RAS-CA)</sub>	Column address hold time after RAS	t <sub>CAH</sub>	55		65		80		100		ns
t <sub>THL</sub>	Transition time	t <sub>T</sub>	3	50	3	50	3	50	3	50	ns
t <sub>TLH</sub>			3	50	3	50	3	50	3	50	ns

Note 5. An initial pause of 500μs is required after power-up followed by any eight RAS or RAS/CAS cycles before proper device operation is achieved.

6. The switching characteristics are defined at t<sub>THL</sub> = t<sub>TLH</sub> = 5ns.7. Reference levels of input signals are V<sub>IH min</sub> and V<sub>IL max</sub>. Reference levels for transition time are also between V<sub>IH</sub> and V<sub>IL</sub>.

8. Except for page-mode.

9. t<sub>d(CAS-RAS)</sub> requirement is only applicable for all RAS/CAS cycles.10. Operation within the t<sub>d(RAS-CAS)</sub> max limit insures that t<sub>d(RAS)</sub> max can be met, t<sub>d(RAS-CAS)</sub> max is specified reference point only; ift<sub>d(RAS-CAS)</sub> is greater than the specified t<sub>d(RAS-CAS)</sub> max limit, then access time is controlled exclusively by t<sub>d(CAS)</sub>.t<sub>d(RAS-CAS)</sub> min = t<sub>h(RAS-RA)</sub> min + 2t<sub>THL</sub>(t<sub>THL</sub>) + t<sub>SU(CA-CAS)</sub> min.

## SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted)

## Read Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>CR</sub>	Read cycle time	t <sub>RC</sub>	160		190		220		260		ns
t <sub>SU(R-CAS)</sub>	Read setup time before CAS	t <sub>RCS</sub>	0		0		0		0		ns
t <sub>h(CAS-R)</sub>	Read hold time after CAS (Note 11)	t <sub>RCH</sub>	0		0		0		0		ns
t <sub>h(RAS-R)</sub>	Read hold time after RAS (Note 11)	t <sub>RRH</sub>	10		10		10		10		ns
t <sub>dIS(CAS)</sub>	Output disable time (Note 12)	t <sub>OFF</sub>	0	20	0	25	0	30	0	35	ns
t <sub>a(CAS)</sub>	CAS access time (Note 13)	t <sub>CAC</sub>		45		50		60		75	ns
t <sub>a(RAS)</sub>	RAS access time (Note 14)	t <sub>RAC</sub>		85		100		120		150	ns

Note 11. Either t<sub>h(RAS-R)</sub> or t<sub>h(CAS-R)</sub> must be satisfied for a read cycle.12. t<sub>dIS(CAS)</sub> max defines the time at which the output achieves the open circuit condition and is not reference to V<sub>OH</sub> or V<sub>OL</sub>.13. This is the value when t<sub>d(RAS-CAS)</sub> ≥ t<sub>d(RAS-CAS)</sub> max. Test conditions; Load = 2TTL, C<sub>L</sub> = 100pF.14. This is the value when t<sub>d(RAS-CAS)</sub> < t<sub>d(RAS-CAS)</sub> max. When t<sub>d(RAS-CAS)</sub> ≥ t<sub>d(RAS-CAS)</sub> max, t<sub>a(RAS)</sub> will increase by the amount that t<sub>d(RAS-CAS)</sub> exceeds the value shown. Test conditions; Load = 2TTL, C<sub>L</sub> = 100pF.

## Write Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>QW</sub>	Write cycle time	t <sub>RC</sub>	160		190		220		260		ns
t <sub>SU(W-CAS)</sub>	Write setup time before CAS (Note 15)	t <sub>WCS</sub>	-10		-10		-10		-10		ns
t <sub>h(CAS-W)</sub>	Write hold time after CAS	t <sub>WCH</sub>	15		20		25		30		ns
t <sub>h(RAS-W)</sub>	Write hold time after RAS	t <sub>WCR</sub>	55		70		85		105		ns
t <sub>h(W-RAS)</sub>	RAS hold time after write	t <sub>RWL</sub>	30		35		40		45		ns
t <sub>h(W-CAS)</sub>	CAS hold time after write	t <sub>CWL</sub>	30		35		40		45		ns
t <sub>W(W)</sub>	Write pulse width	t <sub>WP</sub>	15		20		25		30		ns
t <sub>SU(D-CAS)</sub>	Data-in setup time before CAS	t <sub>DS</sub>	0		0		0		0		ns
t <sub>h(CAS-D)</sub>	Data-in hold time after CAS	t <sub>DH</sub>	15		20		25		30		ns
t <sub>h(RAS-D)</sub>	Data-in hold time after RAS	t <sub>DHR</sub>	55		70		85		105		ns

Note 15. When t<sub>SU(W-CAS)</sub> < t<sub>SU(W-CAS)</sub> min, Data input will contend with the data output because of the common I/O feature.

# MH25609J-85, -10, -12, -15/ MH25609JA-85, -10, -12, -15

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### Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CPG}$	Page-mode cycle time	$t_{PC}$	80		100		120		145		ns
$t_{W(CASH)}$	CAS high pulse width	$t_{CP}$	25		40		50		60		ns
$t_{CPGRW}$	Page-mode read-write cycle time	—	105		130		155		180		ns

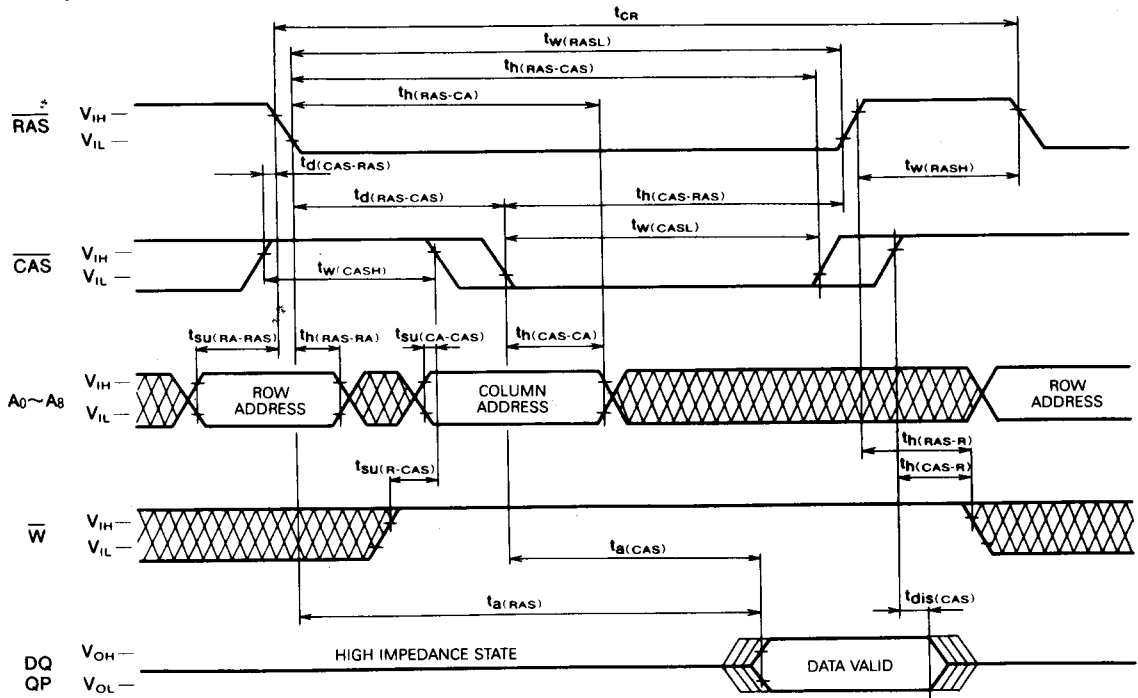
### CAS before RAS Refresh Cycle (Note 16)

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{SUR(CAS-RAS)}$	CAS setup time for auto refresh	$t_{OSR}$	10		10		10		10		ns
$t_{HR(RAS-CAS)}$	CAS hold time for auto refresh	$t_{CHR}$	15		20		25		30		ns
$t_{dR(RAS-CAS)}$	Precharge to CAS active time	$t_{RPC}$	0		0		0		0		ns

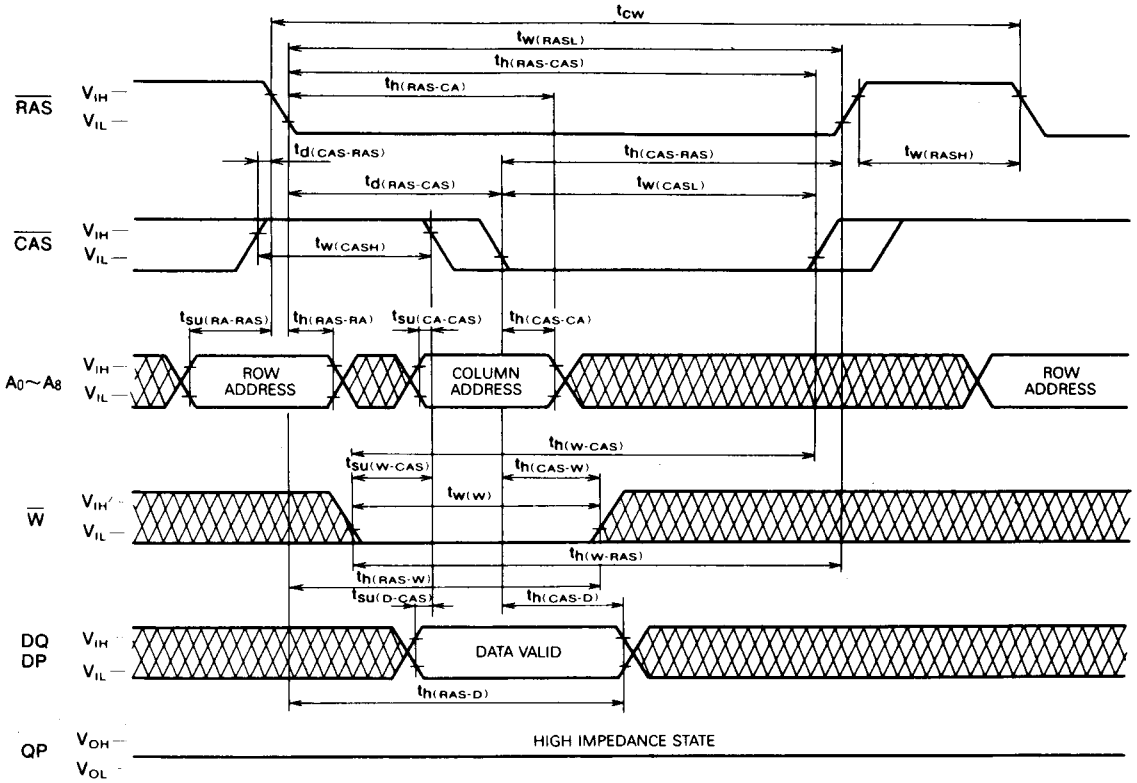
Note 16. Eight or more CAS before RAS cycles is necessary for proper operation of CAS before RAS refresh mode.

### TIMING DIAGRAMS (Note 17)

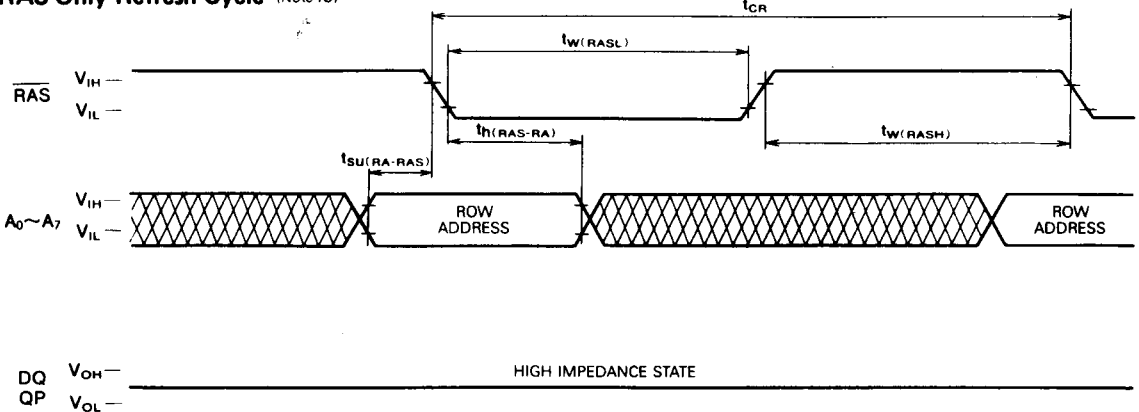
#### Read Cycle



**Early Write Cycle**



**RAS-Only Refresh Cycle (Note 18)**

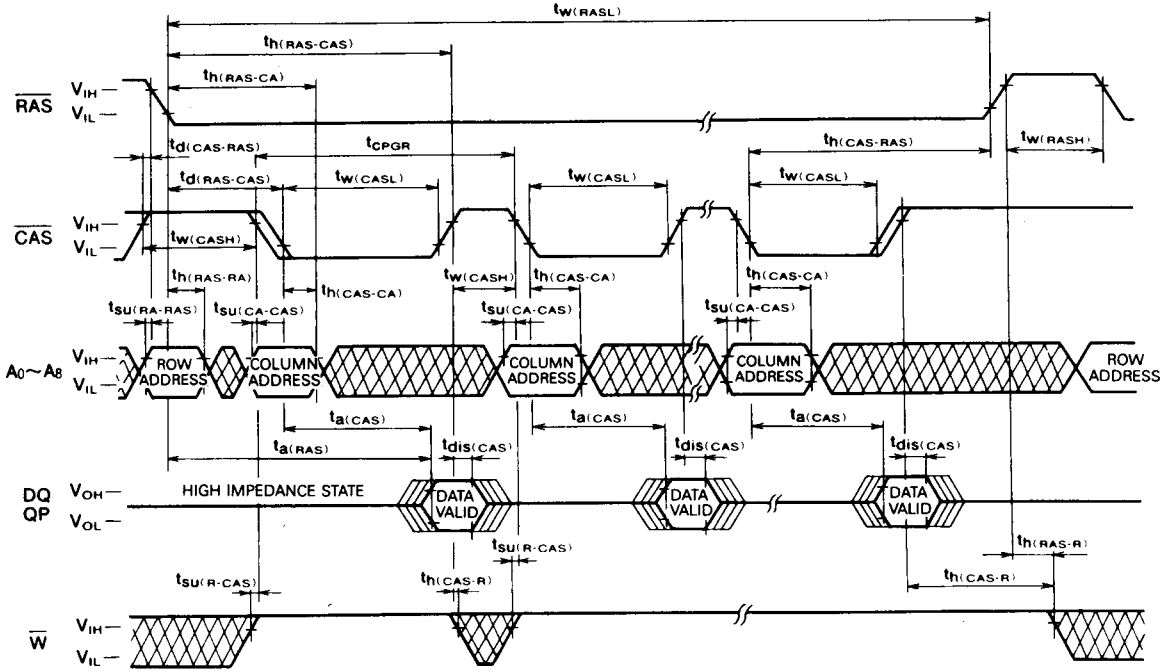


Note 17.  Indicates the don't care input.

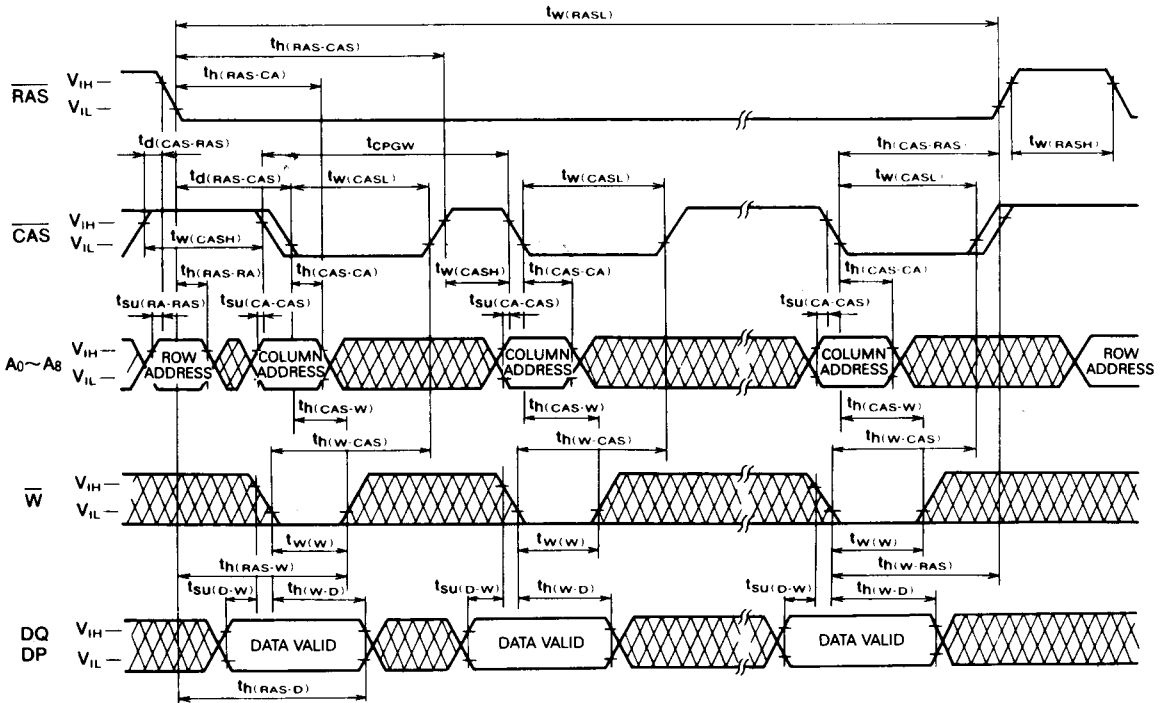
 The center-line indicates the high-impedance state.

Note 18.  $\overline{\text{CAS}} = V_{IH}$ ,  $\overline{\text{W}}$ ,  $\text{D} = \text{don't care}$ .  
A8 may be  $V_{IH}$  or  $V_{IL}$ .

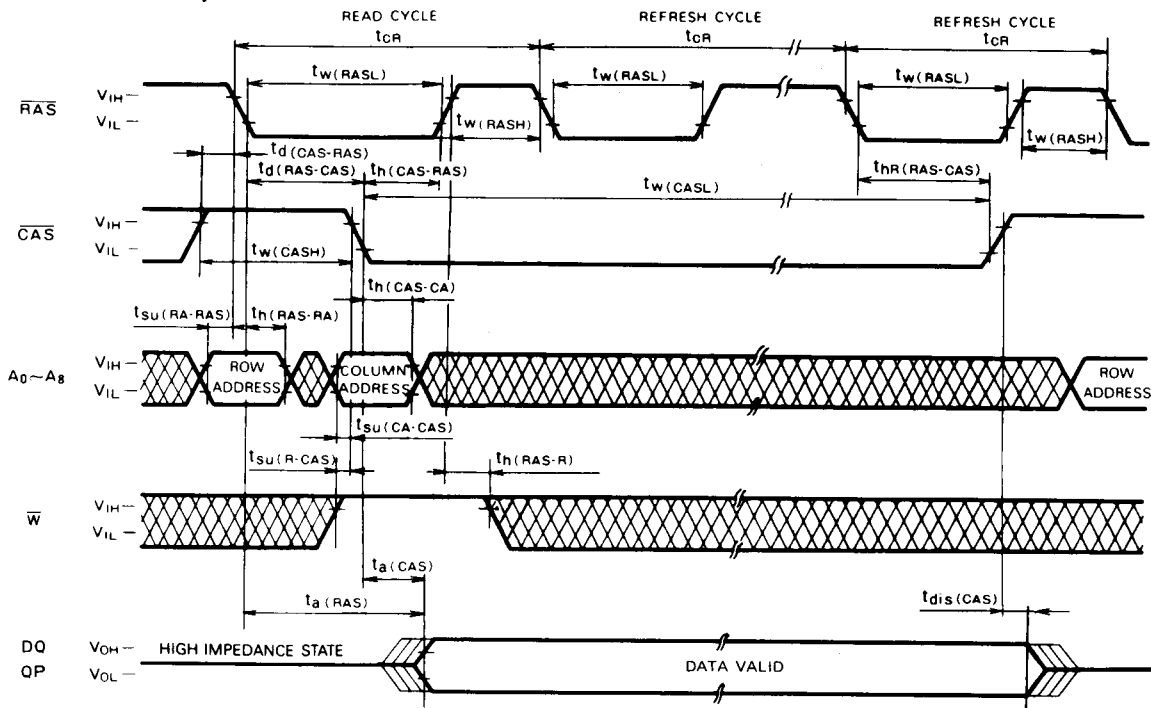
Page-Mode Read Cycle



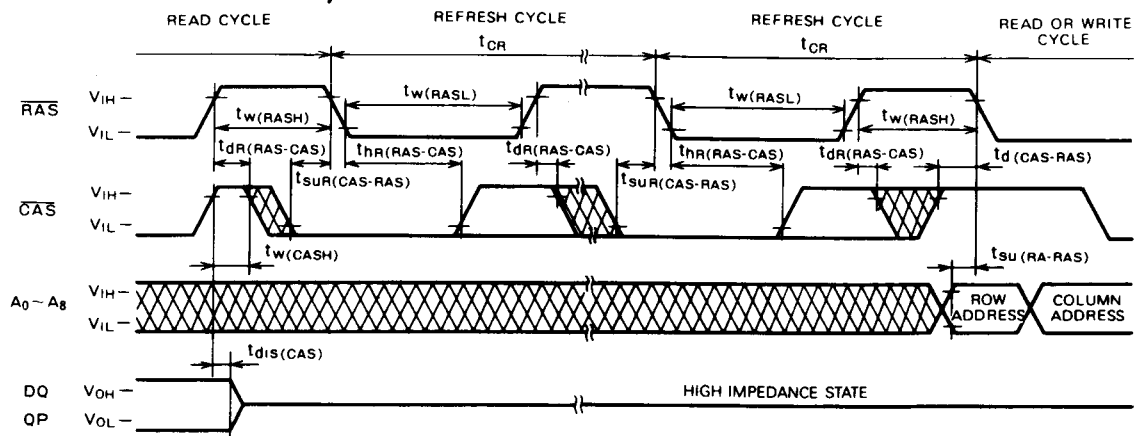
Page-Mode Write Cycle



**Hidden Refresh Cycle**



**CAS before RAS Refresh Cycle** (Note 19)



Note 19:  $\bar{W}$ , D = don't care.