SP720MD-8, SP720MD, SP720MM-8, SP720MM

High Reliability Electronic Protection Array for ESD and Overvoltage Protection

February 1998

Features

- The SP720MD-8 and SP720MM-8 are Harris Class B "Equivalent" Parts with Back-End Conformance to MIL-STD-883 for Final Assembly, Electrical Testing, Burn-In and QC Inspection
- ESD Interface Capability for HBM Standards
  - Modified MIL STD 3015.7 . . . . . 15kV
  - MIL STD 3015.7 . . . . . 6kV
  - IEC 1000-4-2, Direct Discharge,
    Single Input . . . . . 4kV (Level 2)
    Two Inputs in Parallel . . . . . 8kV (Level 4)
  - IEC 1000-4-2, Air Discharge . . . . . 15kV (Level 4)
- High Peak Current Capability
  - IEC 1000-4-5 . . . . . +3A
  - Single Pulse, 100µs Pulse Width . . . . . ±2A
  - Single Pulse, 4µs Pulse Width . . . . . ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to . . . . . +30V
  - Differential Voltage Range to . . . . . ±15V
- Fast Switching . . . . . 2ns Risetime
- Low Input Leakages . . . . . 1nA at 25°C Typical
- Low Input Capacitance . . . . . 3pF Typical
- An Array of 14 SCR/Diode Pairs
- Military Temperature Range . . . . . -55°C to 125°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP720 is a High Reliability Array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures at each IN input. A total of 14 available IN inputs can be used to protect up to 14 external signal or bus lines. Over voltage protection is from the IN to V+ or V-. The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ or at a $-V_{BE}$ diode threshold below V-. From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

The SP720MD-8 and SP720MM-8 Class B "Equivalent" Parts conform to MIL-STD-883 through final assembly, electrical test, burn-in and QC Inspection. The SP720MD and SP720MM are High Reliability Ceramic Packaged ICs.

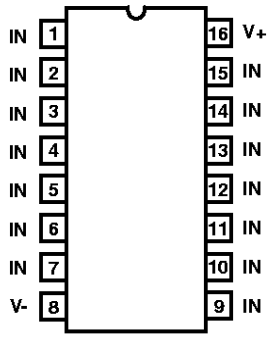
Refer to Application Note AN9304 for general application information and to AN9612 for further information on ESD and transient rating capabilities of the SP720.

Ordering Information

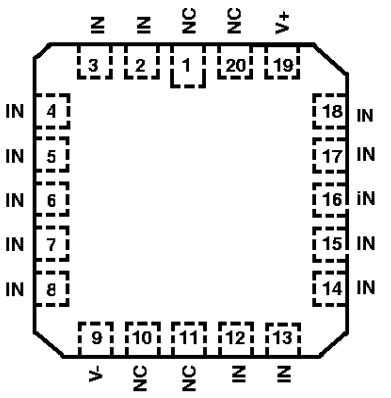
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
SP720MD-8	-55 to 125	16 Ld SBDIP	D16.3
SP720MD	-55 to 125	16 Ld SBDIP	D16.3
SP720MM-8	-55 to 125	20 Pad CLCC	J20.A
SP720MM	-55 to 125	20 Pad CLCC	J20.A

Pinouts

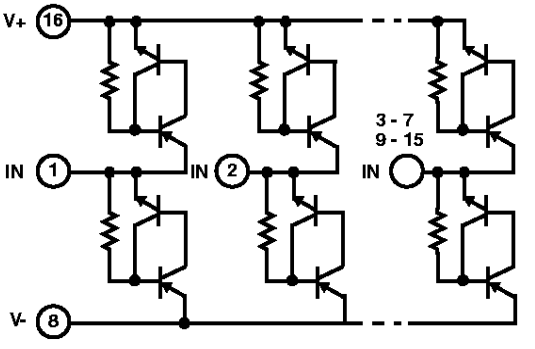
SP720MD (SBDIP)
TOP VIEW



SP720MM (CLCC)
TOP VIEW



Functional Block Diagram (SP720MD)



NOTE: The design of the SP720MD-8, SP720MD, SP720MM-8, and SP720MM SCR/Diode ESD Diode Protection Arrays is covered by Harris patent 4567500.

File Number **3683.6**

Absolute Maximum Ratings

Continuous Supply Voltage, [(V+) - (V-)]. . . . . +35V
Max. DC Input Current, I_{IN} . . . . . ±70mA
Input Peak Current, I_{IN} (Refer to Figure 3). . . . . ±2A, 100µs
ESD Capability, Refer to "ESD Capability" and Table 1, Figure 1

Operating Conditions

Operating Voltage Range, Single Supply . . . . . +2V to +30V
Operating Voltage Range, Split Supply . . . . . ±1V to ±15V
Typical Quiescent Supply Current 50nA
Operating Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld SBDIP Package	80	18
20 Pad CLCC Package	70	16

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 175°C
Maximum Lead Temperature (Soldering 10s) . . . . . 265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

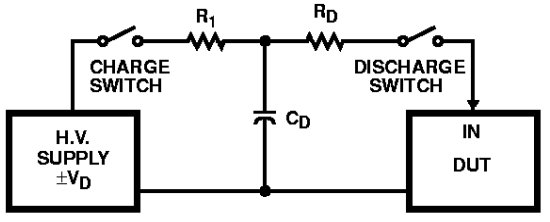
Electrical Specifications

T_A = -55°C to 125°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{SUPPLY}	V_{SUPPLY} = [(V+) - (V-)]	0	2 to 30	35	V
Peak Forward/Reverse Voltage Drop						
IN to V- (with V- Reference)	V_{IN} - (V-)	I_{IN} = -1A (1ms Peak Pulse)	-	-2	-	V
IN to V+ (with V+ Reference)	V_{IN} - (V+)	I_{IN} = +1A (1ms Peak Pulse)	-	+2	-	V
DC Forward/Reverse Voltage Drop						
IN to V- (with V- Reference)	V_{IN} - (V-)	I_{IN} = -100mA to V-	-1.5	-	-	V
IN to V+ (with V+ Reference)	V_{IN} - (V+)	I_{IN} = +100mA to V+	-	-	+1.5	V
Input Leakage Current	I_{IN}	V- < V_{IN} < V+, V_{SUPPLY} = 30V	-15	5	+15	nA
Quiescent Supply Current	$I_{QUIESCENT}$	V- < V_{IN} < V+, V_{SUPPLY} = 30V	-	50	150	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} (Note 3)	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.



IEC 1000-4-2: R_1 50 to 100MΩ
MIL STD 3015.7: R_1 1 to 10MΩ

FIGURE 1. ELECTROSTATIC DISCHARGE TEST

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	±V_D
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 1000-4-2	HBM, air discharge	330Ω	150pF	15kV (Level 4)
	HBM, direct discharge	330Ω	150pF	4kV (Level 2)
	HBM, direct discharge, two parallel input pins	330Ω	150pF	8kV (Level 4)
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP720 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 1000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP720 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

Peak Transient Current Capability

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP720's ability to withstand a wide range of transient current pulses.

The test circuit shown in Figure 2 provides a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e. It is not tied to the ground reference of the current pulse generator.) Figure 3 shows the point of over-stress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the V+ to V- voltage supply level, improving as the supply voltage is reduced. Values of 0, 5, 15 and 30 voltages are shown. The safe operating range of the transient peak current should be limited to no more than 75% of the measured over-stress level for any given pulse width as shown in Figure 3.

When adjacent input pins are paralleled, the sustained peak current capability is increased to nearly twice that of a single pin. For comparison, tests were run using dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15. The over-stress curve is shown in Figure 3 for a 15V supply condition. The dual pins are capable of 10A peak current for a 10µs pulse and 4A peak current for a 1ms pulse. The complete curve for single pulse peak current vs. pulse width time ranging up to 1 second is shown in Figure 3.

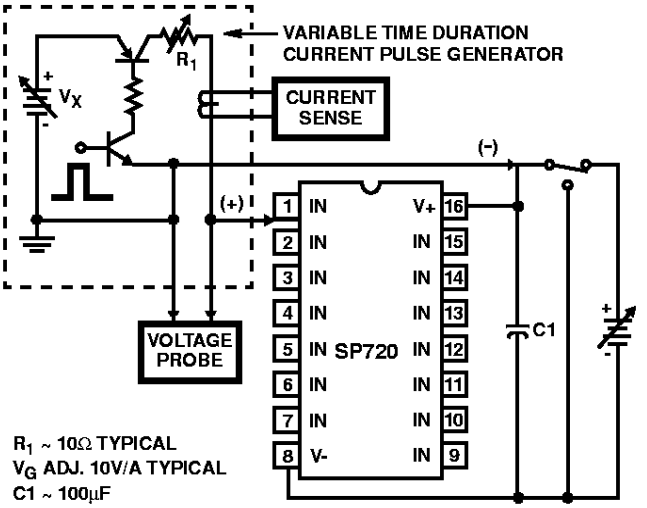


FIGURE 2. TYPICAL SP720 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

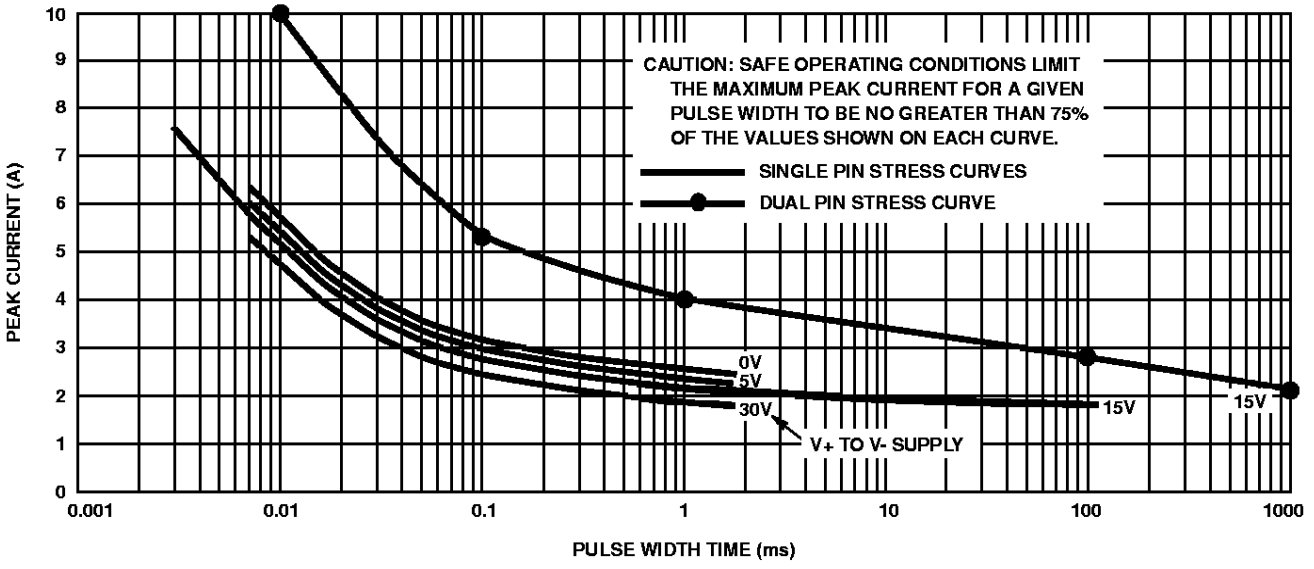


FIGURE 3. TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVER-STRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS, (T_A = 25°C)

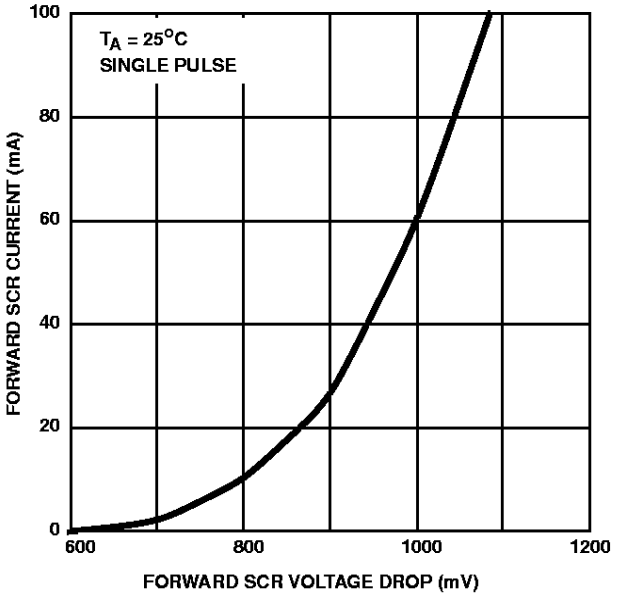


FIGURE 4. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

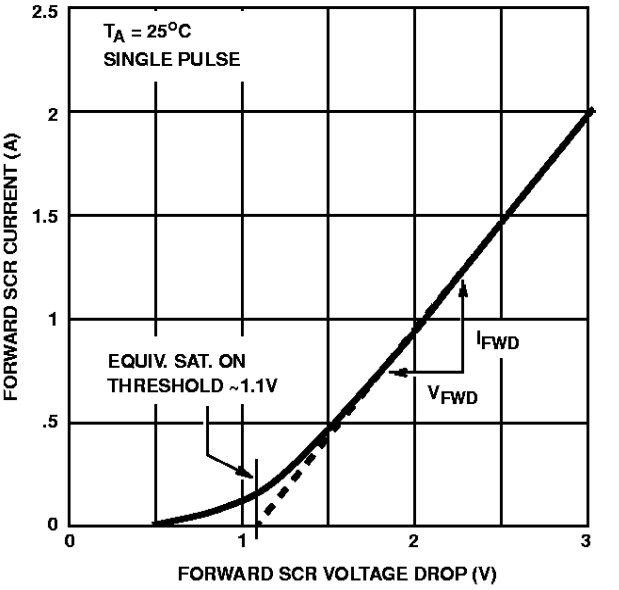


FIGURE 5. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

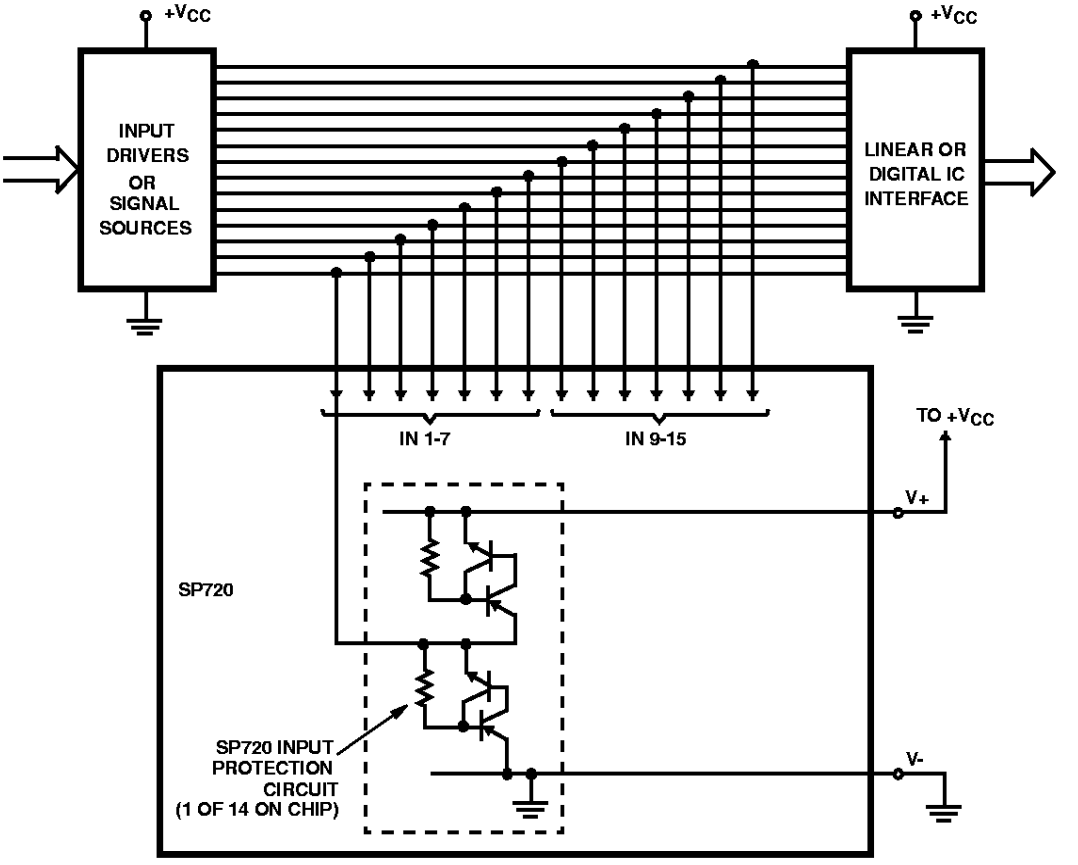


FIGURE 6. TYPICAL APPLICATION OF THE SP720 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN 1V_{BE} ABOVE V+ OR LESS THAN -1V_{BE} BELOW V-. PINOUT SHOWN IS FOR THE SP720MD SBDIP PACKAGE.

Power Dissipation Derating Curves

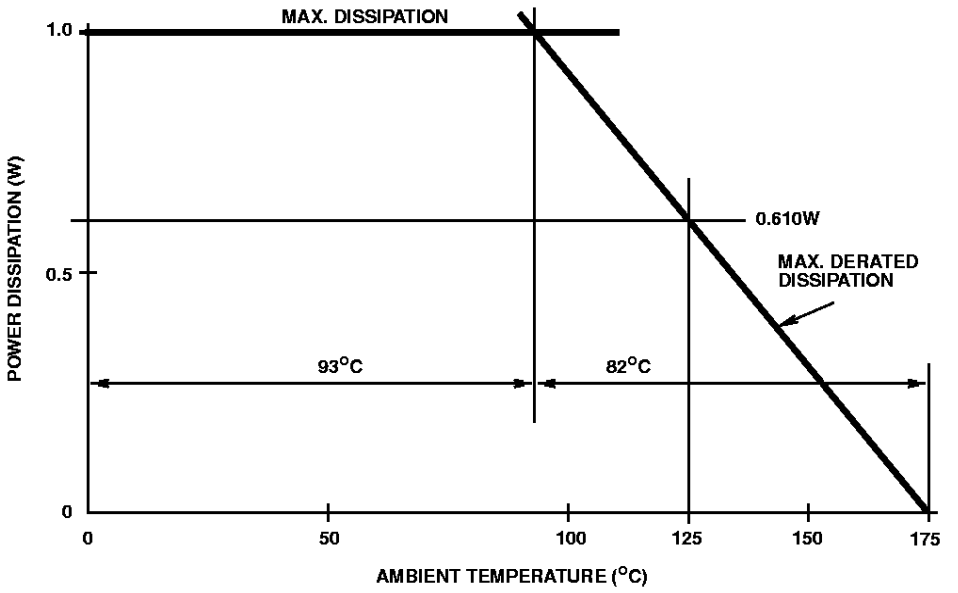


FIGURE 7. SP720MD DERATING CURVE FOR THE 82°C/W THERMAL RESISTANCE OF THE SIDEBRAZE 16 LEAD CERAMIC PACKAGE, DERATED 12.2mW/°C FROM A MAXIMUM P_D OF 1.0W AT 93°C

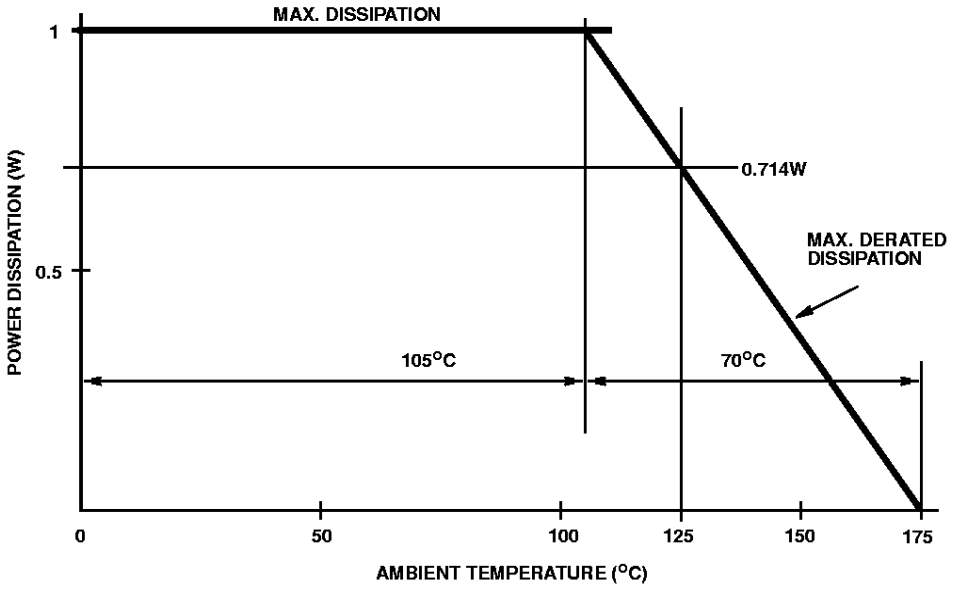
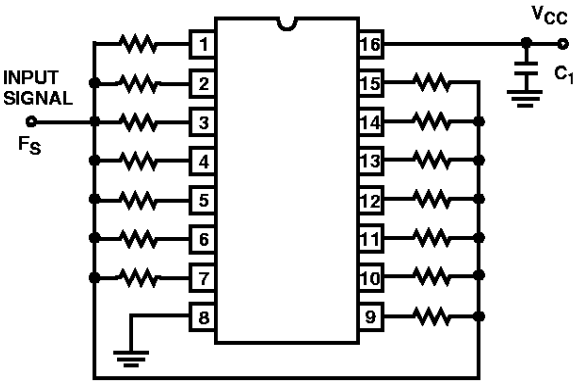


FIGURE 8. SP720MM DERATING CURVE FOR THE 70°C/W THERMAL RESISTANCE OF THE 20 PAD CERAMIC LCC PACKAGE, DERATED 14.3mW/°C FROM A MAXIMUM P_D OF 1.0W AT 105°C

SP720MD-8 and SP720MM-8 Dynamic Burn-In Circuits

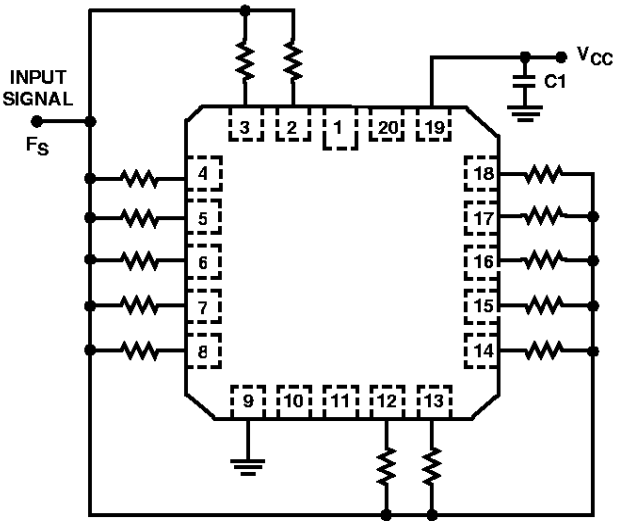
16 LEAD CERAMIC SBDIP



NOTES:

4. All resistors 1kΩ ±10%
5. V_{CC} = 30V ±1%
6. F_S = 0V to 30V ±1%, 50% Duty Cycle
7. C_1 = 22µF Min. Tantalum, 50WV (33WV at 125°C)
8. T_{AMB} = 125°C

20 PAD CLCC



Die Characteristics

DIE DIMENSIONS:
51 x 84 x 14 ±1mils

METALLIZATION:
Type: Al
Thickness: 17.5kÅ ±2.5kÅ

PASSIVATION:
Type: SiO_2
Thickness: 13kÅ ±2.6kÅ

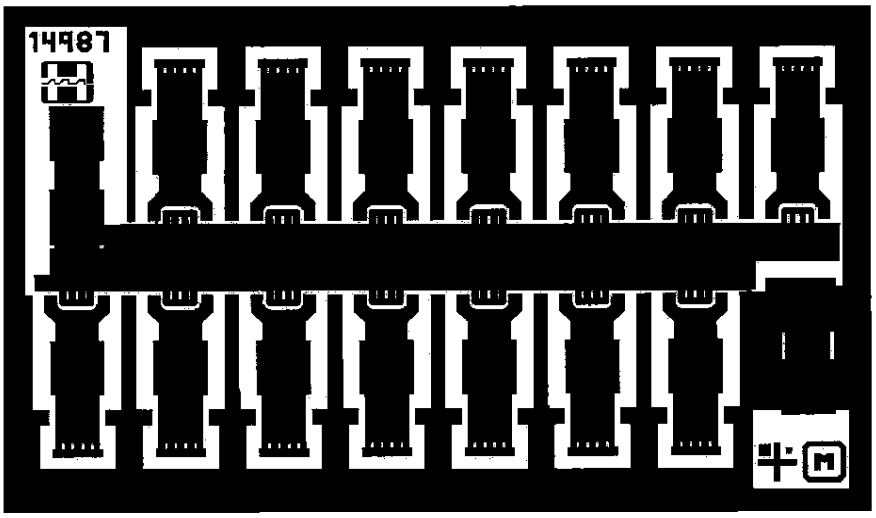
SUBSTRATE POTENTIAL (POWERED UP):
V-

WORST CASE CURRENT DENSITY:
9.18 x 10^4A/cm^2 at 70mA

PROCESS:
Bipolar

Metallization Mask Layout

SP720MD-8, SP720MD, SP720MM-8, SP720MM



(SBDIP PINOUT)