Addendum
DDR3L SDRAM

MT41K512M8RH-125 V:E
MT41K256M16HA-125 V:E

Description

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 (1.5V) SDRAM. Refer to the DDR3 (1.5V) SDRAM data sheet specifications when running in 1.5V compatible mode.

Features

- $V_{DD} = V_{DDQ}$ = 1.35V (1.283–1.45V)
- Backward compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
  - Supports DDR3L devices to be backward compatible in 1.5V applications
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to +95°C
  - 64ms, 8192-cycle refresh at 0°C to +85°C
  - 32ms at +85°C to +95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options / Marking

- Configuration
  - 1 Gig x 4 — 1G4
  - 512 Meg x 8 — 512M8
  - 256 Meg x 16 — 256M16
- FBGA package (Pb-free) – x4, x8
  - 78-ball (10.5mm x 12mm) Rev. D — RA
  - 78-ball (9mm x 10.5mm) Rev. E, J — RH
- FBGA package (Pb-free) – x16
  - 96-ball (10mm x 14mm) Rev. D — RE
  - 96-ball (9mm x 14mm) Rev. E — HA
- Timing – cycle time
  - 1.071ns @ CL = 13 (DDR3-1866) — -107
  - 1.25ns @ CL = 11 (DDR3-1600) — -125
  - 1.5ns @ CL = 9 (DDR3-1333) — -15E
  - 1.875ns @ CL = 7 (DDR3-1066) — -187E
- Special options
  - Visual inspection — V
- Operating temperature
  - Commercial ($0°C \le T_C \le +95°C$) — None
  - Industrial ($–40°C \le T_C \le +95°C$) — IT
- Revision — :D/:E/:J

Table 1: Key Timing Parameters

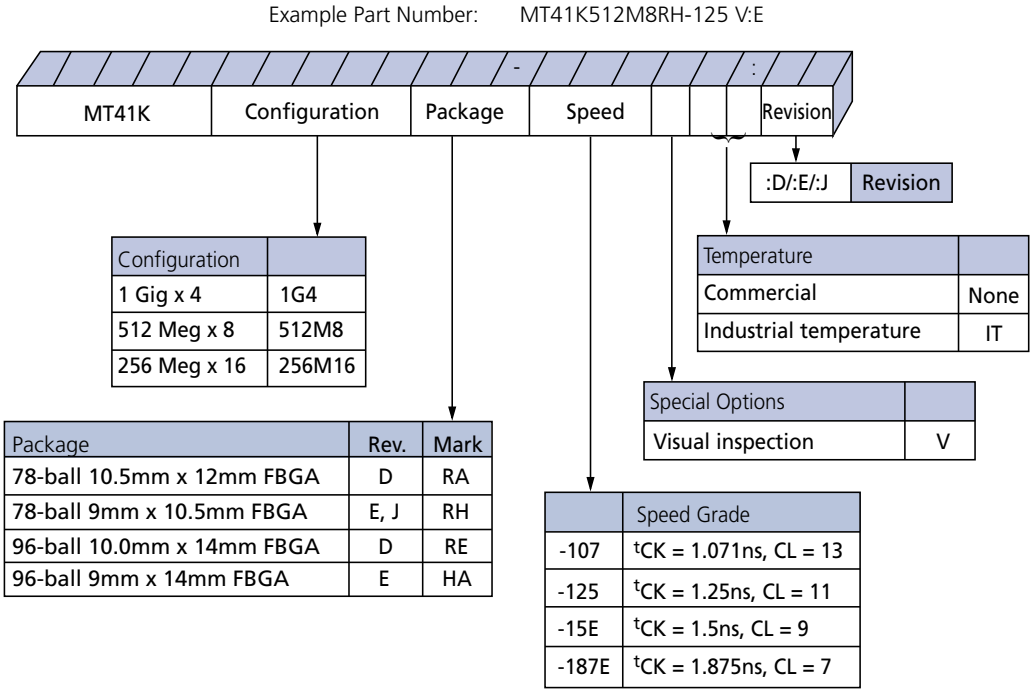
Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-107[1, 2, 3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes:
1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).
3. Backward compatible to 1600, CL = 11 (-125).

Table 2: Addressing

Parameter	1 Gig x 4	512 Meg x 8	256 Meg x 16
Configuration	128 Meg x 4 x 8 banks	64 Meg x 8 x 8 banks	32 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	64K (A[15:0])	64K (A[15:0])	32K (A[14:0])
Bank address	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column address	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page size	1KB	1KB	2KB

Figure 1: DDR3L Part Numbers



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

Revision History

Rev. B – 04/15

- Removed Micron Confidential and Proprietary mark

Rev. A – 02/14

- Initial release; based on 4Gb: x4, x8, x16 DDR3L SDRAM, Rev I 09/13 data sheet (09005aef84780270)

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.