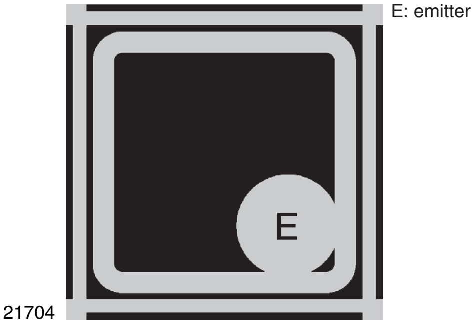
Silicon NPN Phototransistor



FEATURES

- Package type: chip
- Package form: chip
- Dimensions (L x W x H in mm): 0.39 x 0.39 x 0.185
- High photo sensitivity
- High collector current
- Small size
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
e4
RoHS
COMPLIANT
HALOGEN
FREE
GREEN
(5-2008)

DESCRIPTION

T5096P is an epitaxial phototransistor especially designed for optocoupler applications. Despite its small size it has a high sensitivity and ability to drive high currents even under saturation.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY

COMPONENT	I_{ca} (µA)	φ (deg)	$\lambda_{0.1}$ (nm)
T5096P	72 to 600	± 60	480 to 1080

Note

- Test conditions see table “Basic Characteristics”

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T5096P-SD-F	Wafer sawn on foil with disco frame	MOQ: 200 000 pcs	Chip

Note

- MOQ: minimum order quantity

BINNING AND ORDERING CODE

ORDERING CODE DETECTORS	I_{ca} RANGE (µA) AVERAGE
T5096PB-SD-F	80 to 100
T5096PC1-SD-F	100 to 110
T5096PC2-SD-F	110 to 125
T5096PD1-SD-F	125 to 140
T5096PD2-SD-F	140 to 160
T5096PE1-SD-F	160 to 180
T5096PE2-SD-F	180 to 200

BINNING AND ORDERING CODE

ORDERING CODE DETECTORS	I_{ca} RANGE (μA) AVERAGE
T5096PF1-SD-F	200 to 220
T5096PF2-SD-F	220 to 250
T5096PG1-SD-F	250 to 280
T5096PG2-SD-F	280 to 310
T5096PH1-SD-F	310 to 350
T5096PH2-SD-F	350 to 390
T5096PI1-SD-F	390 to 430
T5096PI2-SD-F	430 to 480
T5096PJ1-SD-F	480 to 540
T5096PJ2-SD-F	540 to 600

Note

- I_{ca} values measured on unsawn wafer. E_e = 1 mW/cm2, λ = 950 nm, V_{CE} = 5 V, h_{fe} values for I_C = 1 mA.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Collector emitter voltage		V_{CEO}	85	V
Emitter collector voltage		V_{ECO}	7.8	V
Collector current		I_C	50	mA
Junction temperature		T_j	125	°C
Operating temperature range		T_{amb}	-55 to +125	°C
Storage temperature range		T_{stg1}	-55 to +150	°C

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Collector emitter breakdown voltage	E = 0 mW/cm^2; I_C = 10 μA	$V_{(BR)CEO}$	85			V
Collector emitter dark current	V_{CE} = 50 V, E = 0 lx	I_{CEO}		< 1	50	nA
Wavelength of peak sensitivity		λ_p		910		nm
Range of spectral bandwidth		$\lambda_{0.1}$		480 to 1080		nm

Note

- The measurements are based on samples of die which are mounted on a TO-header without resin coating

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

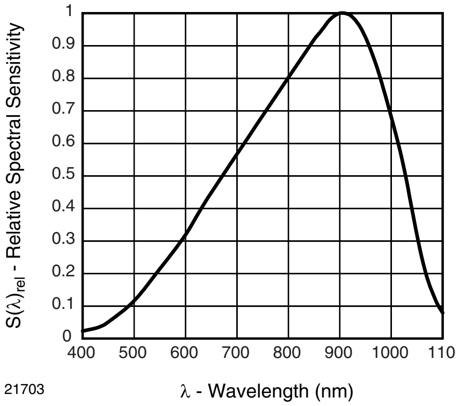


Fig. 1 - Relative Spectral Sensitivity vs. Wavelength

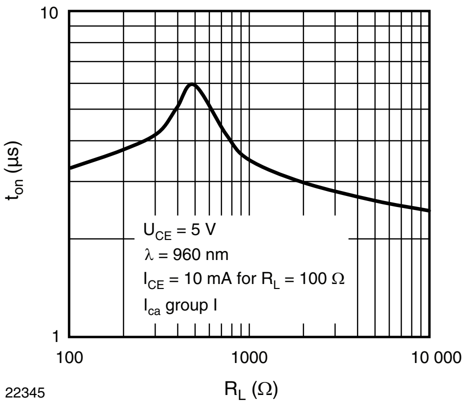


Fig. 2 - Turn-on Time vs. Load Resistance

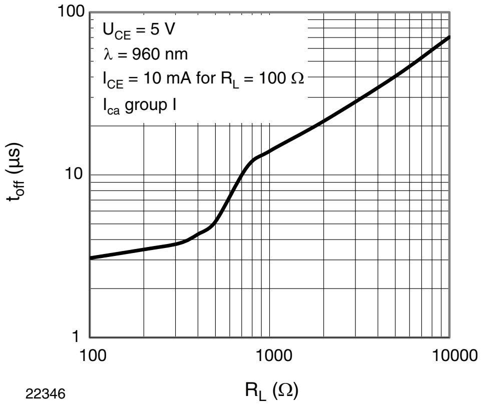


Fig. 3 - Turn-off Time vs. Load Resistance

MECHANICAL DIMENSIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	L_x		0.39		mm
Length of chip edge (y-direction)	L_y		0.39		mm
Die height	H	0.170	0.185	0.200	mm
Bond pad emitter	d		Ø 0.10 (bonding area)		mm

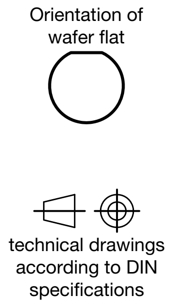
ADDITIONAL INFORMATION

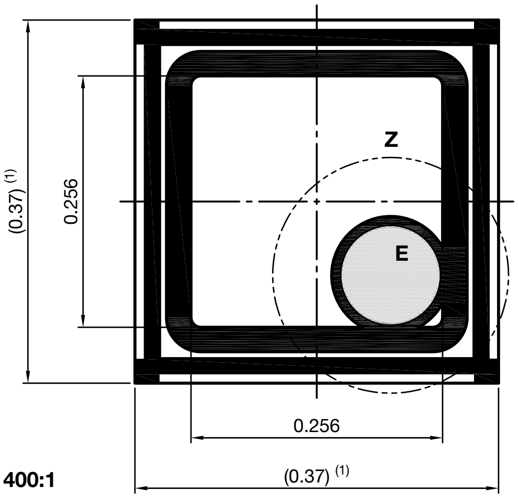
Frontside metallization, emitter	AlSi 1.2 µm
Backside metallization, collector	AuSb 0.4 µm
Dicing	Sawing
Die bonding technology	Epoxy bonding

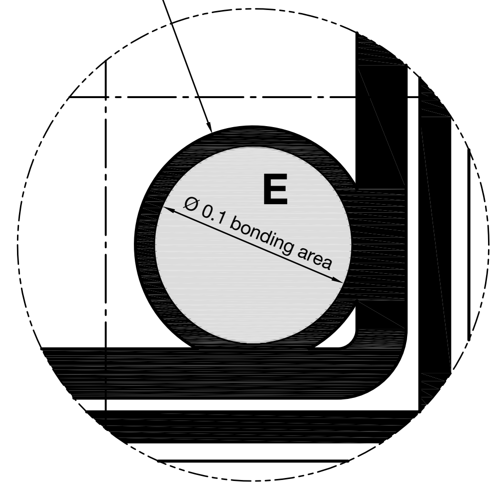
Note

- All products are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.
  The visual inspection shall be made in accordance with the “specification of visual inspection as referenced”. The visual inspection of wafer backside is performed with stereo microscope with incident light and 40x to 80x magnification.
  The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

CHIP DIMENSIONS in millimeters







E: Emitter

Opt. active area: 0.057 mm^2

Bonding area: E: Ø 100 µm

Bonding restricted to this area
in order to avoid damage
of adjacent structures

Thickness: 185 µm ± 15 µm

Drawing-No.: 9.000-5077.3-4
Issue: 2; 03.05.2011

Note

- Not indicated tolerances: ± 0.005

(1) Only for information: dimension of sawn die under consideration of 30 µm saw kerf

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).
Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.

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