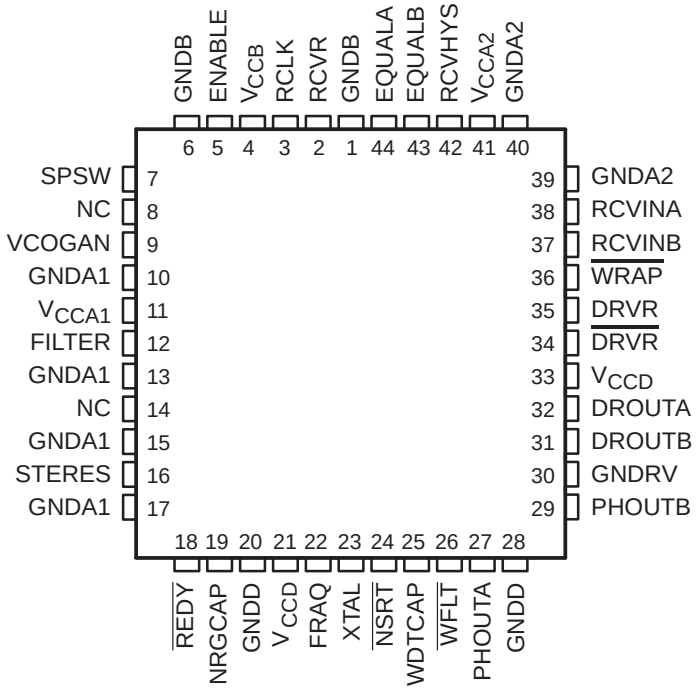
- **Facilitates Connection of the TI380C25, TI380C27, or TMS380C26 to a Token-Ring Network™**
- **Compatible With Electrical Interface of ISO/IEC IEEE Std 802.5:1992 Token-Ring Access Method and Physical-Layer Specifications**
- **Constant-Gain Phase Detector for Unshielded Twisted Pair (UTP) Applications**
- **Phase-Locked Loop (PLL) for Clock Generation and Data Signal Recovery**
- **Independent Transmit and Receive Channels**
- **Phantom Drive for Physical Insertion Onto Ring**
- **16-Mbps and 4-Mbps Token-Ring Data Rates**
- **Integrated Receiver Frequency Equalization**
- **Loop Back (Wrap Mode) for Self-Test Diagnostics**
- **On-Chip Watchdog Timer**
- **ESD Protection Meets 1.5 kV Per MIL-STD-883C, Method 3015**
- **Advanced Low-Power Schottky Technology**
- **Packaged in Plastic J-Leaded Chip Carrier**

FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TMS38054 ring interface device and its associated external passive components form a full-duplex electrical interface to the token ring. Coupling the TMS38054 with one of the TMS380 family of commprocessors forms a highly integrated token-ring LAN adapter compatible with the ISO/IEC IEEE Std 802.5:1992 token-ring access method and physical-layer specifications.

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description (continued)

The TMS38054 operates at the IEEE-standard 16-Mbps and 4-Mbps data rates. The token-ring data stream is received by the TMS38054 and phase aligned using an on-chip phase-locked loop (PLL). The recovered clock and data are passed to the TI380C2x single-chip token-ring commprocessor's protocol-handling circuits for serial-to-parallel conversion and data processing. On transmit, the TMS380C2x provides a differential signal that the TMS38054 converts to analog levels for transmission on the media. A watchdog timer also is included to provide fail-safe deinsertion from the ring in the event of a station failure. The phase-detector gain is constant for all valid differential Manchester data that provide increased margin for unshielded twisted-pair applications.

The TMS38054 is available in a 44-lead plastic chip carrier. The TMS38054 is characterized for operation from 0°C to 70°C with case temperature maintained at or below 99°C.

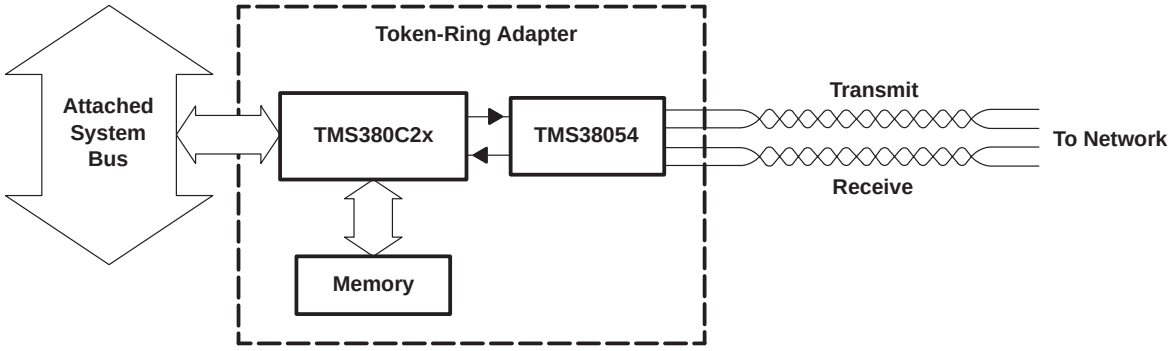


Figure 1. Token-Ring LAN Application Diagram

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O/E†	TYPE‡	DESCRIPTION
DROUTA DROUTB	32 31	O	D	Driver outputs A and B. DROUTA and DROUTB are the differential driver outputs to the token ring via isolation transformers.
DRVR $\overline{\text{DRVR}}$	35 34	I	D	Differential driver data inputs. DRVR and $\overline{\text{DRVR}}$ are the differential inputs that receive the ’380C2x transmit data.
ENABLE	5	I	T	Output-enable control. ENABLE is the TTL input used to enable a board-test mode. High = TMS38054 operates normally Low = All TTL outputs and phantom drive outputs are driven to the high-impedance state. DROUTA and DROUTB are not affected.
EQUALA EQUALB	44 43	E	N	Equalization/gain points A and B. EQUALA and EQUALB are connections that allow frequency tuning of the equalization circuit.
FILTER	12	E	N	Charge pump output/filter buffer input. FILTER allows connection of external components for the PLL filter.
FRAQ	22	I	T	Frequency acquisition control. FRAQ determines the use of frequency or phase-acquisition mode. High = Wide range. Frequency centering to XTAL reference. Low = Narrow range. Phase locked onto the incoming data (RCVINA and RCVINB).
GNDA1§¶	10, 13, 15, 17			Ground reference for VCO and filter input
GNDA2§¶	39, 40			Ground reference for receiver circuits
GNDB§¶	1, 6			Ground reference for input and output buffers
GNDD§	20, 28			Ground reference for digital circuits
GNDRV§	30			Ground reference for driver output circuits
NC§	8, 14			Not internally connected
NRGCAP	19	E	N	Energy-detect capacitor. NRGCAP allows connection to an external capacitor for sensing received-data transitions (energy).
$\overline{\text{NSRT}}$	24	I	T	Phantom-driver control. $\overline{\text{NSRT}}$ enables PHOUTA and PHOUTB through the watchdog timer for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) Falling edge = Active, current output on PHOUTA and PHOUTB
PHOUTA PHOUTB	27 29	O	N	Phantom-driver outputs A and B. PHOUTA and PHOUTB cause insertion onto the token ring.
RCLK	3	O	T	Recovered clock. RCLK is the clock recovered from the token-ring received data. For 16-Mbps operation, RCLK is a 32-MHz clock. For 4-Mbps operation, RCLK is an 8-MHz clock.
RCVHYS	42	E	N	Receiver hysteresis resistor. RCVHYS allows setting of the receiver (hysteresis) threshold.
RCVINA RCVINB	38 37	I	D	Receiver inputs A and B. RCVINA and RCVINB receive the token-ring data via isolation transformers.
RCVR	2	O	T	Recovered data. RCVR contains the data recovered from the token ring.
$\overline{\text{REDY}}$	18	O	T	Ready. $\overline{\text{REDY}}$ to the ’380C2x provides an indication that sufficient time has elapsed since the last transition of FRAQ for the PLL to achieve lock as monitored by the energy-detect capacitor. High = Received data not valid Low = Received data valid

† I = input, O = output, E = provides external component connection to the internal circuitry for tuning
‡ T = TTL signal, N = non-TTL signal, D = differential drive or data
§ These terminals should be connected to a single power or ground plane as appropriate.
¶ GNDA1, GNDA2, and GNDB are internally connected together.

Terminal Functions (Continued)

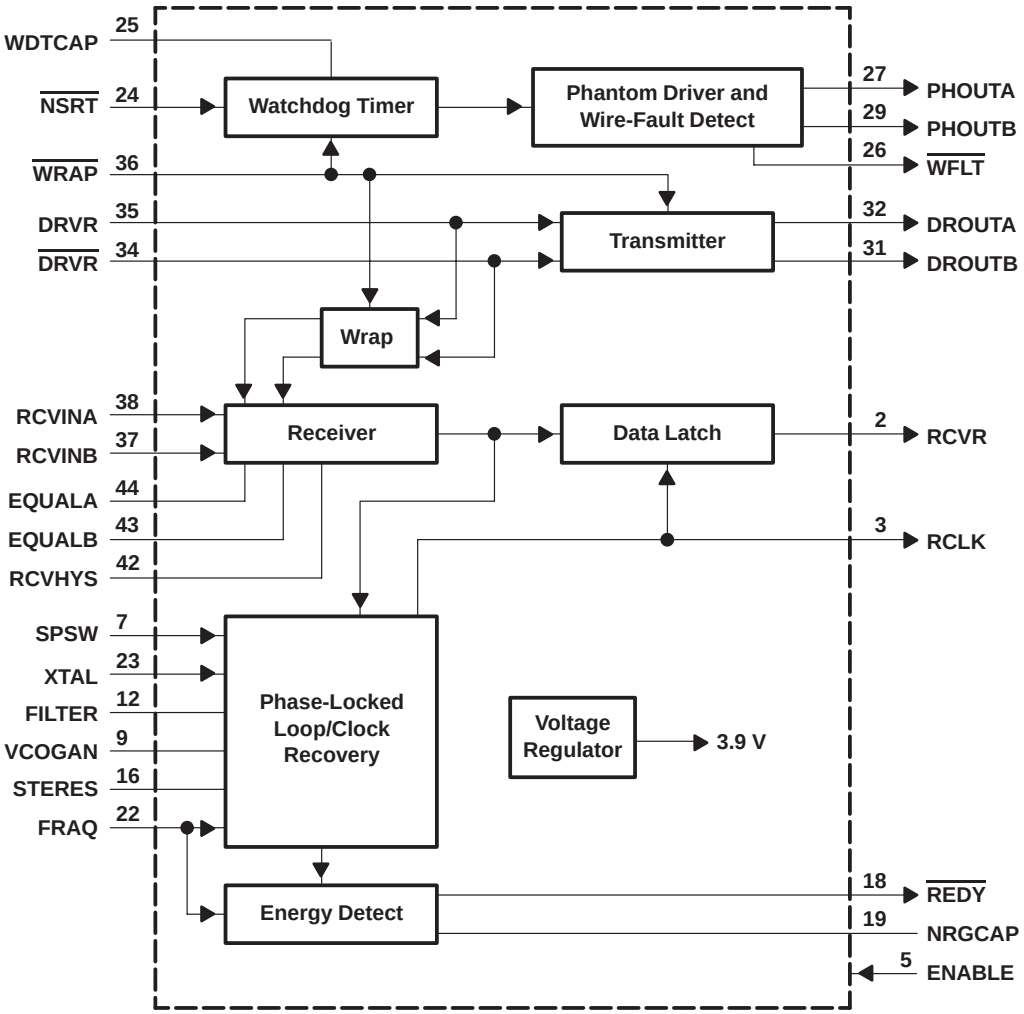
TERMINAL NAME	TERMINAL NO.	I/O/E†	TYPE‡	DESCRIPTION
SPSW	7	I	T	Speed switch. SPSW specifies the token-ring data rate. High = 4-Mbps data rate Low = 16-Mbps data rate
STERES	16	E	N	Static timing error resistor. STERES allows connection to an external resistor for adjusting the static-timing error.
V_{CCA1}§	11			Positive supply voltage for VCO and filter input
V_{CCA2}§	41			Positive supply voltage for receiver circuits
V_{CCB}§	4			Positive supply voltage for input and output buffers
V_{CCD}§	21, 33			Positive supply voltage for digital circuits (5 V)
VCOGAN	9	E	N	VCO gain resistor. VCOGAN allows connection to an external resistor for setting the VCO gain.
WDTCAP	25	E	N	Watchdog timer capacitor. WDTCAP allows connection to an external capacitor, which sets the watchdog-timeout period.
$\overline{\text{WFLT}}$	26	O	T	Phantom-wire-fault. $\overline{\text{WFLT}}$ provides an indication of the presence of a short circuit or open on PHOUTA or PHOUTB. High = No fault Low = Open or short
$\overline{\text{WRAP}}$	36	I	T	Internal-wrap mode control. $\overline{\text{WRAP}}$ allows the TMS38054 to be placed in the loopback-wrap mode for adapter self test. High = Normal ring operation Low = Transmit data drives the receive data.
XTAL	23	I	T	Crystal-oscillator input. XTAL (normally externally gated by FRAQ) is used to synchronize the PLL. XTAL is 32 MHz for 16-Mbps ring, and 8 MHz for 4-Mbps ring.

† I = input, O = output, E = provides external component connection to the internal circuitry for tuning
‡ T = TTL signal, N = non-TTL signal, D = differential drive or data
§ These terminals should be connected to a single power or ground plane as appropriate.

architecture

The major blocks of the TMS38054 include the receiver, data latch, transmitter, wrap, voltage regulator, energy detect, phase-locked loop, watchdog timer, and phantom driver and wire-fault detect (see functional block diagram). The functionality of each block is described in the following sections.

functional block diagram



receiver

The receiver circuit reads incoming data from the ring and performs five other functions:

- Provides dc bias for the differential input
- Provides clamping of large signal swings
- Provides gain and equalization
- Provides definition of thresholds
- Provides hysteresis for data detection

receiver (continued)

Gain as a function of frequency is set by the equalizer impedance. Equalization characteristics are determined by the external equalization circuit across EQUALA and EQUALB. Equalization is effective at low-signal amplitudes. At larger-signal levels, nonlinear effects reduce the effective equalization. The signal level at which saturation occurs is determined by the impedance between EQUALA and EQUALB. The circuit is suitable for differential Manchester-encoded data at 16 Mbps or 4 Mbps.

data latch

The output of the receiver drives two internal circuits: the data latch and the phase detector. The latch samples the internal receiver output signal on the rising edge of the internal recovered clock. Data (RCVR) is therefore stable and can be sampled at the rising edge of RCLK. The timing of this edge is set by the phase detector and other loop components so that the received signal is sampled at the optimum time for error-free data recovery. Both the sampled data and the recovered clock signal are buffered and sent to the ’380C2x token-ring commprocessor as the RCVR and RCLK signals to provide decoding of the differential Manchester data.

Static-timing error is defined as the amount of error that the rising edge of the recovered clock has from the midpoint of the data signal into the data latch. An error of zero is optimum sampling, as this places the rising edge of the sampling clock in the middle of the data pulse. A positive offset represents early sampling.

transmitter

The transmit driver provides differential current drive at a suitable level for driving the data onto the ring. Both outputs (DROUTA and DROUTB) are open collector and intended to drive a center-tapped transformer with the center tap connected to V_{CC}. The output stage controls a fixed current between the two outputs under the control of the driver data input (DRVR and $\overline{\text{DRVR}}$).

DRVR and $\overline{\text{DRVR}}$ drive a differential transmit circuit that enhances the symmetry of the current switching on DROUTA and DROUTB. The DRVR and $\overline{\text{DRVR}}$ inputs are not retimed within the TMS38054. Consequently, low skew in the input is important in order to avoid degrading the transmitted output waveform. The transmitter-drive outputs are not affected by ENABLE. When DRVR is high and $\overline{\text{DRVR}}$ is low, the output current is directed to DROUTA and, when reversed, to DROUTB.

wrap

The wrap function provides an internal signal path used for system self-test diagnostics. When $\overline{\text{WRAP}}$ is taken low, the transmitter outputs are disabled and the receiver inputs are ignored. An alternate path is provided from the transmitter output circuitry to the receiver input circuitry through the wrap circuit. This wrap path to RCVR inverts the transmitted signal. In the internal-wrap mode, attenuation is checked by observing the signal amplitude at EQUALA and EQUALB. Equalization is active at this signal level although the signal does not exhibit the high-frequency attenuation effects for which equalization is intended to compensate.

phantom driver and wire-fault detector

The phantom-drive circuit under control of $\overline{\text{NSRT}}$ generates a dc signal on both of the two drive outputs, PHOUTA and PHOUTB. To maintain the dc signal, $\overline{\text{NSRT}}$ must provide a positive (low-to-high) clock edge once every 20 ms. An internal watchdog timer (oneshot) is designed so that the PHOUTA and PHOUTB dc signals are removed if $\overline{\text{NSRT}}$ fails to have the required transitions. The PHOUTA and PHOUTB signals are sent over the transmit-signal pair to the trunk-coupling unit (TCU) to request that the station be inserted into the ring. The signal current is detected by the TCU, causing the external-wrap path from the transmitter outputs back to the receiver inputs to be broken. A connection is established from the ring to the receiver inputs and from the transmitter outputs to the ring. The phantom-drive outputs are short-circuit protected; they detect a short circuit from either output to ground or when there is an abnormally low load current at either output corresponding to an open circuit in the signal or TCU wiring. Either type of fault results in $\overline{\text{WFLT}}$ being driven low. The logic state of $\overline{\text{WFLT}}$ is high when $\overline{\text{NSRT}}$ is high. All three outputs, PHOUTA, PHOUTB, and $\overline{\text{WFLT}}$, are in the high-impedance state when ENABLE is low.

watchdog timer

The watchdog timer provides protection against a failed adapter remaining on the ring. $\overline{\text{NSRT}}$ must be toggled low or the watchdog timer turns off the phantom drive. The period of the watchdog timer is determined by the value of the external capacitor connected to WDTCAP. The capacitor is chosen to give a period of 21 ms minimum and 50 ms maximum. This assures compatibility with a system that toggles $\overline{\text{NSRT}}$ at a rate faster than once every 20 ms and assures deinsertion from the ring within 50 ms of the last $\overline{\text{NSRT}}$ high-to-low transition.

The duty cycle of $\overline{\text{NSRT}}$ is not critical. Phantom drive is turned on following a falling $\overline{\text{NSRT}}$ edge. Deinsertion occurs if $\overline{\text{NSRT}}$ is left high or low or if the internal-wrap mode is selected from $\overline{\text{WRAP}}$. The following describes the operation of the watchdog timer and indicates the priorities of the control signals:

- $\overline{\text{WRAP}}$ is low (internal mode selected):
  - Phantom drive is off. Operation of the watchdog timer is not defined but can continue, and if the timer has not expired, taking $\overline{\text{WRAP}}$ high can result in the phantom drive being turned on.
- $\overline{\text{WRAP}}$ is high:
  - If the timing capacitor is connected and $\overline{\text{NSRT}}$ goes from high to low, the timing capacitor is charged or recharged to a defined level. Phantom drive is on and discharging of the timing capacitor continues.
  - If the timing capacitor is connected and $\overline{\text{NSRT}}$ goes from low to high, there is no effect on the watchdog timer and the discharging of the timing capacitor continues.
  - If the timing capacitor is connected and the capacitor discharges to a defined level, the phantom drive is turned off regardless of the state of $\overline{\text{WRAP}}$.
  - If the timing capacitor is not connected and the timing capacitor pin is held to V_{CC} + 0.5 V, the phantom drive is controlled directly by $\overline{\text{NSRT}}$. This serves to disable the watchdog-timer function.

voltage regulator

The internal voltage regulator is used to make the performance of the TMS38054 less dependent on the supply voltage. The regulator consists of a band-gap reference scaled up to a nominal 3.9 V with a temperature coefficient designed to compensate for coefficients in circuits referenced to the voltage regulator.

PLL/clock recovery

The TMS38054 contains a PLL for recovering a data clock from the received bit stream. The elements of PLL are: phase and frequency detectors, a charge pump, an external filter (connected to FILTER), a filter buffer, a voltage-to-current converter, and a voltage-controlled oscillator (VCO). There are three pins on the TMS38054 that allow connection to external components and tuning of the characteristics of the PLL. These pins are FILTER, STERES, and VCOGAN. Figure 2 illustrates these blocks. The following paragraphs describe the PLL elements.

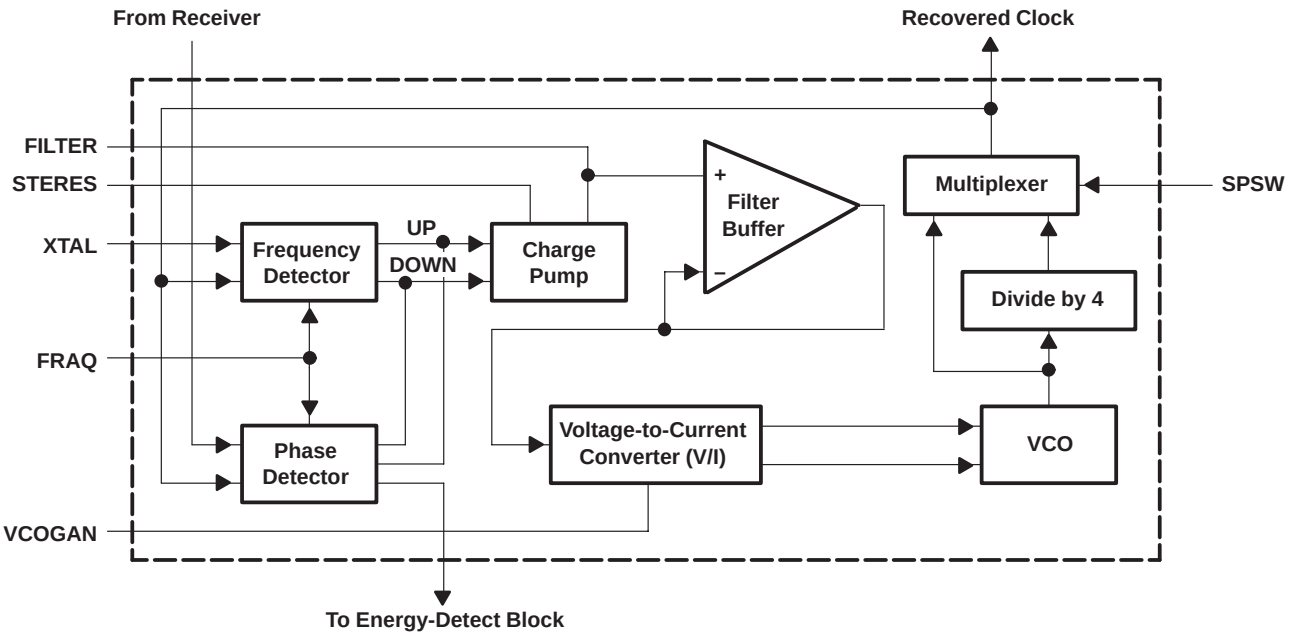


Figure 2. Phase-Locked-Loop Block Diagram

phase and frequency detectors

The phase- and frequency-detector blocks generate control signals suitable for controlling the charge pump. The frequency detector is used to bring the frequency of the VCO close to the frequency of XTAL. The phase detector is used to provide precise phase alignment of the recovered clock to the incoming data. The circuit is not capable of locking the PLL in cases in which the VCO frequency and incoming data frequency differ substantially, hence, the need for frequency centering before phase alignment to incoming data occurs.

The phase detector compares the phase of the received data and the recovered clock, and accordingly generates the charge pump control signals, UP and DOWN. The width of the UP pulse is determined by the phase alignment of the received data and the recovered clock. Each UP pulse is followed by a DOWN pulse of constant width. Phase-detector UP-DOWN sequences are initiated at a 16-MHz rate for all valid differential Manchester data patterns. This rate can drop momentarily during code violations or delimiters, but such deviations are of short duration and the gain of the phase detector can be considered constant.

A multiplexer selects the required detection mode during insertion onto the ring. The frequency-detection mode is selected by taking FRAQ high and the phase-detection mode is selected by taking FRAQ low. The phase or frequency detectors supply the necessary charge (or UP) and discharge (or DOWN) control signals to the charge pump.

charge pump

The charge pump supplies charge to and removes charge from the external filter components.The output of either the phase detector or frequency detector drives the charge pump as selected by FRAQ. The charge pump has two internal inputs, so there are four possible states of the charge pump:

- Pump UP – current into the filter, increasing the voltage
- Pump DOWN – current out of the filter, reducing the voltage
- No pump – in the high-impedance state, holding the voltage on the filter
- Pump UP and pump DOWN – both currents on (not allowed by the detector logic)

charge pump (continued)

The pump UP and pump DOWN currents are approximately equal; the net charge supplied by the charge pump in a given time depends primarily on the relative duration and frequency of UP and DOWN controls from the phase and frequency detectors. If the net current output is positive, the voltage at FILTER rises causing an increase in the VCO clock frequency. If the net output is negative, the FILTER voltage falls, slowing the VCO clock.

The charge-pump block has two constant-current circuits operating continuously, one for pump UP and one for pump DOWN. They are designed for stability under all operating conditions. The UP current is fixed and directly affects the magnitude of the loop gain and the bandwidth and damping factor of the loop. Any difference between the UP and DOWN currents creates an offset in the loop, which introduces a static-timing error. Provision for an external resistor at STERES is included to allow slight variation in the DOWN current and allows the static-timing error of the loop to be adjusted to compensate for error introduced by the charge pump and other elements of the PLL. This resistor is not required for normal operation of the TMS38054, but provisions should be made to accommodate this resistor in future applications.

external filter

The external filter consists of passive external components connected from FILTER to ground. A system diagram for the PLL circuit is shown in Figure 3. The phase-detector/charge-pump gain, G_d, is given in the electrical specifications as 16 Mbps. This value is true for any valid differential Manchester data pattern. The result is in μA/ns, which can be converted to A/rad by using equation 1. The value, in A/rad, is the same at both 16 Mbps and 4 Mbps.

The VCO gain, G_O, is given in the electrical specifications at 16 Mbps. This value is in MHz/V, which can be converted to rad/volt by using equation 1. The value at 4 Mbps is one-fourth this value because of the ×4 divider on the VCO output at 4 Mbps.

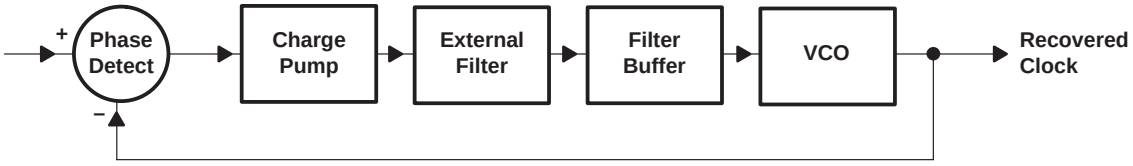


Figure 3. Analytical PLL Diagram

A typical external filter circuit is shown in Figure 4. Capacitor C5 limits the filter-buffer ripple but should be chosen to be as small as possible to reduce PLL overshoot. The resistor (R5) sets the effective bandwidth of the PLL closed loop, and capacitor C4 sets the damping factor. The filter buffer is an amplifier with bandwidth of 3–5 MHz.

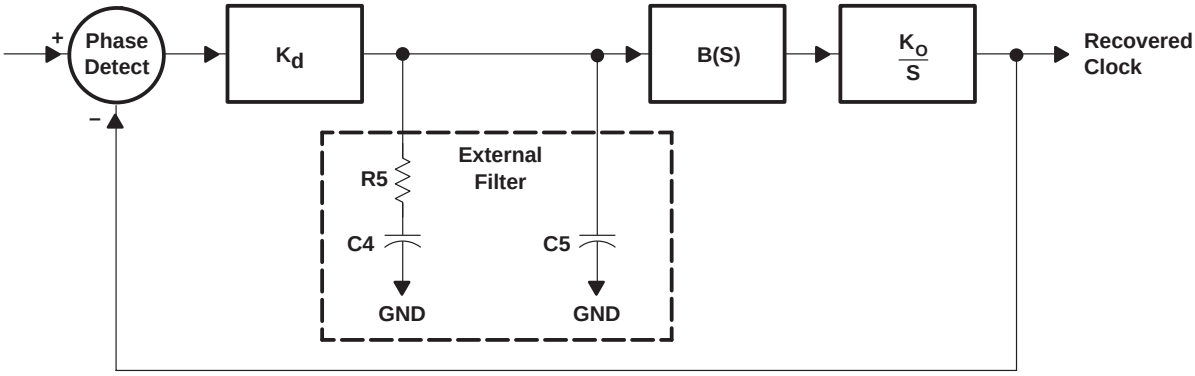


Figure 4. Analytical PLL Model

external filter (continued)

The simplified equations for the PLL are:

VCO gain

$$K_o = (G_o)(10^6)(2\pi)(F) \qquad \text{rad/(s • v)} \qquad (1)$$

Phase-detector gain

$$K_d = \frac{(G_d)(10^3)(31.25)(10^{-9})}{2\pi} \qquad \text{A/rad}$$

PLL-noise-equivalent bandwidth

$$B_L = \frac{(K_o)(K_d)(\text{R5 in ohms})}{4} \qquad \text{Hz}$$

Where:

G_O = the VCO gain measured in MHz/V
G_d = phase-detector gain measured in μA/ns
F = the frequency divider factor; i.e., F = 1 for 16-Mbps operation
F = 0.25 for 4-Mbps operation

These equations are only a guide and the actual bandwidth and PLL-damping characteristics should be obtained through correlation and modeling on specific hardware implementations that take into effect all circuit card parasitics. Both 16-Mbps and 4-Mbps ring operation can be achieved by suitable selection of glue components at each frequency. More information on PLL characteristics are found in:

- Gardner, Floyd, *Phase Lock Techniques*, John Wiley & Sons, 1979.
- *Token Ring Access Method and Physical Layer Specification*, ANSI/IEEE/ISO/IEC Standard 802.5:1992.
- Gardner, Floyd, “Charge-Pump Phase-Locked Loops*”, IEEE Transaction Communications,* Vol. COM–28, pp. 1849–1858, Nov. 1980.

filter buffer and voltage-to-current converter (V/I)

The filter-buffer amplifier is a unity-gain amplifier used to buffer the voltage present at FILTER with minimal leakage current. The output of the filter buffer drives a voltage-current (V/I) converter that produces equal currents, proportional to the filter voltage, for use in the VCO. The current level or constant of proportionality is set by the external resistor connected to ground connected at VCOGAN. This resistor sets the VCO gain, which is critical to loop gain and damping. The filter voltage range over which the current level tracks the voltage determines the pull-in range of the VCO.

VCO

The VCO is an emitter-coupled astable multivibrator. The frequency is set by internal circuit parameters, the currents from the filter buffer, and an internal VCO timing capacitor. Symmetrical circuit design helps ensure symmetry of the VCO output, which has a nominal frequency of 32 MHz. The VCO output is buffered and sent to the divider (for 4-Mbps operation) and multiplexer circuit.

divider and multiplexer

The multiplexer selects the source of the recovered clock, which can be either the direct output of the VCO (nominally a 32-MHz signal) or the divided version of the VCO output (nominally an 8-MHz signal) for 16- or 4-Mbps operation. The output clock of the VCO is fed to a divide-by-4 circuit and to a multiplexer. The divider is enabled when SPSW is high. The recovered clock is passed to frequency and phase detectors, the clock of the data latch, and is buffered at RCLK and passed on to the ’380C2x commprocessor for processing of the received data.

energy detect

The energy-detect circuit provides a timing delay on $\overline{\text{REDY}}$. When FRAQ changes state, it indicates to the energy-detect circuit that a change of lock mode has occurred and that time must be allowed before data recovered by the TMS38054 can be considered valid. The energy-detect-timing capacitor is discharged shortly after a low or high going transition of FRAQ, which results in the $\overline{\text{REDY}}$ signal being deasserted.

The time taken for the TMS38054 to acquire phase lock depends on the transition density of the incoming data, so the delay of the energy-detect circuit also changes. Each rising transition of data results in a current pulse of fixed duration being injected into the energy-detect-timing capacitor. The charge time of the capacitor is dependent on incoming-data-transition density and $\overline{\text{REDY}}$ is reasserted after the capacitor reaches an internally set threshold voltage.

A small discharge current is always present on the energy-detect-timing capacitor. When the incoming-data-transition density falls below a certain threshold, the current pulses may not be sufficient to overcome this discharge current and $\overline{\text{REDY}}$ may not be asserted.

test mode

The TMS38054 features a test mode for board-level testing with the components in the circuits. This facilitates testing by bed-of-nails testers. This test mode is enabled by pulling ENABLE to a low level. DROUTA and DROUTB are not affected by this function. When ENABLE is high, the TMS38054 operates normally. When ENABLE is low, the circuit continues to operate except that PHOUTA, PHOUTB, RCVR, $\overline{\text{WFLT}}$, and RCLK are driven to the high-impedance state and $\overline{\text{REDY}}$ is driven high.

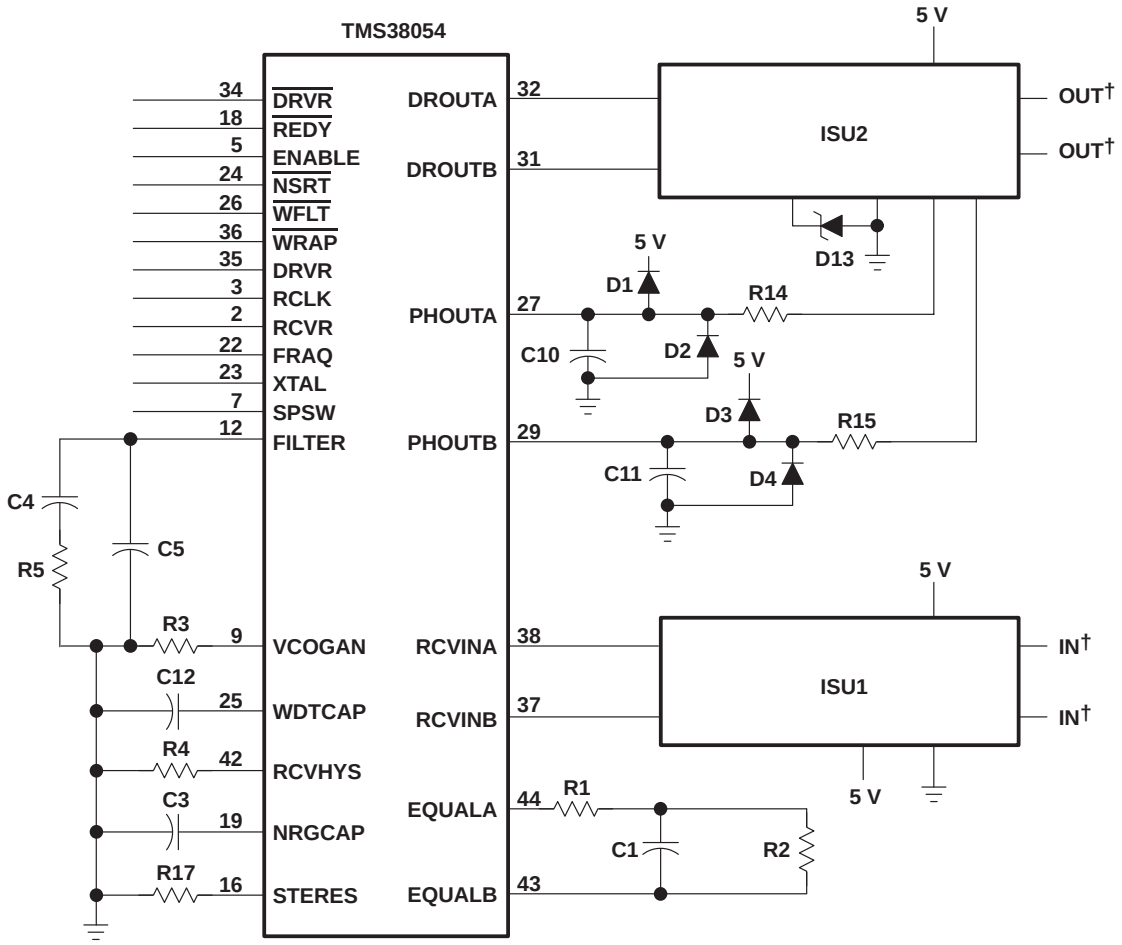
external passive circuitry

Figure 5 shows an arrangement of external components for a typical 16-Mbps or 4-Mbps token-ring interface. The selection of component values is dependent on the objective of the design. The design needs to take into account the importance of layout and component selection (values and tolerances).

The ISU1 and ISU2 blocks represent transformers that couple data from the TMS38054 to the ring. They also represent protection circuitry against large voltage excursions. Information on ISU1 and ISU2 connections can be found in the *TMS38054 Second-Generation Ring Interface Design Note* (revision C). To obtain this design note, contact the TMS380 Technical Support Line at NETWORKS@ti.com.

Table 1. Typical Components for Figure 5

SYMBOL(S)	FUNCTION
C1	Equalizer capacitor
C3	Energy-detect capacitor
C4	PLL-filter capacitor
C5	PLL-filter capacitor
C10, C11	Phantom-drive isolation capacitor
C12	Watchdog-timer capacitor
D1–D4	Phantom surge-suppression diodes
D13	Driver surge-suppression zener diode
R1	Equalizer resistor
R2	Equalizer resistor
R3	VCO gain resistor
R4	Receiver-hysteresis resistor
R5	PLL-filter resistor
R14, R15	Phantom-drive resistor
R17	Static-timing-error resistor
ISU 1	Isolation/shaping unit (see previous page)
ISU 2	Isolation/shaping unit (see previous page)



† Refer to the *TMS38054 Second-Generation Ring Interface Design Note* (revision C) for further information.

Figure 5. Typical Token-Ring Interface Circuit for 16 Mbps or 4 Mbps

absolute maximum ratings (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range: Driver outputs	–0.5 V to 8 V
All other outputs (see Note 2)	–0.5 V to 7 V
Power dissipation (see Note 3)	1.25 W
Storage temperature range, T_{stg}	–10°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Inputs may be taken to more negative voltages if the current is limited to 20 mA.
2. These outputs may not be taken more than 0.5 V above the V_{CC} pins.
3. Maximum power dissipation per package

recommended operating conditions†

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	2			V
V_{IL}	Low-level input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW			0.7	V
	Receiver input bias voltage (see Note 4)		V_{SB}–1		V_{SB}+1	V
I_{OH}	High-level output current	RCVR, RCLK, $\overline{WFLT}$, $\overline{REDY}$			–0.1	mA
I_{OL}	Low-level output current	$\overline{REDY}$, RCVR, $\overline{WFLT}$, RCLK			1	mA
T_C	Operating case temperature		0		99	°C

† Recommended operating conditions indicate the conditions that must be met to ensure that the device functions as intended and meets the detailed electrical specifications. Unless otherwise noted, all electrical specifications apply for all recommended operating conditions. Voltages are measured with respect to the device ground pins. Currents into the device are considered to be positive.

NOTE 4: V_{SB} is the self-bias voltage of the input pair RCVINA and RCVINB. It is defined as $V_{SB} = (V_{SBA} + V_{SBB})/2$ (where V_{SBA} is the self-bias voltage of RCVINA; V_{SBB} is the self-bias voltage of RCVINB). The self-bias voltage of both pins is approximately $V_{CC}/2$.

electrical characteristics over recommended range of supply voltage (unless otherwise noted)

TTL input

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{IH}	High-level input current	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 2.7 V		20	µA
I_{IL}	Low-level input current	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 0.4 V		–0.4	mA
I_I	Input current at maximum input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 7 V		100	µA
V_{IK}	Input clamp voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW, DRVR, $\overline{DRVR}$	I_I = –12 mA		–1.5	V

TTL output (RCVR, RCLK, $\overline{REDY}$, and $\overline{WFLT}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA		0.45	V
I_{OZH}	Off-state output current with high-level voltage applied	V_O = 2.7 V		±100	µA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0.4 V		±100	µA

electrical characteristics over recommended range of supply voltage (unless otherwise noted) (continued)

receiver input (RCVINA and RCVINB)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Rising input threshold voltage, V_{T+}	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 4, 5, and 6		35	mV
Falling input threshold voltage, V_{T-}	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 4, 5, and 6	–35†		mV
Asymmetry threshold voltage, ($V_{T+} + V_{T-}$)	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 4, 5, and 6	–20†	20	mV
Rising input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	R_{tst} = 330 Ω, R4 = 2.49 kΩ, See Notes 4, 5, and 6	–30†	30	mV
Falling input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	R_{tst} = 330 Ω, R4 = 2.49 kΩ, See Notes 4, 5, and 6	–30†	30	mV
Receiver input current	R_{tst} = 330 Ω, Both inputs at V_{SB}, See Note 4		±25	μA
	R_{tst} = 330 Ω, Input under test at V_{SB} + 1.0 V, Other input at V_{SB} – 1 V, See Note 4	300	700	
	R_{tst} = 330 Ω, Input under test at V_{SB} – 1.0 V, Other input at V_{SB} + 1.V, See Note 4	–300	–700	
Equalizer bias current (EQUALA and EQUALB)	RCVINA and RCVINB open, EQUALA and EQUALB at 3 V	1.125	1.875	mA

† The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this data sheet for threshold voltages only.

NOTES: 4. V_{SB} is the self-bias voltage of the input pair RCVINA and RCVINB. It is defined as $V_{SB} = (V_{SBA} + V_{SBB})/2$ (where V_{SBA} is the self-bias voltage of RCVINA; V_{SBB} is the self-bias voltage of RCVINB). The self-bias voltage of both pins is approximately $V_{CC}/2$.
5. R_{tst} is a resistor connected between pins 43 and 44; it replaces R1, R2, and C1 (see Figure 5).
6. V_{IC} is the common-mode voltage applied to RCVINA and RCVINB.

transmitter

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
	Output current, on	DROUTA, DROUTB	$V_O = V_{CC}$,	See Note 7	20	35	mA
	Output current, off	DROUTA, DROUTB	V_O = 8 V,	See Note 7		100	μA
	Output current, off	DROUTA, DROUTB	$\overline{WRAP} = V_{IL}$,	V_O = 8 V		100	μA
I_{IH}	High-level input current	DRVR, $\overline{DRVR}$	Input under test at 2.7 V,	Other input at 0.4 V	100	700	μA
I_{IL}	Low-level input current	DRVR, $\overline{DRVR}$	Input under test at 0.4 V,	Other input at 2.7 V	–100	–700	μA

NOTE 7: Output not under test is loaded with 75 Ω to V_{CC}.

phantom driver (PHOUTA and PHOUTB)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA		4.1		V
		I_{OH} = –2 mA		3.8		
I_{OS}	Short circuit output current	V_O = 0 V,	$\overline{NSRT} = V_{IL}$	–4	–20	mA
I_{OH}	High-level output current	$V_O = V_{CC}$,	$\overline{NSRT} = V_{IH}$		±100	μA
I_{OZH}	Off-state output current with high-level voltage applied	$V_O = V_{CC}$,	ENABLE = V_{IL}		±100	μA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0 V,	ENABLE = V_{IL}		±100	μA

electrical characteristics over recommended range of supply voltage (unless otherwise noted) (continued)

wire fault ($\overline{\text{WFLT}}$) (see Notes 8 and 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Phantom-normal condition	2.9 kΩ < R_{L1} < 5.5 kΩ, 2.9 kΩ < R_{L2} < 5.5 kΩ	2.4		V
Phantom-open condition	R_{L1} > 9.9 kΩ and 2.9 kΩ > R_{L2} < 5.5 kΩ or R_{L2} > 9.9 kΩ and 2.9 kΩ < R_{L1} < 5.5 kΩ		0.45	V
Phantom-short condition	R_{L1} < 0.1 kΩ and 2.9 kΩ < R_{L2} < 5.5 kΩ or R_{L2} < 0.1 kΩ and 2.9 kΩ < R_{L1} < 5.5 kΩ		0.45	V

NOTES: 8. The wire-fault logic recognizes a load condition corresponding to greater than 9.9 kΩ to ground as an open-circuit fault, but it does not recognize a load condition less than 5.5 kΩ to ground as an open. The wire-fault logic recognizes a load condition corresponding to less than 100 Ω to ground as a short-circuit fault, but it does not recognize a load condition corresponding to greater than 2.9 kΩ to ground as a short. Figure 6 illustrates this with R_{L1} connected from PHOUTA to ground and R_{L2} connected from PHOUTB to ground.

9. R_{L1} is connected from PHOUTA to ground; R_{L2} is connected from PHOUTB to ground.

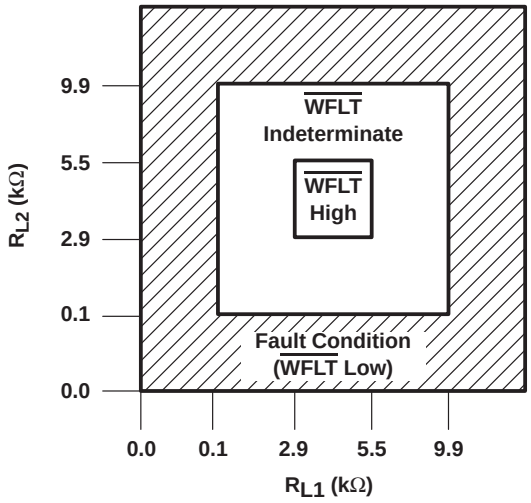


Figure 6. Wire-Fault Pin Test

electrical characteristics over recommended range of supply voltage (unless otherwise noted) (continued)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.25 V, See Figure 7		180	200	mA

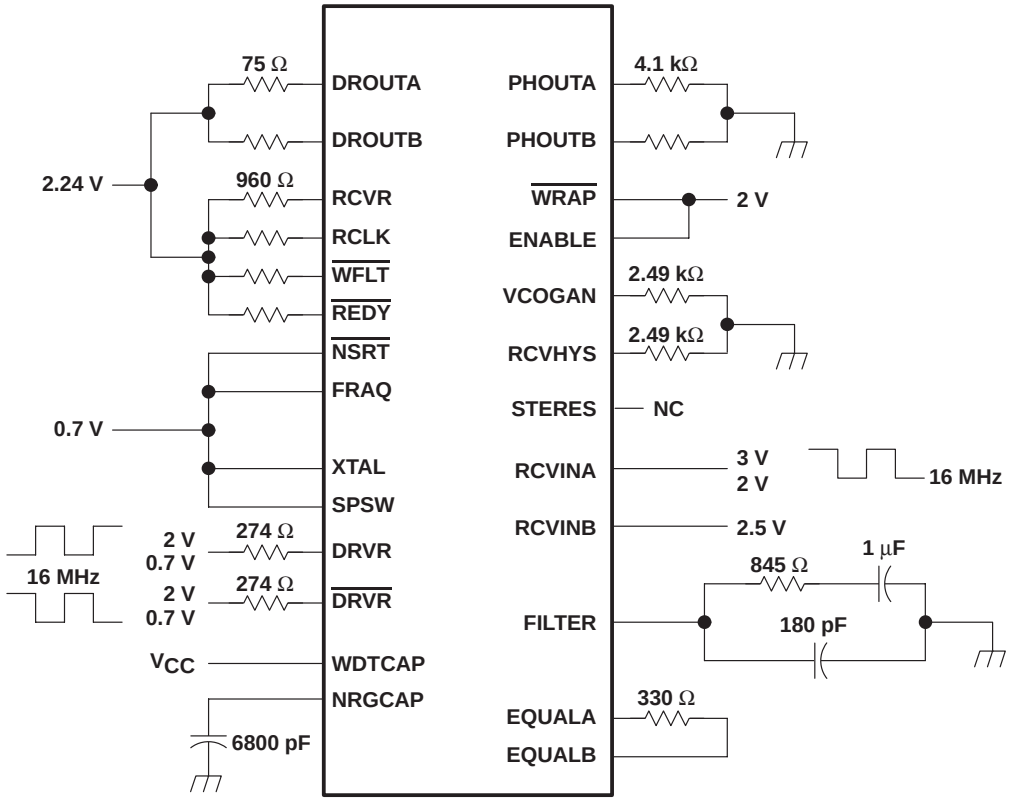


Figure 7. I_{CC} Test Circuit

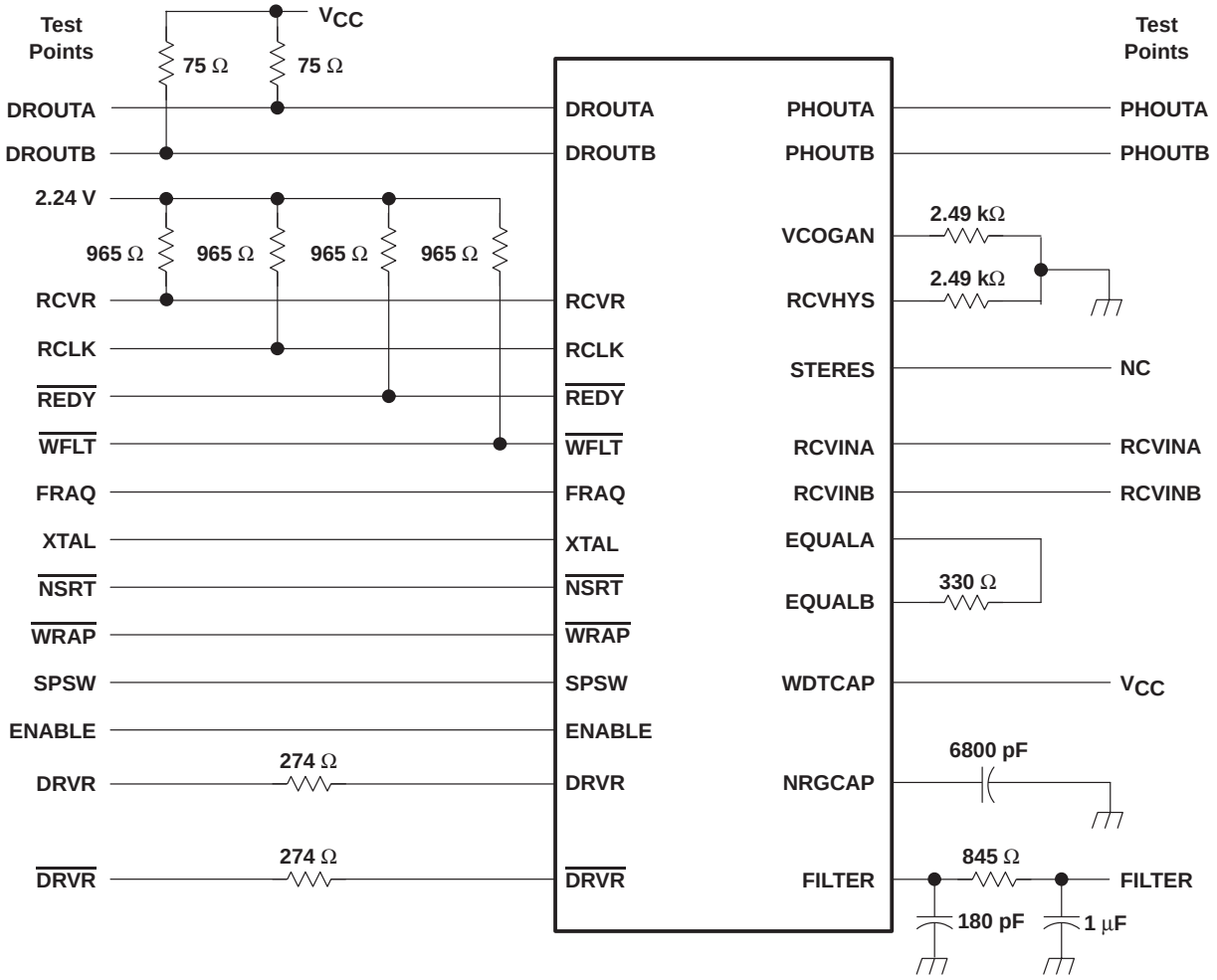


Figure 8. ac Test Circuit

timing requirements over recommended range of supply voltage (unless otherwise noted)

transmitter (see Figures 8 and 9)

NO.			TEST CONDITIONS	MIN	TYP	MAX	UNIT
1	$t_{sk(DRVR)}$	Delay time, $\overline{DRVR}$ edge (1.5 V) to following $\overline{DRVR}$ edge (1.5 V)		See Note 10			
2	$t_{d(DROUTA)H}$	Delay time, DRVR falling edge (1.5 V) to DROUTA rising edge (midpoint)		See Note 10			
3	$t_{d(DROUTA)L}$	Delay time, DRVR rising edge (1.5 V) to DROUTA falling edge (midpoint)		See Note 10			
4	$t_{d(DROUTB)L}$	Delay time, DRVR falling edge (1.5V) to DROUTB falling edge (midpoint)		See Note 10			
5	$t_{d(DROUTB)H}$	Delay time, DRVR rising edge (1.5 V) to DROUTB rising edge (midpoint)		See Note 10			
6	DROUTA/DROUTB skew	$t_{d(DROUTA)H} - t_{d(DROUTB)L}$	$t_{sk(DRVR)}$ = –1 ns			±3	ns
		$t_{d(DROUTA)L} - t_{d(DROUTB)H}$	$t_{sk(DRVR)}$ = 1 ns			±3	
7	DROUTA/DROUTB asymmetry	$\frac{t_{d(DROUTA)L} + t_{d(DROUTB)H}}{2} - \frac{t_{d(DROUTA)H} + t_{d(DROUTB)L}}{2}$	$t_{sk(DRVR)}$ = –1 ns			±2	ns
			$t_{sk(DRVR)}$ = 1 ns			±2	

NOTE 10: This parameter is not tested to a minimum or a maximum but is measured and used as a component required for parameters 6 and 7.

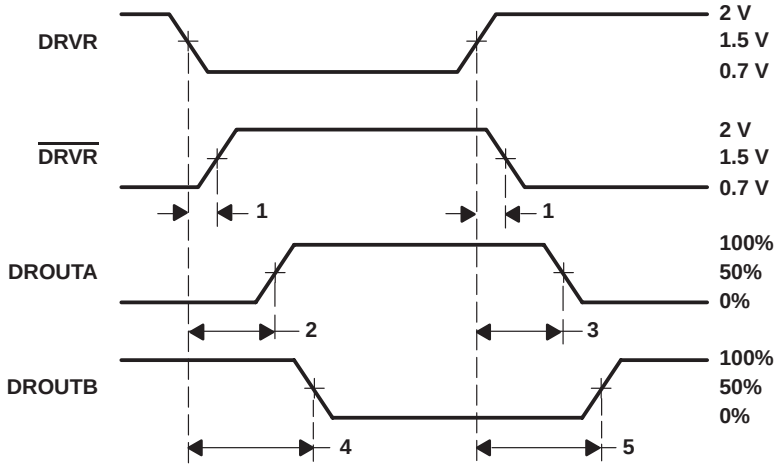


Figure 9. Skew and Asymmetry From DRVR and $\overline{DRVR}$ to DROUTA and DROUTB

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

RCLK and RCVR (see Figures 8 and 10)

NO.			TEST CONDITIONS		MIN	TYP	MAX	UNIT
8	$t_{w(RCLK)L}$	Pulse duration, RCLK low	4 Mbps, $t_{c(RCLK)}$ = 115 ns	See Note 11	46			ns
			16 Mbps, $t_{c(RCLK)}$ = 30 ns		10			
9	$t_{w(RCLK)H}$	Pulse duration, RCLK high	4 Mbps, $t_{c(RCLK)}$ = 115 ns,	See Note 11	35			ns
			16 Mbps, $t_{c(RCLK)}$ = 30 ns,		8			
10	$t_{su(RCVR)}$	Setup time, RCVR valid to RCLK rising edge (1.5-V point)	$t_{c(RCLK)}$ = 31.25 ns		10			ns
11	$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK rising edge (1.5-V point)	$t_{c(RCLK)}$ = 31.25 ns		2			ns
12	$t_{c(RCLK)}$	Cycle time, RCLK (see Note 12)	4 Mbps			125		ns
			16 Mbps			31.25		

NOTES: 11. The pulse duration high and low of RCLK is tested at a frequency in excess of nominal to ensure correct operation during brief periods where lock is lost.
12. This parameter is not tested. The typical value shown is that for the recovered clock from an IEEE 802.5 token ring.

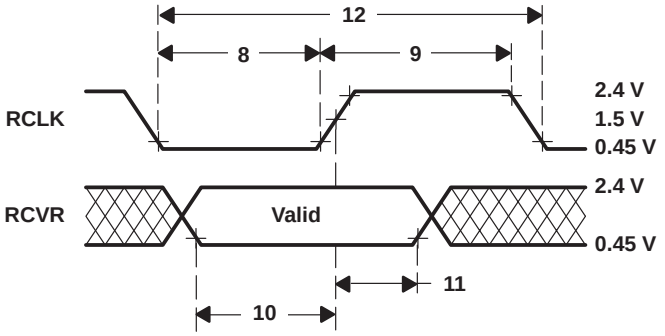


Figure 10. RCLK and RCVR Timing

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

loop parameters (see Figures 8, 11, and 12)

	TEST CONDITIONS				MIN	MAX	UNIT
Filter voltage, low	f = 30.8 MHz,	See Note 13			2		V
Filter voltage, high	f = 33.3 MHz,	See Note 13				3	V
VCO gain (G_O)	f1 = 28.6 MHz,	f2 = 36.4 MHz,	See Note 14		12.75	17.25	MHz/V
Phase-detector gain (G_d)	$I_{(FILTER)1}$ = +50 μA,	$I_{(FILTER)2}$ = –50 μA,	f = 32 MHz,	See Note 15	5.40	7.20	μA/ns

NOTES: 13. The frequency f is applied to XTAL with FRAQ high as shown in Figure 11. The voltage at FILTER is measured after lock is achieved.

14. A frequency of f1 is applied to the XTAL with FRAQ high. After lock is achieved, the voltage at FILTER is measured (V1). This is repeated using f2 and measuring V2. VCO gain is calculated as (f2 – f1)/(V2 – V1). The result is in Hz/V (see external filter section).

15. The circuit of Figure 8 is used to measure phase-detector gain with $I_{(FILTER)}$ injected at the filter test point. Figure 12 shows the relevant timing. With the TMS38054 in phase lock, the propagation delay (t_p) between RCVINA positive transition and RCLK negative transition is measured. A value t_{p1} is seen when $I_{(FILTER)} = I_{(FILTER)1}$, and a value of t_{p2} is seen when $I_{(FILTER)} = I_{(FILTER)2}$. The phase-detector gain is then calculated as $(I_{(FILTER)2} – I_{(FILTER)1}) \div (t_{p1} – t_{p2})$. The result is in μA/ns (see *external filter* section).

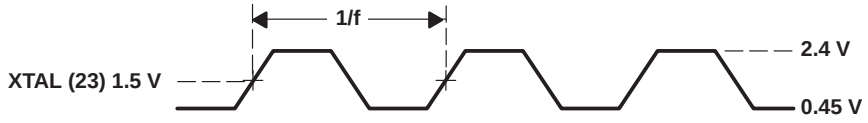


Figure 11. VCO-Gain and Filter-Voltage Test Timing

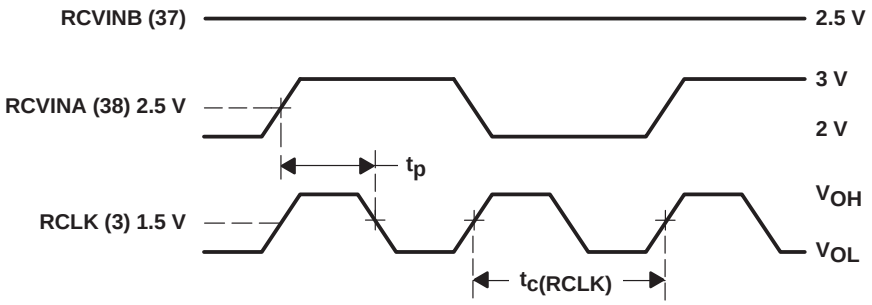


Figure 12. Phase-Detector-Gain Test Timing

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

data recovery (see Figures 8 and 13 and Note 16)

NO.			TEST CONDITIONS	MIN	MAX	UNIT
13	t_{se}	Static timing error from voltage midpoint of RCVINA edge to midpoint to RCVINA pulse	4 Mbps, f = 8 MHz		±20	ns
			16 Mbps, f = 32 MHz		±3.62	

NOTE 16: The TMS38054 is phase locked to a RCVINA waveform as shown in Figure 13 with RCVINB biased to 2.5 V. RCVR is monitored for proper data being latched. For one pulse, shorten the time at which RCVINA's negative transition occurs. Check RCVR if the short pulse was latched. Restabilize the VCO with normal pulses. Input another short pulse. Continue this routine, while gradually shortening the pulse, until the data is not latched. The time between this negative transition and the midpoint of the original pulse's uptime is t_{se}. Repeat this procedure using all of the RCVINA waveforms shown.

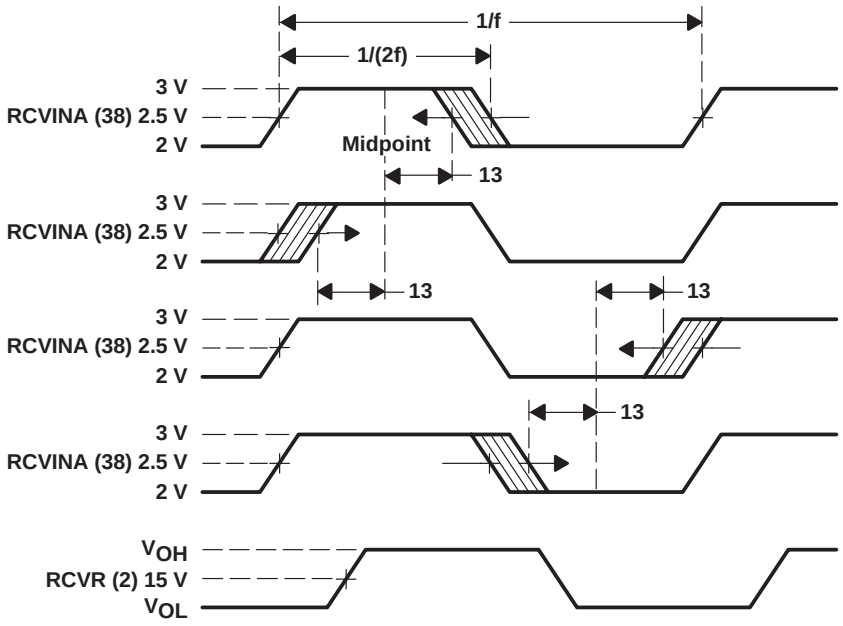


Figure 13. TMS38054 Phase Locked to RCVINA

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

energy detect (REDY) (see Figure 8 and Note 17)

NO.			TEST CONDITIONS	MIN	MAX	UNIT
14	$t_{d(REDYHL)}$	Delay time, FRAQ transition to REDY low again	Data transition density = 100%, See Figure 14	2		µs
			Data transition density = 33%, See Figure 14	6	100	
15	$t_{d(REDYH)}$	Delay time, data loss to REDY high	Data transition density changes 100% to 2.5%, See Figure 15	20	100	µs

NOTE 17: The transition density of the incoming data is the percentage of transitions of the incoming data as compared to the maximum possible number of transitions. For a string of Manchester-encoded 0 data, 100% transition density is a 16-MHz signal at a 16-Mbps data transmission rate.

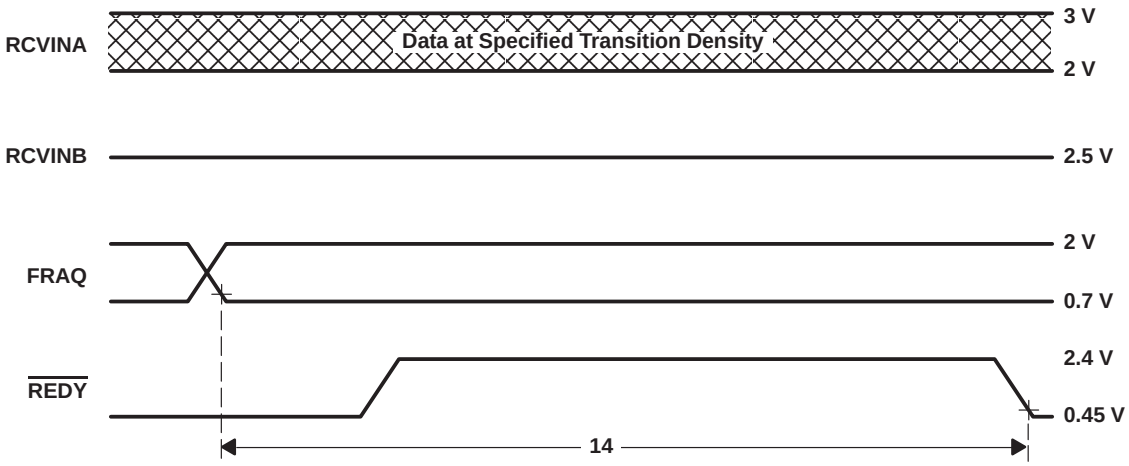


Figure 14. Timing Waveforms for Energy-Detect, FRAQ to REDY Timing

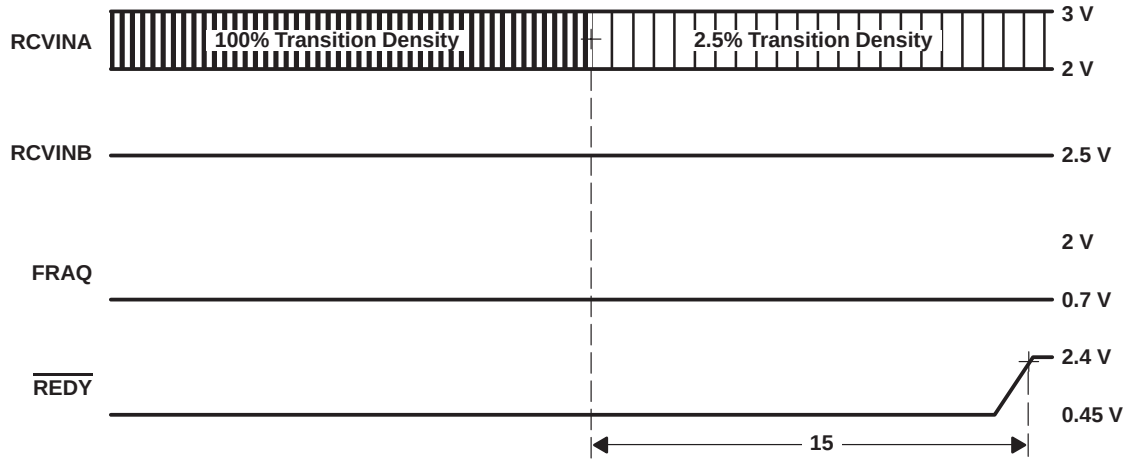


Figure 15. Timing Waveforms for Energy-Detect to Energy-Loss Timing

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

watchdog timer (see Figures 16 and Notes 9, 18, 19, 20)

NO.			TEST CONDITIONS	MIN	MAX	UNIT
16	$t_{d(WDT)H}$	Delay time, watchdog-timer expiration	C_{wdt} = 1.5 µF, $R_{L1} = R_{L2}$ = 2.9 kΩ	21	50	ms

NOTES: 9. R_{L1} is connected from PHOUTA to ground; R_{L2} is connected from PHOUTB to ground.
18. To enable the phantom-driver signals, $\overline{\text{NRST}}$ must be toggled high with a maximum 20-ms period (50-Hz repetition rate). Phantom-driver signals are assured to be disabled if $\overline{\text{NRST}}$ does not toggle for 50 ms. The '380C2x software ensures a maximum 20-ms period toggling rate for the insertion condition.
19. Pulse duration high of $\overline{\text{NSRT}}$ is not critical, but it is recommended that it be at least 125 ns.
20. C_{wdt} is the capacitor connected from WDTCAP to GND.

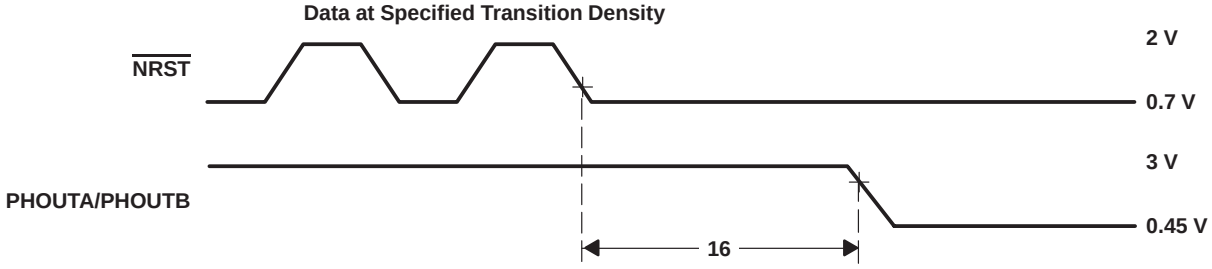
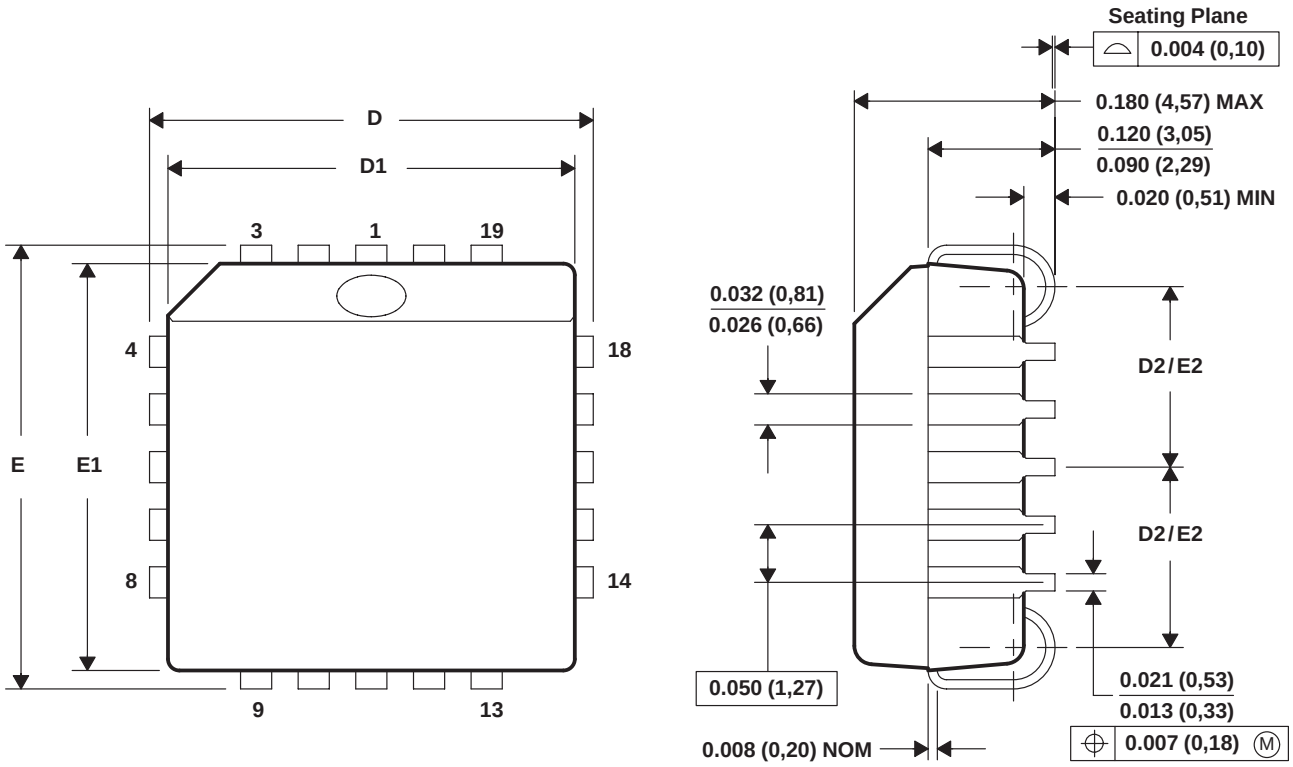


Figure 16. Watchdog-Timer Expiration Waveforms

MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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