

74LS01 Gate

Quad Two-Input NAND Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS01	16ns	1.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS01N
Plastic SO	N74LS01D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

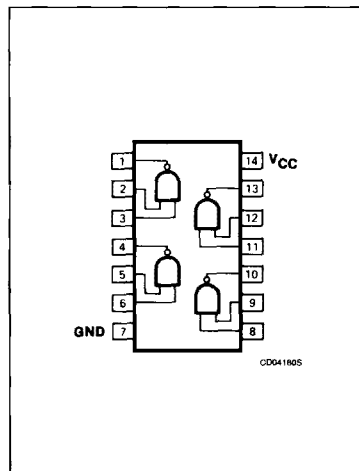
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
A, B	Inputs	1LSul
Y	Output	10LSul

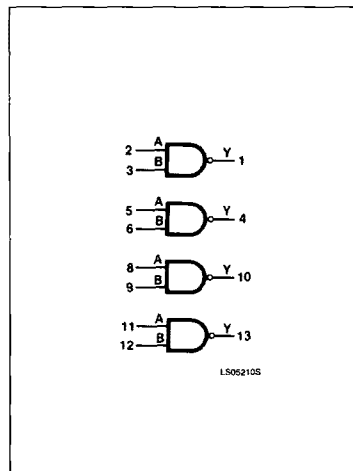
NOTE:

Where a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{OL}$.

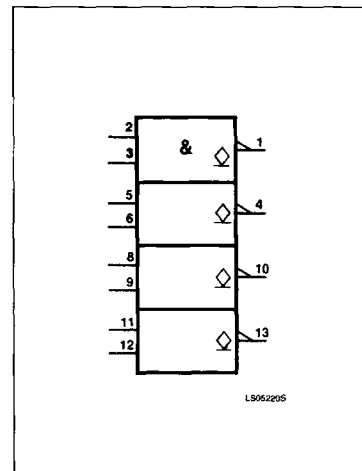
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74LS01

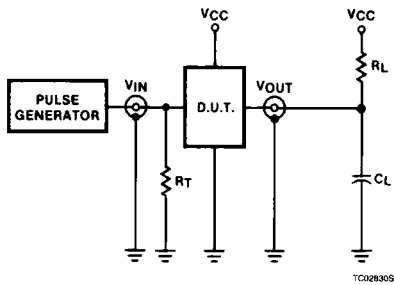
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

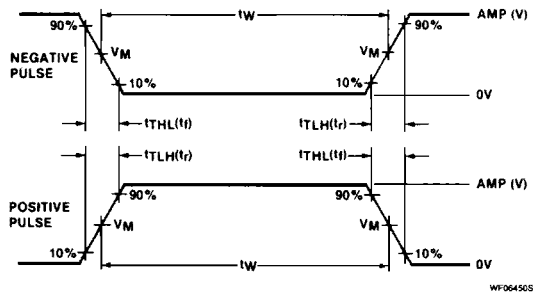
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
V _{OH} HIGH-level output voltage			5.5	V
I _{OL} LOW-level output current			8	mA
T _A Operating free-air temperature	0		70	°C

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

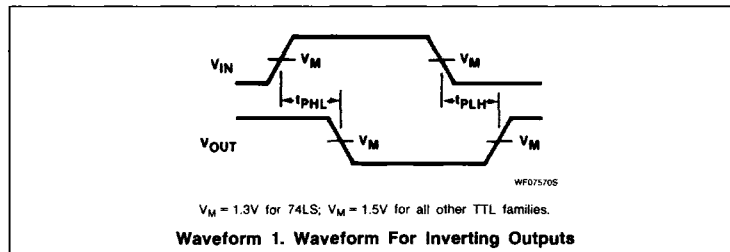
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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS01			UNIT	
		Min	Typ ²	Max		
I_{OH}	HIGH-level output current $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$			100	μA	
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$		0.35	0.5	V
		$I_{OL} = 4\text{mA}$		0.25	0.4	V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_i = I_{IK}$			-1.5	V	
I_i	Input current at maximum input voltage $V_{CC} = \text{MAX}, V_i = 7.0\text{V}$			0.1	mA	
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}, V_i = 2.7\text{V}$			20	μA	
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}, V_i = 0.4\text{V}$			-0.4	mA	
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}$	I_{CCH}	Outputs HIGH	0.8	1.6	mA
		I_{CCL}	Outputs LOW	2.4	4.4	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM**AC ELECTRICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1		32 28	ns