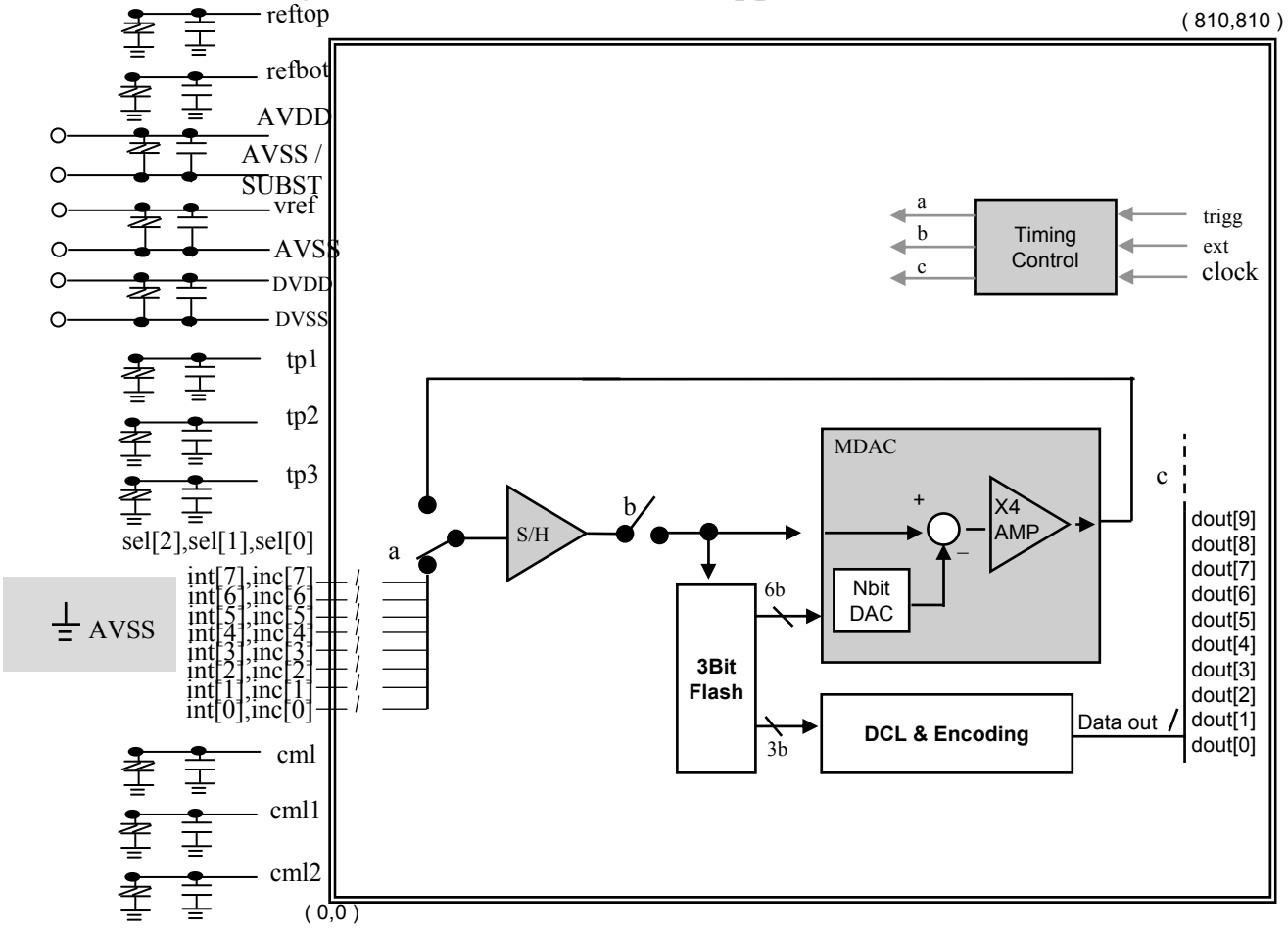
1. General Description

H18GAD42H is a 10bit CMOS (0.18㎛ ASIC, Single poly, Quadruple metal, MIM) Analog-to-Digital converter (ADC) for industry. This ADC cell adopts algorithmic method which makes implementation able simply.

2. Features

- Algorithmic method
- Resolution : 10bits
- Maximum Clock frequency : 10MHz
- Conversion Rate : Max 2MHz
- Power supply : 3.3V
- Power Dissipation : 17mW (@clock 10MHz)
- Process : 0.18㎛ CMOS generic process (1-poly, 4-metal, MIM)
- Library Layout Size : 810㎛ x 810㎛ (without PAD)

3. Block Diagram with Recommended Application Circuit



4. Pin Descriptions

Name	Type	Description
AVDD	power	Analog power
AVSS	ground	Analog ground
SUBST	ground	Substrate bias (Analog ground)
vref	power	Analog power(nominally AVDD)
sel[2]~sel[0]*	input	Analog input channel selection
int[0]~int[7]	input	Analog input channels(positive)
inc[0]~inc[7]	input	Analog input channels(negative)
clock	input	Clock input
ext	input	Resolution selection (nominally L)
trigg	input	Trigger for ADC(nominally H)
reftop	input / output	Reference top(cml+0.6;2.25V)
refbot	input / output	Reference bottom(cml-0.6;1.05V)
tp1	output	Analog test pin1
tp2	output	Analog test pin2
tp3	Input /output	Analog test pin3
cml	output	Common mode level(AVDD/2)
cml1	output	Common mode level1
cml2	output	Common mode level2
DVDD	power	Digital power
DVSS	ground	Digital ground
dout[9]~dout[0]	output	Digital outputs

* 000 for Analog input channel 0 (int[0],inc[0])

5. Function Description

The operation of the multi-channel algorithmic ADC is as follows.

With trigg signal, S/H(Sample-and-Hold Amplifier) samples external differential input voltage through the selected one out of 8 input channels(int[0],inc[0]~int[7],inc[7]) by switch a. While the sampled voltage is held on the output of S/H via switch b, 3Bit Flash encodes the held voltage level digitally. The MDAC subtracts analog value of this digital code from the S/H output and multiplies the result by 4. The output of the MDAC is sampled by S/H via switch a.

This procedure is repeated for 5 times to get final 10 bit output.

6. Operating Conditions

Normal Operation

• vref = 3.3 V(= AVDD)
• int[0],inc[0]~int[7]inc[7] Max amplitude = 2.4 Vp-p

• Common Mode Level cml = 1.65 V normally and generated internally.
cml1 = 1.95 V normally and generated internally.
cml2 = 1.35 V normally and generated internally.

• Test Pins for Bias : tp1 = 2.1 V normally and generated internally.
tp2 = 2.1 V normally and generated internally.
tp3 =

• Reference Top = 2.25 V normally and generated internally.
• Reference Bottom = 1.05 V normally and generated internally.

• Input Selection	sel[2]	sel[1]	sel[0]
int[0],inc[0]	0	0	0
int[1],inc[1]	0	0	1
int[2],inc[2]	0	1	0
int[3],inc[3]	0	1	1
int[4],inc[4]	1	0	0
int[5],inc[5]	1	0	1
int[6],inc[6]	1	1	0
int[7],inc[7]	1	1	1

Symbol	Parameter	Min.	Typ.	Max.	Unit	
AVDD	Power Supply	3.0	3.3	3.6	V	
DVDD		3.0	3.3	3.6	V	
(DVSS-AVSS)				100	mV	
int[0],inc[0] ~ int[7],inc[7]	8 CH differential inputs	Described above			V	
Top	Operation Temperature	0	25	70	℃	
vref	Bias Current Control Voltage		3.3		V	
tp1, tp2	Bias Test Pins		2.1		V	
clock	System Clock		10		MHz	
trigg	A/D Conversion Trigger Signal	H for continuous operation				
ext	A/D Resolution Control Signal	LOW				

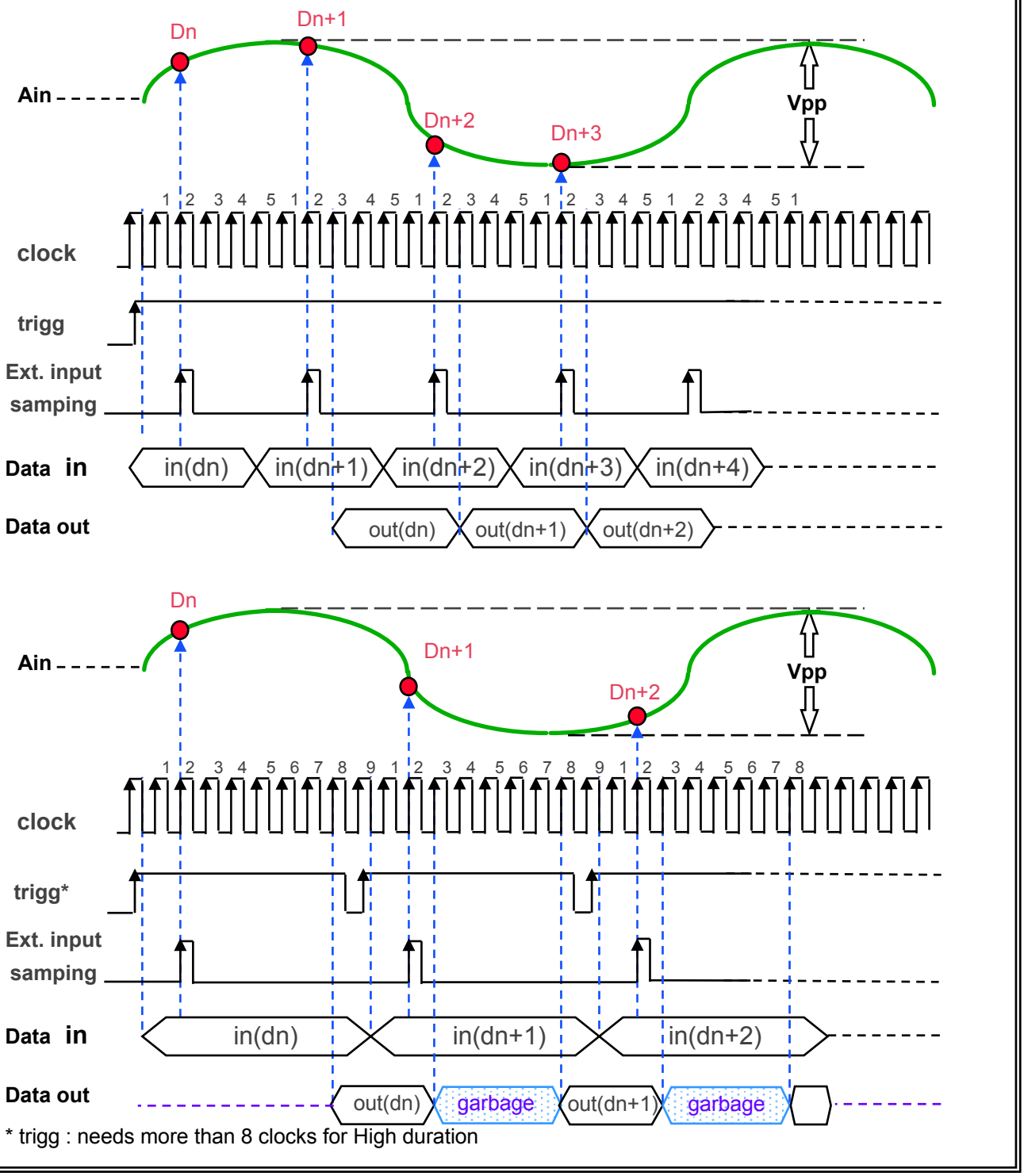
7. Electrical Characteristics

(Temp = 25 ℃ DVDD = 3.3V AVDD = 3.3V
clock = 10MHz RL = Ω) unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ain	Analog Input Range	Differential Input		2.4		Vp-p
clock	Clock Frequency			10		MHz
Fc	Conversion Rate	clock / 5		2		MHz
Idd	Current Consumption	Ain = 1 ~ 2V (clock = 10 MHz)		5		mA
INL	Integral Non Linearity	Ain = 1 ~ 2V (Fin = 1KHz)		1.0		LSB
DNL	Differential Non Linearity			0.5		LBS
SNR	Signal to Noise Ratio	Ain = 1 ~ 2V (Fin = 1MHz)		50		dB
SNDR	Signal to Noise plus Distortion Ratio					dB
SFDR	Spurious Free Dynamic Range					dBc
THD	Total Harmonic Distortion					dB

* SNDR, SFDR and THD are the specs for the internal tests.

8. Timing Diagram



* trigg : needs more than 8 clocks for High duration