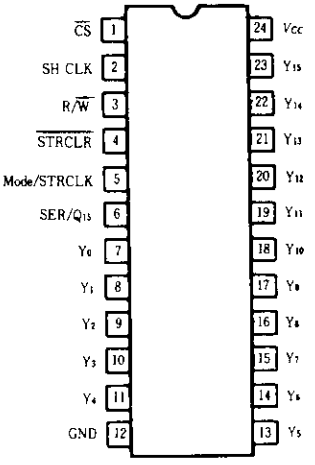
HD74HC673 ● 16-bit Shift Register

The HD74HC673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (data I/O) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-select ($\overline{CS}$) input disables both the shift-register clock and the storage register clock and places the data I/O in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

■ PIN ARRANGEMENT



(Top View)

■ FEATURES

- High Speed Operation :tpd (MODE/STRCLK to Y)=23ns typ.(C_L=50pF)
- High Output Current: Fanout of 15 LSTTL Loads (Q15 output)
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

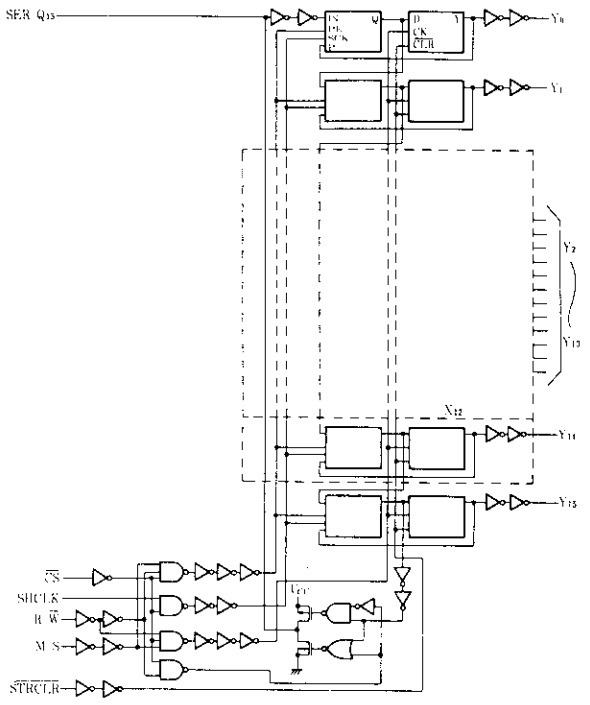
■ FUNCTION TABLE

Inputs					SER/ Q15	Shift Register Functions				Storage Register Functions	
$\overline{CS}$	R/$\overline{W}$	SHCLK	$\overline{STRCLR}$	Mode/ STRCLK		Shift	Read from Serial Output	Write into Serial Input	Parallel Load	Clear	Load
H	X	X	X	X	Z	No	No	No	No		No
X	X	X	L	X						Yes	
L	L	↓	X	X	Z	Yes	No	Yes	No		
L	H	X	X	X	Q15		Yes	No			No
L	H	↓	X	L	Q14n	Yes	Yes	No	No		No
L	H	↓	L	H	L	No	Yes		Yes	Yes	No
L	H	↓	H	H	Y15n	No	Yes		Yes	No	No
L	L	X	H	↑	Z		No		No	No	Yes

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	V_{CC}	−0.5~+7.0	V
Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Output Current	I_{OUT}	±35	mA
DC Current Drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Power Dissipation per Package	P_T	500	mW
Storage Temperature	T_{stg}	−65~+150	°C

LOGIC DIAGRAM



DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Input Voltage	V_{IH}	2.0			1.5	–	–	1.5	–	V
		4.5			3.15	–	–	3.15	–	
		6.0			4.2	–	–	4.2	–	
	V_{IL}	2.0			–	–	0.5	–	0.5	V
		4.5			–	–	1.35	–	1.35	
		6.0			–	–	1.8	–	1.8	
Output Voltage	V_{OH}	2.0	Q_{15} $V_{in}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	1.9	2.0	–	1.9	–	V
		4.5			4.4	4.5	–	4.4	–	
		6.0			5.9	6.0	–	5.9	–	
		4.5		$I_{OH}=-6mA$	4.18	–	–	4.13	–	
		6.0		$I_{OH}=-7.8mA$	5.68	–	–	5.63	–	
	V_{OL}	2.0	Q_{15} $V_{in}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	–	0.0	0.1	–	0.1	V
		4.5			–	0.0	0.1	–	0.1	
		6.0			–	0.0	0.1	–	0.1	
		4.5		$I_{OL}=6mA$	–	–	0.26	–	0.33	
		6.0		$I_{OL}=7.8mA$	–	–	0.26	–	0.33	
Output Voltage	V_{OH}	2.0	$Y_0\sim Y_{15}$ $V_{in}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	1.9	2.0	–	1.9	–	V
		4.5			4.4	4.5	–	4.4	–	
		6.0			5.9	6.0	–	5.9	–	
		4.5		$I_{OH}=-4mA$	4.18	–	–	4.13	–	
		6.0		$I_{OH}=-5.2mA$	5.68	–	–	5.63	–	
	V_{OL}	2.0	$Y_0\sim Y_{15}$ $V_{in}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	–	0.0	0.1	–	0.1	V
		4.5			–	0.0	0.1	–	0.1	
		6.0			–	0.0	0.1	–	0.1	
		4.5		$I_{OL}=4mA$	–	–	0.26	–	0.33	
		6.0		$I_{OL}=5.2mA$	–	–	0.26	–	0.33	
Off-state Output Current	I_{OZ}	6.0	$V_{in}=V_{IH}$ or V_{IL}, $V_{out}=V_{CC}$ or GND		–	–	±0.5	–	±5.0	μA
Input Current	I_{in}	6.0	$V_{in}=V_{CC}$ or GND		–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{in}=V_{CC}$ or GND, $I_{out}=0\mu A$		–	–	4.0	–	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	27	—	21	
		6.0		—	—	32	—	25	
Propagation Delay Time	t_{PHL}	2.0	$\overline{STRCLR}$ to Y	—	—	200	—	250	ns
		4.5		—	23	40	—	50	
		6.0		—	—	34	—	43	
	t_{PLH} t_{PHL}	2.0	Mode/STRCLK to Y	—	—	200	—	250	ns
		4.5		—	23	40	—	50	
		6.0		—	—	34	—	43	
	t_{PLH} t_{PHL}	2.0	SH CLK to SER/Q_{15}	—	—	200	—	250	ns
		4.5		—	19	40	—	50	
		6.0		—	—	34	—	43	
Output Enable Time	t_{ZH} t_{ZL}	2.0		—	—	150	—	190	ns
		4.5		—	—	30	—	38	
		6.0		—	—	26	—	33	
Output Disable Time	t_{HZ} t_{LZ}	2.0		—	—	150	—	190	ns
		4.5		—	—	30	—	38	
		6.0		—	—	26	—	33	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	6	—	20	—	
		6.0		14	—	—	17	—	
Setup Time	t_{su}	2.0	SER/Q_{15} to SH CLK	100	—	—	125	—	ns
		4.5		20	1	—	25	—	
		6.0		17	—	—	21	—	
	t_{su}	2.0	$\overline{CS}$ to R/$\overline{W}$	100	—	—	125	—	ns
		4.5		20	7	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0	SH CLK to SER/Q_{15}	5	—	—	5	—	ns
		4.5		5	0	—	5	—	
		6.0		5	—	—	5	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0	6 Pin	—	—	60	—	75	ns
		4.5		—	4	12	—	15	
		6.0		—	—	10	—	13	
	t_{TLH} t_{THL}	2.0	Other Pins	—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF