QUALITY SEMICONDUCTOR, INC.

10BaseT/100BaseTX Ethernet MII Transceiver for Category 5 Twisted Pair Cable

QS6612

PRELIMINARY

FEATURES/BENEFITS

- Single chip 5V 10BaseT/100BaseTX transceiver with MII interface and Auto-Negotiation
- Built-in transmit wave-shaping, receive filters and adaptive equalization eliminates the need for external filters
- Built-in 10BaseT and 100BaseTX multiplexing eliminates external relays or switches
- High speed Phase Lock Loop for low-jitter clock recovery
- Requires one external 25MHz crystal only
- 10BaseT/100BaseTX half- and full-duplex operation
- Low latency bit budget supports type II repeater design for MII or symbol wide interfaces
- 25MHz free-running clock output for controller
- IEEE 802.3u compliant MII and Serial Management standard interface
- IEEE 802.3u compliant Auto-Negotiation for auto 10/100Mbps speed selection
- 4B/5B Encoder/Decoder and Stream Cipher Scrambler/Descrambler for 100BaseTX
- Programmable scrambler seed reduces EMI in multi-port repeater design
- Manchester ENDEC and 10BaseT
- Optional symbol wide interface
- MLT-3 transceiver with DC restoration for baseline wander compensation for 100BaseTX-mode
- PHY isolate, local/remote loop-back, and 4 LED drivers
- Full CMOS with low power requirements
- Small footprint 64-pin LQFP (10x10x1.4mm) package

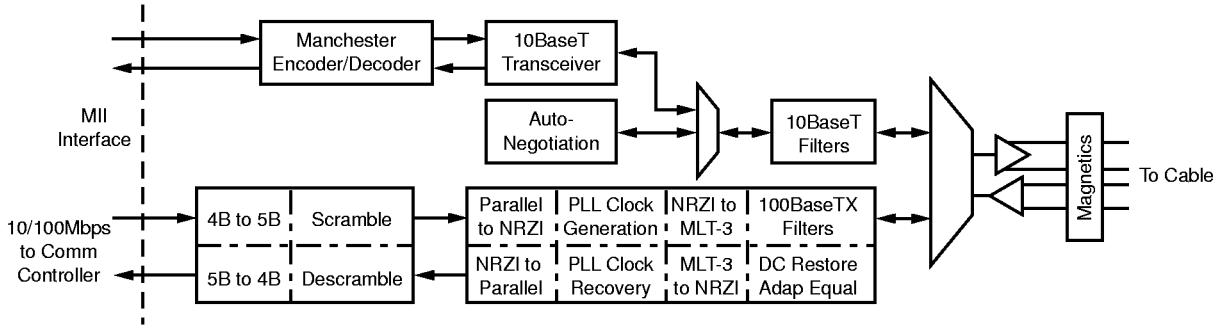
DESCRIPTION

The QS6612 provides all of the IEEE 802.3u 100BaseTX and ISO 8802-3 10BaseT Physical Layer (PHY) functions needed for most workstations, hubs, bridge, router, and switch applications. It can operate as a 100Mbps only device, or as a dual speed 10/100Mbps device with built-in Auto-Negotiation for speed selection. The QS6612 supports the standard Media Independent Interface (MII) for glueless interface with 10/100 Ethernet Media Access Controllers (MAC), or MII-based repeaters. The QS6612 supports an optional symbol wide interface for Type II repeater applications.

The MII supports a 25MHz transfer rate for 100BaseTX and 2.5MHz transfer rate for 10BaseT. The built-in IEEE 802.3u Auto-Negotiation feature automatically selects internal 10BaseT or 100BaseTX, full or half-duplex, as a result of negotiation between the station and its link partner.

The QS6612 supports half and full-duplex operation at both 10Mbps and 100Mbps speeds. It complies with ANSI X3T9 TP-PMD and includes MLT-3 Encoder/Decoder and Stream Cipher scrambler/de-scrambler functions for 100BaseTX. The QS6612 supports Category 5 Unshielded Twisted Pair and Type 1 Shielded Twisted Pair wiring. The on-chip Serial Management Interface features the Basic and Extended register set. The 4B/5B Encoder and Decoder are also included.

Figure 1. Functional Block Diagram



The QS6612 includes clock generation and clock recovery circuits for both 10BaseT and 100BaseTX and requires only one external 25MHz clock source or crystal. All the clock generation and recovery PLL components are built in to reduce external components and improve noise immunity.

The QS6612 includes the MLT-3 transceiver with built-in DC restoration. This feature eliminates the baseline wander problem associated with some 100BaseTX data patterns. The built-in adaptive equalizer automatically compensates for signal roll-off for various cable lengths and eliminates the need for external equalization.

The built-in transmit wave-shaping and multiplexing of the 10BaseT and 100BaseTX drivers eliminate the need for external filters and relays in 10/100Mbps applications, and provide for a direct connection to a single isolation transformer and common mode choke. The need for expensive magnetic hybrids containing filters is thus eliminated.

The QS6612 has various modes of operation to support a variety of repeater designs. The MII interface supports MII based repeater controllers with multiple QS6612 based ports bussed on the MII. The low bit budget design of the QS6612 enables the design of a MII Type II repeater. The symbol interface is also suitable for Type II repeater designs with multiple QS6612 devices on the same symbol-wide bus.

In addition to Auto-Negotiation for speed selection, the QS6612 can be operated at either 10Mbps or 100Mbps by hardware mode or software control.

The QS6612 provides various diagnostics features. It includes four outputs to directly drive four LEDs. It features local and remote loop-back for board level diagnostics. The PHY isolate feature allows for isolation of the QS6612 when multiple transceivers are bussed together.

The QS6612 is manufactured in a low power, sub-micron, all CMOS process to minimize the power consumption and heat dissipation. The part is thus suitable for multi-port repeaters and PCMCIA as well as CardBus designs.

APPLICATION

The QS6612 is suitable for use in virtually any 100BaseTX or 10BaseT/100BaseTX application, full- or half-duplex, including adapter cards, repeaters (Classes I and& II), bridges, switches, routers and gateways. A few examples are shown in this section.

Figure 2 and Figure 3 illustrate general methods of connecting a QS6612 to the system and network. Figure 2 shows connection to a 10/100BaseTX system with Auto-Negotiation. In this application, the QS6612 transfers data to and from the MAC over its 4-bit wide MII interface. Connection to the network requires only a single set of magnetics since the QS6612 multiplexes both 10 and 100 functions into the same physical port.

Figure 3 shows a QS6612 connected to a 100BaseTX-only Class II repeater via its symbol (5-bit wide) interface, and to the network via a set of magnetics and an RJ45-8 connector.

Figure 2. QS6612 in a 10/100BaseTX System Using the MII Interface

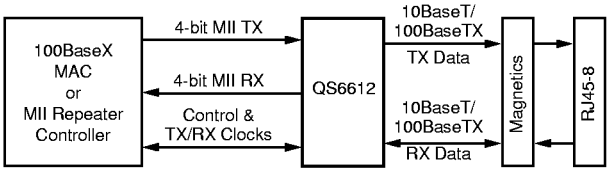
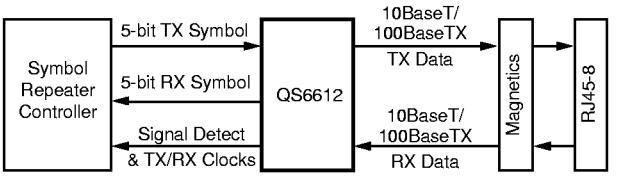


Figure 3. QS6612 in a 100BaseTX-only Class II Repeater System Using the Symbol Interface



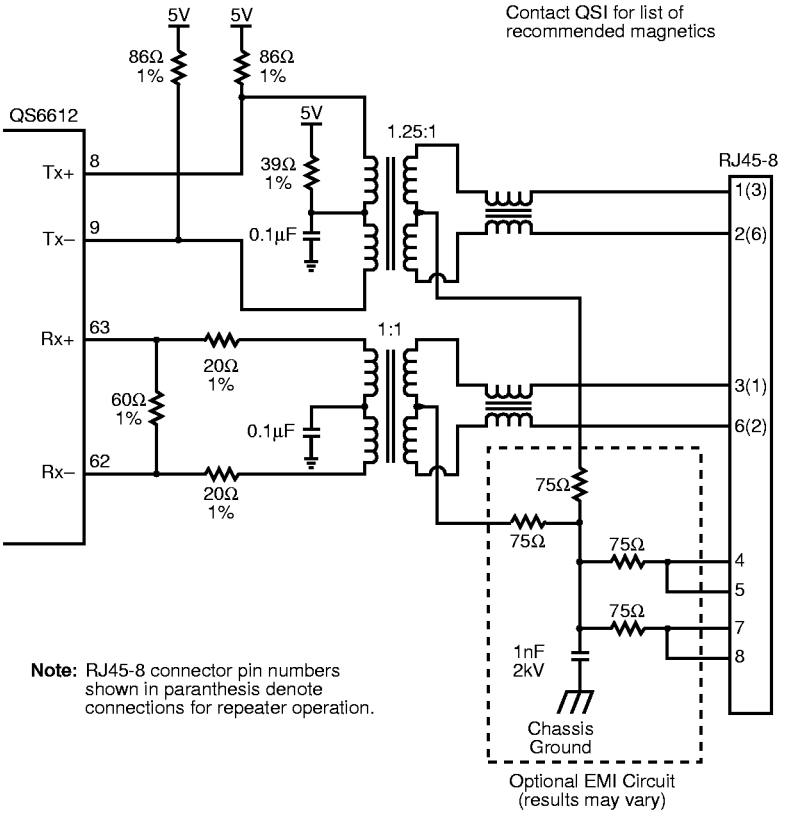
10BaseT/100BaseTX MAGNETICS CONNECTIONS

Figure 4 illustrates connection of the QS6612 to its magnetics and a Cat-5 UTP cable through an RJ45 connector. The QS6612 provides switching for the built-in 10BaseT transceiver, and performs signal buffering and filtering for 10BaseT Manchester-encoded signaling. As a result, common magnetics can be used for both 10BaseT and 100BaseTX transmission modes.

The pin numbers of the RJ45 connector not shown in paranthesis in Figure 4 apply for MAC-based applications for 100BaseTX systems as well as dual-speed 10/100BaseTX systems, both full-duplex and half-duplex, including adapters and switches.

The pin numbers in paranthesis apply to repeater operation. The Optional EMI Circuit may reduce EMI if the transformer is designed to work with the termination network shown. It may increase EMI if the transformer is not so designed. Use caution when designing-in this circuit.

Figure 4. 10BaseT/100BaseTX Cable Connection



Connections

RJ45 pin assignments for MAC and repeater operation are summarized in Table 1.

Table 1. RJ45-8 Connector Pin Assignments

100BaseTX/10BaseT Signals	Pin Numbers	
	MAC Applications	Repeater Applications
Transmit Pair	1 (TX+) and 2 (TX–)	3 (TX+) and 6 (TX–)
Receive Pair	3 (RX+) and 6 (RX–)	1 (RX+) and 2 (RX–)
Unused Pair	4/5, 7/8	4/5, 7/8

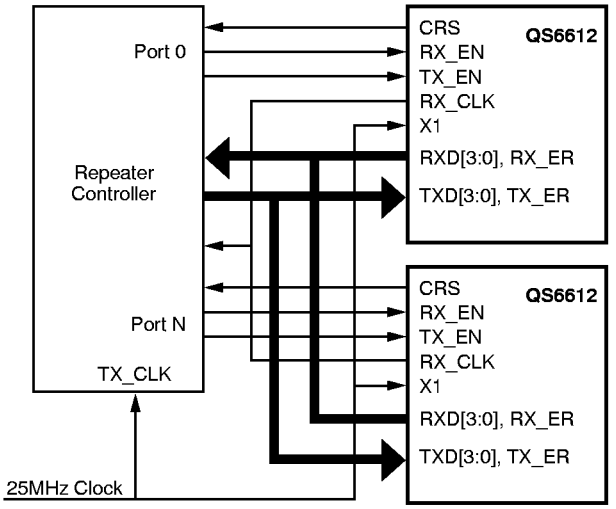
MAC-Based System Applications

Many of the Fast Ethernet MACs interface to the PHY Layer through the industry-standard Media Independent Interface (MII). The QS6612 has this interface, and can therefore interface gluelessly to MII controllers. The controller device may be configurable for 100BaseTX/FX only, or for dual-speed 10BaseT/100BaseTX/FX.

Repeater-Based System Applications

The QS6612 can be used in the design of different types of repeaters in conjunction with repeater controller ICs that provide MII or symbol-wide interface to multiple PHYs via a bus architecture as shown in Figure 5 below.

Figure 5. Repeater Application Using MII or Symbol-Wide Buss



The QS6612 is configured in 100BaseTX repeater mode by setting the MODE pins to 101. In this architecture, one QS6612 is required per port. The repeater controller can support MII signals or symbol-wide signals. If a symbol-wide interface is used, the QS6612 must be configured with PCSEN disabled. In this mode the data is a 5-bit wide symbol and is carried over RXD[3:0], RX_ER and TXD[3:0], TX_ER.

The QS6612 does not 4B/5B encode/decode, nor does it scramble/de-scramble, nor does it detect and generate JK or TR symbols for the Start or End of Frame. This mode is used to save a few delay clocks in the repeater path to accommodate symbol-wide repeater chips. If PCSEN is enabled, the QS6612 performs the full encode/decode, scramble/de-scramble, and JK/TR generation and detection. This mode is used with MII repeater chips and can support Type I or Type II repeater designs. The RXD[3:0] and TXD[3:0] signals carry the data.

In either mode all the TXD[3:0] and RXD[3:0] signals are respectively bussed together. Each port has separate CRS and RX_EN lines to signal receive activity on that port. The Repeater Controller enables the receiving port by activating the RX_EN of the corresponding QS6612. The Repeater Controller receives the data over the RXD lines and repeats the data over the TXD lines. The Repeater Controller activates the TX_EN lines of all the QS6612 (except for the receiving port) to enable them to transmit the repeated data. A collision is detected by the Repeater Controller when multiple CRS signals are active. In that case the Repeater Controller sends the jam pattern over all the ports on the TXD bus by enabling the TX_EN of all ports.

In repeater mode the CRS and the LED_ACT pins are activated on data reception only.

An external 25MHz source supplies the clock reference to the QS6612 devices and the TXC25 of the repeater controller.

Implementing a 100BaseFX repeater can be accomplished by setting the MODE pins to 000. The MODE pin settings of 000 disable Auto-Negotiation as required for FX operation and allows for a half-duplex connection as required for repeater designs.

General 10/100BaseTX Notes

The following contains application notes regarding the basic connections of the QS6612 when used in 10/100BaseTX systems.

Power Connections

Figure 6 shows the power connections. Refer to "QS6612 Layout Guidelines" for the latest component values and layout recommendations.

10/100BaseTX Transmit Operation

The transmit transformer recommended for use with the QS6612 has a step-down winding ratio of 1.25:1, with a center tap on its secondary winding (cable side) as shown in Figure 4. With this transformer, the recommended values for the pull-up resistors from the TX± pins to the 5V supply is 86Ω and the value of the resistor connected between the IREF pin and ground should be 4.53kΩ as shown in Figure 6.

The transmit output of the QS6612 in a 100BaseTX operation is nominally a 1.25V peak differential signal. When used in 10BaseT mode, the QS6612 10BaseT driver produces a differential signal with peak amplitude of 3.125V. These signals, when coupled over the 1.25:1 isolation transformer, are reduced to peak differential voltages of 1.0V and 2.5V respectively at the cable end, due to the step-down characteristic of the transformer.

10/100BaseTX Receive Operation

The QS6612 RX± input pins are self-biasing and can receive 1) MLT-3 100BaseTX data, or 2) Manchester-encoded 10BaseT data, and 3) Fast Link Pulse and Normal Link Pulse signaling for Auto-Negotiation. The magnetics used for receiving is a 1:1 transformer with center tap on the cable side. A combined 100Ω resistive termination is used to match the CAT-5 UTP cable impedance. This is fulfilled with the combination of two 20Ω resistors and a 60Ω resistor as shown in Figure 4. The QS6612 RX± input receive signal appears across the 60Ω resistor, which provides about 60% of the signal appearing at the transformer windings. The 0.01µF capacitor provides common mode filtering to decrease noise susceptibility.

For the receiver, the transformer winding ratio is 1:1, so there is no voltage step up or step down.

Figure 6. Power Connections for QS6612 Typical Application

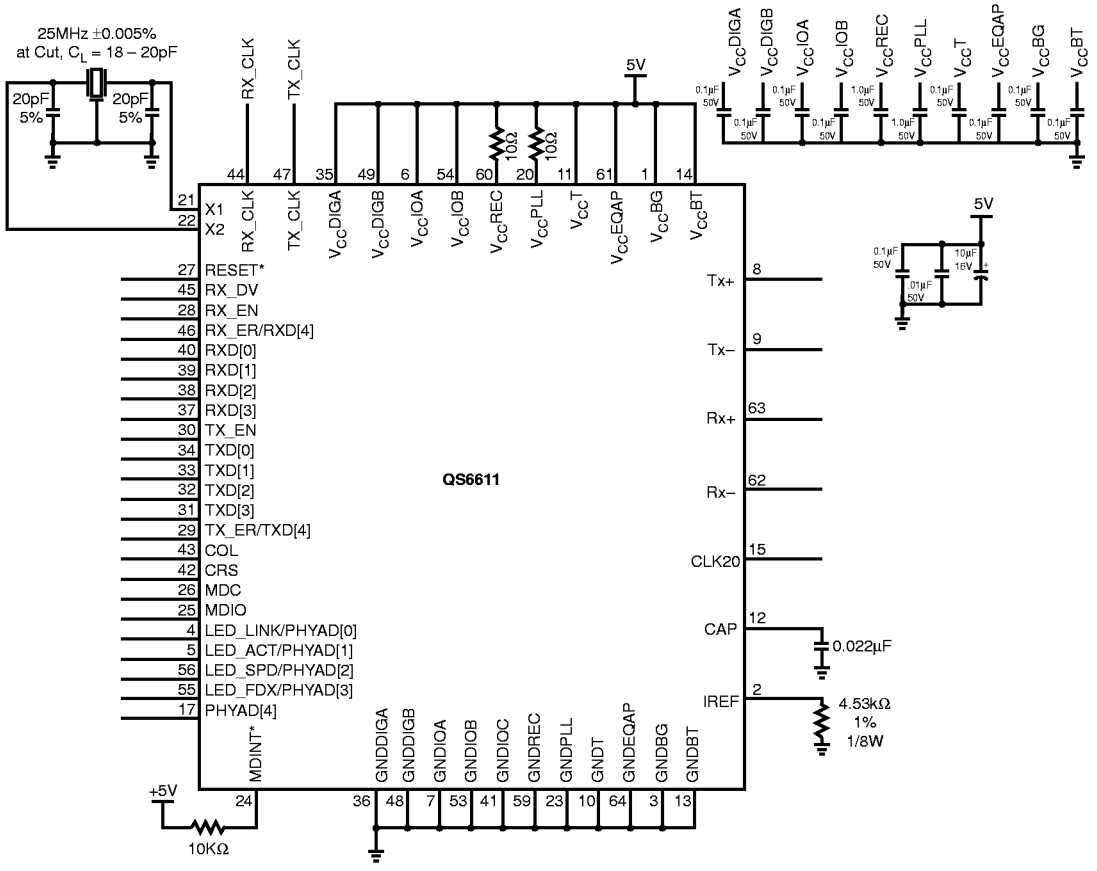
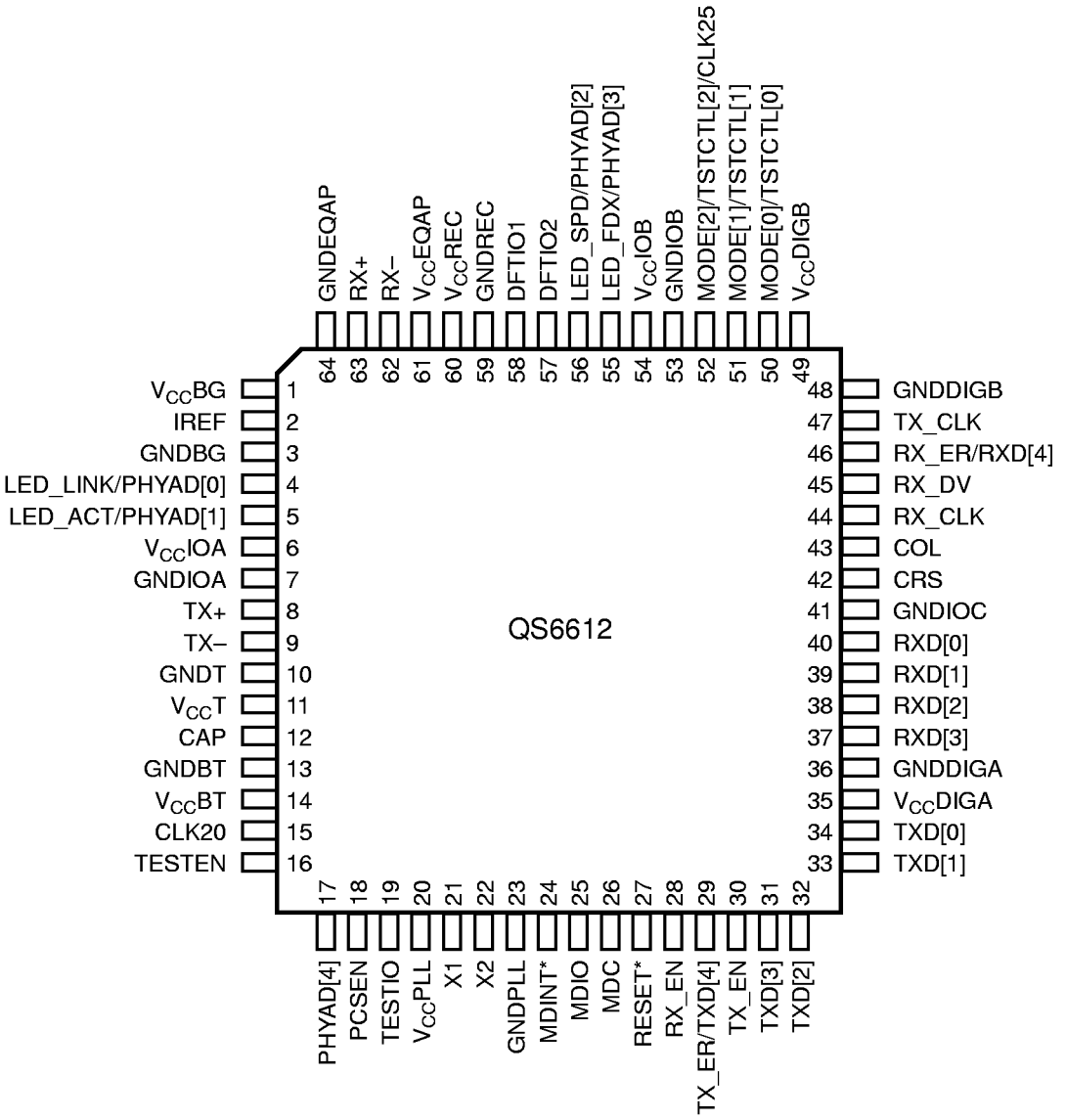


Figure 7. Pin Assignment



In the following tables , all signals are active HIGH signals except for those ended with a '*'. A signal which is tri-stateable is denoted with a '†' symbol appended to its I/O Type. A signal with a built-in 100KΩ pull-up is denoted by a '↑' symbol and a signal with a built-in pull-down is denoted by a '↓' symbol.

Table 2. Pin Descriptions — MII Signal (18)

Signal Name	Type	Pin No.	Description
TX_CLK	O, †	47	MII Transmit clock output: • 25MHz in 100BaseTX mode • 2.5MHz in 10BaseT nibble mode • High impedance when PHY is isolated.
RX_CLK	O, †	44	MII Receive clock output: • 25MHz in 100BaseTX mode • 2.5MHz in 10BaseT nibble mode • High impedance when PHY is isolated or when RX_EN is de-asserted.
RXD[3:0]	O, †	37-40	MII Received data. Active high and driven synchronously from falling edge of RX_CLK. RXD[0] is LSB. High impedance when PHY is isolated or when RX_EN is de-asserted.
RX_DV	O, †	45	MII Receiver Data Valid. Active high and driven synchronously from falling edge of RX_CLK. This signal indicates that recovered and decoded data nibbles are being presented synchronously to RX_CLK. High impedance when PHY is isolated or when RX_EN is de-asserted.
RX_ER/ RXD[4]	O, †	46	Receiver error. Driven High synchronously from falling edge of RX_CLK when invalid symbol has been detected in 100BaseTX mode. In Type II Repeater mode, this output represents the high order bit of the 5-bit symbol code-group. This signal is ignored in 10BaseT operations. High impedance when PHY is isolated or when RX_EN is de-asserted.
COL	O, †	43	MII Collision detected. Active High. This signal is de-asserted in full-duplex operations. High impedance when PHY is isolated.
CRS	O, †	42	MII Carrier Sense. Active High. High impedance when PHY is isolated.
TXD[3:0]	I	31-34	MII Transmit data. TXD[0] is LSB. High impedance when PHY is isolated.
TX_EN	I/O	30	MII Transmit enable. When active (High), causes the transmit data TXD[3:0] to be encoded and scrambled for transmission. Use as an output for factory testing ONLY.
TX_ER/ TXD[4]	I/O	29	MII Transmit error. When active (High), causes the 4B/5B encode process to substitute the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in a 10BaseT operation. In symbol mode, this input represents the high order bit of the 5-bit symbol code-group. When this pin is not used it should be tied low via a 10kΩ resistor.
MDC	I	26	Serial management clock synchronous to the MDIO data interface.
MDIO	I/O, †	25	Serial management data input and output. This pin needs an external pull up.

Table 3. Pin Descriptions — 10/100 PHY Signals

Signal Name	Type	Pin No.	Description
RX±	I	63, 62	100BaseTX or 10BaseT differential receive inputs from magnetics.
TX±	O, †	8, 9	100BaseTX or 10BaseT differential transmit outputs to magnetics.
IREF	O	2	Reference resistor (4.53kKΩ ±1%) connection pin.
CAP	I	12	Capacitor. Nominal value is .022µF to ground.

Table 4. Pin Descriptions — System Clock Signals (2)

Signal Name	Type	Pin No.	Description
X1	I	21	25MHz clock reference input. This input is connected to one terminal of a 25MHz crystal or an external 25MHz clock source.
X2	O	22	25MHz crystal feedback. This output is connected to the other terminal of a 25MHz crystal. If X1 is driven with an external clock source, X2 must be left open.

Table 5. Pin Descriptions — Control Status Signals (17)

Signal Name	Type	Pin No.	Description
LED_LINK/ PHYAD[0]	I/O	4	Lights the LINK LED when a good link is detected. At reset, sampled as an input to set PHYAD[0] bit.
LED_ACT/ PHYAD[1]	I/O	5	Lights the Activity LED when transmitting or receiving. At reset, sampled as an input to set PHYAD[1] bit.
LED_SPD/ PHYAD[2]	I/O	56	Lights the SPEED LED when 100Mbps is selected. At reset, sampled as an input to set PHYAD[2] bit.
LED_FDX/ PHYAD[3]	I/O	55	Lights the FDX LED when in Full-duplex. At reset, sampled as an input to set PHYAD[3] bit.
PHYAD[4]	I/O, ↑	17	At reset, sampled as an input to set PHYAD[4] bit. This pin has an internal pull up.
PCSEN	I/O, ↑	18	At reset, sampled as an input. If strapped low, 5 bit (RXD[4:0] and TXD[4:0]) unscrambled data symbols appear over MII pins. If high, 4 bit MII data appear over MII pins. This pin has an internal pull up.
MDINT*	O, †	24	Active low signal used as an interrupt source indicating occurrence of one of several defined management functions. This pin needs an external pull up.
RESET*	I	27	Active low signal. It forces the device to a known state.
RX_EN	I, ↑	28	Active high to enable outputs of RXD[3:0], RX_ER, RX_CLK, RX_DV. Otherwise these outputs will be tri-stated. This pin has an internal pull up and can be left open for standard MII operation. Useful in repeater designs.
MODE[2:0]/ TSTCTL[2:0]/ CLK25	I/O, ↑	52-50	These pins carry encoded input signals that are latched into the QS6612 at power up/reset to set the mode of operation. If TESTEN is High, these pins are used for factory test. In normal operation, TESTEN is Low. A buffered 25MHz clock is available on MODE[2] after RESET. This pin has an internal pull-up.
TXC_SEL/ TESTIO	I, ↓	19	When TESTEN is active, a High input enables I/O Pin Mapping Test. A Low input enables Device Function Test. This pin has an internal pull down. When TESTEN is inactive, TXC_SEL High at the rising edge of reset selects TSCLK as the clock. When Low X1 is selected for TXCLK.
CLK20	I, ↑	15	For 10BaseT testing purposes, by writing '0' to Reg. 27.0, this pin becomes an input for an external 20MHz clock source for driving the transmit clock.
TESTEN	I, ↓	16	Tie high to enable factory test modes. Normal operation when low. This pin has an internal pull down.
DFTIO[2:1]	I/O	57, 58	Test I/O pins. For factory use only.

Table 6. Pin Descriptions — Power and Ground (21)

Signal Name	Type	Pin No.	Description
V_{CC}IOA	P	6	Digital 5V power supply for I/O.
GNDIOA	P	7	Digital ground for I/O.
V_{CC}IOB	P	54	Digital 5V power supply for I/O.
GNDIOB	P	53	Digital ground for I/O.
GNDIOC	P	41	Digital ground for I/O.
V_{CC}DIGA	P	35	Digital 5V power supply for logic.
GNDDIGA	P	36	Digital ground for logic.
V_{CC}DIGB	P	49	Digital 5V power supply for logic.
GNDDIGB	P	48	Digital ground for logic.
V_{CC}REC	P	60	5V power supply for clock recovery circuit.
GNDREC	P	59	Ground for clock recovery circuit.
V_{CC}PLL	P	20	Analog 5V power supply for 10 & 100 PLL clock synthesizer.
GNDPLL	P	23	Analog ground for 10 and 100 PLL clock synthesizer.
V_{CC}T	P	11	Analog 5V power supply for transmitter.
GNDT	P	10	Analog ground for transmitter.
V_{CC}EQAP	P	61	Analog 5V power supply for equalizer and adaptation circuit.
GNDEQAP	P	64	Analog ground for equalizer and adaptation circuit.
V_{CC}BG	P	1	Analog 5V power supply for band-gap circuit.
GNDBG	P	3	Analog ground for band-gap circuit.
V_{CC}BT	P	14	Analog 5V power supply for 10BT circuit.
GNDBT	P	13	Analog ground for 10BT circuit.

FUNCTIONAL DESCRIPTION

The QS6612 integrates 100BaseTX PCS, PMA, and PMD functions and the 10BaseT Manchester ENDEC and transceiver functions into a single chip for Ethernet 100Mbps and 10Mbps operation. It provides an IEEE802.3u compatible Media Independent Interface (MII) to communicate with an Ethernet Media Access Controller (MAC). Selection of 10Mbps or 100Mbps operation is based on settings of internal Serial Management Interface registers or determined by the on-chip Auto-Negotiation logic. The device can be set to operate either in full-duplex mode or in half-duplex mode in either 10Mbps or 100Mbps operation.

100BaseTX Transmit Function

The 100BaseTX QS6612 transmit function converts synchronous 4-bit data nibbles from the MII to a pair of 125Mbps differential serial data for transmitting over network twisted pair cables via an isolation transformer. Data conversion includes 4B/5B encoding, scrambling, parallel to serial, NRZ to NRZI, and MLT-3 encoding. The entire operation is synchronous to a 25MHz clock and a 125MHz clock, both of which are generated by an on-chip PLL clock synthesizer locked to an external 25MHz clock source.

4B/5B Data Translation

The transmit data, in 4-bit nibbles at 25MHz rate, is transferred from the MAC controller into the QS6612 via the MII TXD lines. The MAC controller asserts TX_EN during transmission, or forces an error in the encoded data using TX_ER.

The 4B/5B encoder replaces the first two nibbles of the preamble from the MAC frame with a /J/K/ code-group pair, Start-of-Stream Delimiter (SSD), following onset of TX_EN signal (refer to Appendix A for the 4B/5B code table). It appends to the end of the frame a /T/R/ code-group pair, End-of-Stream Delimiter (ESD), in place of the first two IDLE code-groups following negation of the TX_EN signal. The encapsulated data stream is converted from 4-bit nibbles to 5-bit code-groups (see Appendix A). During inter-packet gap (IPG) when no data is present, IDLE code-group is transmitted. When TX_ER is asserted while TX_EN is active, the Transmit Error code-group /H/ is substituted for the translated 5-bit code word.

4B/5B encoding is bypassed when bit 6 of Serial Management Register 31 is set to "1," or the PCSEN pin is strapped low.

Transmit Data Scrambling

During normal operation, the 5-bit transmit data stream is scrambled as defined by the TP-PMD Stream Cipher function. The Stream Cipher function minimizes the electromagnetic emission from the TP-PMD physical link. The scrambler encodes a plain text NRZ bit stream using a key stream periodic sequence of 2047 bits generated by the recursive linear function:

$$X[n] = X[n-11] + X[n-9] \text{ (modulo 2)}$$

When bit 0 of Serial Management Register 31 is set to "1," or the PCSEN pin is strapped low, the data scrambling function is disabled and the 5-bit data stream is clocked directly to the device's PMA sublayer.

The scrambler seed is partially dependent on the address latched into the QS6612 at power-up/reset on the PHYAD[0:4] pins so that different scrambled idle pattern data streams will be generated by each transmitter in multi-port repeaters to reduce EMI.

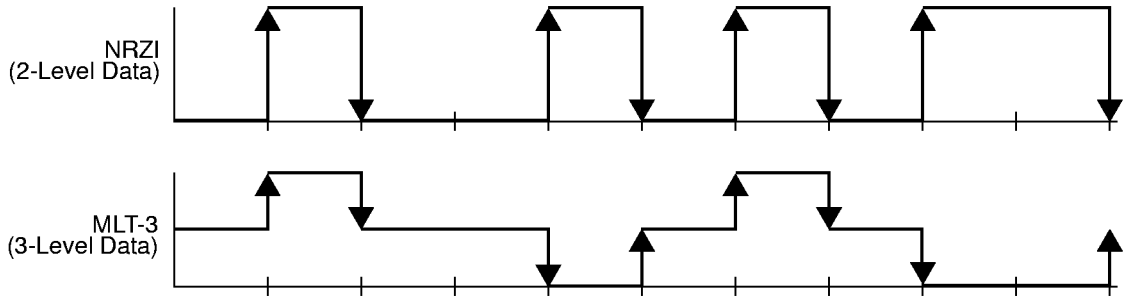
Parallel to Serial and NRZ to NRZI Conversion

NRZ data transmitted from the device's Physical Coding Sub-layer (PCS) in 5 bit code-group format is loaded into a shift register with a 25MHz clock, then clocked out with a 125MHz clock to convert it into a serial bit stream. Both clocks are generated by an on-chip clock synthesizer and are in sync to each other. The serialized data is further converted from NRZ to NRZI format, which produces a transition on every logic "1" and no transition on logic "0."

NRZI to MLT-3 Conversion

The QS6612 performs the NRZI to MLT-3 translation as defined in the TP-PMD specification. When electrical signals are transmitted over twisted-pair copper wire, the wire acts as an antenna and generates electromagnetic interference (EMI). As a two-level signal, NRZI encoding has a relatively large voltage transition which emits large amount of energy, making it difficult to meet FCC specifications for EMI. When NRZI data is MLT-3 encoded, frequency components of the signal are lowered, which results in a reduction of energy on the media in the critical frequency range of 20 to 100MHz. The effect offers a 3 to 6dB reduction in EMI emissions over an unconverted NRZI signal, thus increasing the margin of operation in respect to the FCC Class B limit.

Figure 8. NRZI to MLT-3 Conversion



The conversion from NRZI to MLT-3 is shown in Figure 8. Whenever there is a transition occurring in the NRZI data, there is a corresponding transition for MLT-3 data. For NRZI data, the count up/down direction changes after every transition. For MLT-3 data, it changes only after every two transitions, as presented in the figure.

Transmit Drivers

Unshielded twisted pair cable as used in 10BaseT and 100BaseTX systems is an extremely difficult medium with which to obtain low levels of radiated emissions. The absence of a grounded shield means that the cable will radiate unless the differential signal is symmetrical and contains very low levels of common-mode noise. A good transmit signal should have low skew and slow but symmetric rise/fall times. The QS6612 output waveform, for both 10BaseT and 100BaseTX operation, is digitally synthesized, resulting in closely matched and controlled rise/fall time to minimize presence of higher harmonic components in the waveform. The effect of this is a reduction of jitter in the output waveform and therefore external filtering requirements are no longer needed. These controlled transition times, in conjunction with the associated magnetics, result in typical rise/fall times of approximately 4ns, which are within the target range specified in the ANSI TP-PMD standard.

The individually wave-shaped 10BaseT and 100BaseTX transmit signals are multiplexed in the transmit output driver. This arrangement results in one device that uses the same external magnetics for both the 10BaseT and the 100BaseTX operating modes with a single configuration of RC components and connections. The transmit driver provides differential current at a suitable level for connecting directly to an external transformer that drives the twisted pair cable. Driver output current levels are set by a built-in band-gap reference and an external resistor connected to the IREF output pin. Each of the TX± outputs is a high output impedance open drain device.

100BaseTX Receive Function

The 100BaseTX receive function implements the reverse order functionality of the 100BaseTX transmit path. It includes a receiver with adaptive equalization and DC restoration, MLT-3 to NRZI conversion, data and clock recovery at 125MHz with a digital phase lock loop, NRZI to NRZ conversion, serial to parallel conversion, de-scrambling, and 5B to 4B decoding.

Receiver

The 100BaseTX receiver circuit provides DC bias for the differential RX± inputs, clamping of large signal swing, equalization, and signal slicing for better noise immunity and signal detection. The amplification gain and slicing threshold are set by the on-chip band-gap reference.

Adaptive Equalizer

The 100BaseTX uses unshielded twisted pair copper wire for signal transmission. Since copper has resistance, the signal is reduced and its phase is changed as it travels down the wire. The transfer function of a TP cable, shielded (STP) or unshielded (UTP), is a function of the frequency, cable length, cable type, and environment temperature. Among different manufacturers of cables, the variation of cable performance is within ±2dB of each other. Other factors such as punch down block, patch panel, and connectors, etc., on wire installation will introduce another 1-2dB variation. A typical cable characteristic

impedance is 100Ω for UTP Category 5 and 150Ω for STP Type 1 cable. The QS6612 is designed to typically drive a maximum of 120 meters UTP-5 cable.

The amplitude and phase distortions cause inter-symbol interference (ISI) which makes clock and data recovery impossible. Compensation is therefore required at the receiving end to remove the ISI prior to the clock recovery or as a part of the clock/data recovery loop. This is done by including an equalization filter in the receive path to closely match the inverse transfer function of the TP cable.

The QS6612 uses an adaptive equalizer, which changes filter frequency response in accordance with cable length. The cable length is estimated based on comparisons of incoming signal strength against known cable characteristics. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions introduced by the cable.

Baseline Wander Compensation

The scrambled 5B code with MLT-3 line encoding is not D.C. balanced. The media, with transformer and common mode filtering, blocks the D.C. component of the code and therefore some amount of baseline wander will occur. The shift in the signal levels, coupled with non-zero rise and fall times of the serial stream, causes pulse-width distortion as measured after the data receiver and creates apparent jitter and possible increase in error rates. Studies have shown the worst case sustainable wander to be around 800mV, which can be accumulated within 20ms. The QS6612 uses a low frequency (LF) booster circuit to compensate for the attenuation of D.C. components.

MLT-3 to NRZI Conversion

The MLT-3 data is converted to NRZI by the QS6612. MLT-3 data to NRZI data conversion adopts the same principle as described in Sec. 4.1.4. For every transition in MLT-3 data, there is a corresponding transition in NRZI data. MLT-3 data changes the up/down direction of transitions after every two transitions while NRZI data changes the up/down direction after every transition. Setting bit 1 of Serial Management Register 31 to "1" bypasses the MLT-3 to NRZI conversion.

Clock/Data Recovery

The QS6612 uses a mixed-mode analog/digital phase locked loop (PLL) clock recovery circuit to extract clock information of the incoming NRZI data, which is then used to re-time the data stream and set data boundaries. After power-on or reset, the PLL locks to a free-running 25MHz clock that is a buffered version of the external clock source. When initial lock is achieved, the PLL switches to lock to the data stream, and extracts a 125MHz clock from the data which is used for bit framing of the recovered data. The PLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase align (lock) to data and its data/clock acquisition time after power-on is less than 100 transitions. The PLL can maintain lock on run-lengths of 10's of data bits in the absence of signal transitions. When no valid data is present, the PLL switches back to lock to the free running 25MHz clock, providing a continuously running 25MHz clock for the QS6612 internal operation.

NRZI/NRZ and Serial/Parallel Conversion

The recovered data is converted from NRZI to NRZ first and then to a 5-bit parallel format for output to the QS6612 de-scrambler. The 5-bit parallel data is not necessarily aligned to 4B/5B code-group's boundary.

When the PCSEN pin is strapped low, the NRZI to NRZ conversion is bypassed and the recovered data is routed directly to the serial-to-parallel shifter.

Data De-Scrambling

Bit 0 in Serial Management Register 31 directs the device to de-scramble received data. The scrambled data is presented in groups of 5 bits (quints) to a de-ciphering circuit which acquires synchronization ("lock") with the data stream by recognizing IDLE bursts of 30 or more bits and locking its de-ciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving lock, the incoming data is multiplied by the de-ciphering LFSR and de-scrambled, again in groups of 5 bits (quints). The de-scrambler is not required to decode data until it sees an IDLE burst of sufficient length to lock onto the data.

Once acquired, lock is re-affirmed by detection of what looks like IDLE concurrently in both the de-scrambled data and the scrambled stream. If lock fails to be re-affirmed within an interval of 325ms following its previous affirmation, it is deemed lost and the device will revert to lock acquisition mode.

De-scrambled (or clear-text) quints are then processed by an alignment detection circuit and a carrier sense circuit which scans for the /J/K/ delimiter pair.

The de-scrambling option is bypassed when the PCSEN pin is strapped low.

Carrier Sense Function

Carrier sense starts with detection of 2 non-continuous zeros within any 10-bit span. Carrier sense terminates if a span of 10 consecutive ones is seen before a /J/K/ delimiter pair. If /J/K/ is seen, carrier is maintained until either /T/R/ delimiter pair or a pair of IDLE code-groups is seen. Carrier is negated after the /T/ code-group or the first IDLE code-group is identified. If /T/ is not followed by /R/, then carrier is maintained. Carrier is treated similarly for IDLE followed by some non-IDLE code-group.

The CRS signal at the MII is asserted when: [(Receiving_Data) or (TX_EN and not(Full-Duplex))]. It is not synchronized to any particular clock.

In half-duplex mode, CRS is activated during transmit and receive of data. In full-duplex or repeater mode, CRS is activated during data reception only.

Alignment Function

The alignment circuit in the QS6612 determines code word alignment by recognizing the /J/K/ delimiter pair. This circuit is capable of finding /J/K/ at any of the 5 possible starting positions within the de-scrambled data quints. Note that /J/K/ is 10 bits long. Once code word alignment is determined, it is remembered and utilized until start of the next frame.

5B/4B Decoding

The 5B code words are converted to 4B DATA by translation according to the 5B/4B table (see Appendix A). The translated data is presented on the RXD[3:0] signal lines. The first /J/K/ pair is translated to a '55' nibble pair. Successive valid data quints translate to data nibbles. The /T/R/ delimiter and IDLE symbols are used to terminate carrier sense and the RX_DV signals and do not translate into data. In the absence of line code errors, the RXD signal presents nibble-aligned decoded data while RX_DV is active. RXD0 represents the LSB of the translated nibble. IDLE and /T/R/ delimiters do not result in data nibbles being transferred over the RXD[3:0] signals.

The RXD signals may be driven with arbitrary data while RX_DV is inactive. Driving them with a constant (static) value is preferred to avoid extraneous transitions on the pins.

The 5B/4B decoding is bypassed when bit 6 of Serial Management Register 31 is set to "1," or the PCSEN pin is strapped low.

Receiver Errors

In the decoding process (after finding /J/K/ and before ending delimiter), it is possible to detect receive errors. These occur for every received code-group other than a member of the DATA set (0:F) or /T/R/ code-group pair. When an error occurs, the RX_ER signal is asserted and arbitrary data may be put on the RXD lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RX_ER is asserted true and the value '1110' is placed onto RXD[3:0]. Note that the Valid Data signal is not yet asserted when this error occurs.

Valid Data Signal

The Valid Data signal (RX_DV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RX_CLK. RX_DV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or no signal is detected, where upon RX_DV is negated synchronously to falling of RX_CLK.

RX_DV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII).

The RX_ER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RX_DV asserted, RX_ER will be asserted for each code word that does not map to DATA.

Link Integrity Test

The QS6612 performs the link integrity test as outlined in the IEEE 100BaseX document (Clause 24) Link Monitor state diagram. The link status is multiplexed with 10Mbps link status to form the reportable link status bit in Serial Management Register 1, and driven to the LED_LINK pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state, and waits for an enable from the Auto-Negotiation block. When received, the Link-Up state is entered,

and the Transmit and Receive logic blocks become active. Should Auto-Negotiation be disabled, the link integrity logic moves immediately to the Link-Up state after entering the Link-Ready state.

Note that to allow the line to stabilize, the link integrity logic will wait a minimum of 330ms from the time signal is detected until the Link-Ready state is entered. Should the signal detect be lost at any time, this logic will immediately negate the LED_LINK signal and enter the Link-Down state.

When the device is in 10BaseT mode, the LED_LINK signal reflects the value of link status input signal from the 10BaseT transceiver.

10BaseT Operation

The QS6612 10BaseT module is comprised of these functional blocks:

- Manchester Encoder and Decoder
- Collision Translator
- Link Test Function
- Transmit Driver and Receiver
- Serial and Parallel Interface
- Jabber and SQE Test Functions
- Full- and Half-Duplex Operation

Manchester Encoder/Decoder

Data encoding and transmission begins when the transmit enable input (TX_EN) goes high and continues as long as the TX_EN remains high. Transmission ends when the transmit enable input goes low. The last transition occurs at the center of the bit cell if the last bit is one, or at the boundary of the bit cell if the last bit is zero.

Decoding is accomplished by a differential receiver circuit and a phase-locked loop that recovers a clock signal and NRZ data from the Manchester-encoded data stream.

To prevent noise at the RX+ or RX– input from falsely triggering the decoder, a squelch circuit rejects signals with short pulse widths, or with levels less than 300mV. When the input exceeds the squelch limits, the phase-locked loop locks onto the incoming signal and the QS6612 decodes a data frame. The carrier sense (CRS) and RX_DV signals are activated, and the receive data (RXD) becomes available. The receive clock RX_CLK is maintained active during idle periods in between data reception. The QS6612 supports extended length cables for 10BaseT by optionally selecting a lower squelch level around 150mV.

Collision Detection

The detection of signal collision causes the QS6612 to stop transmitting in Half-duplex operation mode and to report collision by asserting the COL signal on the MII. The collision detect output is deactivated within 160ns after the absence of the 10MHz signal.

Link Test Function

Each Twisted-Pair (TP) driver transmits a short positive pulse known as Normal Link Pulse (NLP) periodically when it is not sending data. These pulses are received at the other end of the TP cable to signal that the link is operating correctly. The time between link test pulses is compared to the expected range at the receiver to avoid false detection of noise pulses as link test pulses. If the link test fails (no pulses or data received in a fixed time period), then the LED_LINK pin is de-asserted. The Link monitor and Link Pulse transmit function can be disabled, forcing a good receive link, by setting bit 1 of the Control Register 17, NLP Disable.

Transmit Driver and Receiver

The QS6612 10BaseT driver is designed to operate with up to 160m of Unshielded Twisted-Pair (UTP) cable. The driver includes a circuit for transmit equalization, which attenuates low frequency components of the transmit waveform. This reduces the zero crossing jitter of the received signal and eliminates the need for a receive equalizer. In addition, the QS6612 provides the transmit wave-shaping to eliminate the need for external filters.

The signal received from the unshielded cable can be noisy so minimum voltage and timing limits must be met before the receiver logic is enabled. A “smart squelch” digital noise filter is used in addition to the analog squelch circuit in the receiver. The smart squelch circuit provides extra protection against false collisions and false link connections.

The QS6612 performs reverse polarity detection and correction. If the input polarity is reversed, it will be automatically detected and corrected.

10BaseT MII Interface

The QS6612 10BaseT supports the MII interface. The 10BaseT data is transferred in 4-bit nibbles and TX_CLK and RX_CLK are now 2.5MHz signals instead of 25MHz. To support this mode, the 10MHz 10BaseT serial clocks are divided by four.

Jabber and SQE Test Functions

If TX_EN is high for greater than 46ms, the 10BaseT transmitter will be disabled and COL will go active high. If TX_EN then goes low for more than 368ms, the 10BaseT transmitter will be re-enabled and COL will go low.

In 10BaseT operation, a short pulse will be output on COL after each packet is transmitted. This is required as a test of the 10BaseT transmit/receive path, and is called SQE Test or CD Heartbeat. The SQE Test can be disabled by setting bit 0 of the Mode Control Register 17, SQE Disable.

Full- and Half-Duplex Operation

The QS6612 10BaseT module is capable of operating in either Half-duplex mode or Full-duplex mode. In Half-duplex mode the QS6612 functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL pin signals collision, and the CRS is asserted during transmit and receive. In Full-duplex mode the QS6612 can simultaneously transmit and receive data. The COL signal is inactive, and CRS is asserted during receive only.

LED_ACT Operation

The LED_ACT pin connects directly to an LED to display activity. The LED_ACT is active on transmit or receive, except in Repeater mode which is only active on receive.

Auto-Negotiation

The purpose of the Auto-Negotiation function is to automatically configure devices with multiple PHY speeds and protocols based on the capabilities of their link partners. Information is exchanged (out of band) to determine a "highest common denominator" of functionality, and the devices are setup accordingly. Information is passed back to software by way of the Serial Management registers (described above).

The Auto-Negotiation function can be disabled by software or by the various settings of the MODE pins. Auto-Negotiation exchanges information with the link partner using a burst of link pulses known as Fast Link Pulses (FLPs). This burst is used to pass up to 16 bits of signaling information to and from the remote device (link partner). The FLPs advertise the device capabilities, as determined by the Auto-Negotiation Advertisement register (Register 4). The specific timing for the FLP burst is given in Table 7.

At power-up and at device reset, the MODE pins are sampled. If disabled, Auto-Negotiation will not occur until software enables bit 12 in Register 0. If Auto-Negotiation is enabled, the negotiation process will commence immediately, with bit 12 set appropriately.

Once the negotiation is successfully complete, the PHY configures itself for one of the following:
- 100BaseTX Full-duplex
- 100BaseTX Half-duplex
- 10BaseT Full-duplex
- 10BaseT Half-duplex

The results of the negotiation process are reflected in the Speed Select and the Duplex Mode bits of Register 0, as well as the Link Partner Ability Register (Register 5).

When Auto-Negotiation is disabled, the operating mode is set either by software using the bits in Register 0 (The default is 10BaseT half-duplex), or by the MODE pin settings which is read at power-on reset.

The implementation of the Auto-Negotiation function meets the 100BaseX specification. Refer to Clause 28 of the IEEE specification for more details on the negotiation protocol.

Table 7. Fast Link Pulse Timing

Parameter	Min	Typ	Max	Units
Link Pulse Width (either Data or Clock)		100		ns
Clock Pulse to Clock Pulse	111	125	139	µs
Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	µs
Pulses in a Burst	17		33	#
Burst Width		2		ms
FLP Burst to FLP Burst	8	16	24	ms

Media Independent Interface (MII)

The MII transfer data using 4-bit nibbles in each direction. On the transmit side, TX_EN signals the presence of data on TXD, and TX_ER indicates validity of data. On the receive side, RX_DV signals the presence of data on RXD, and RX_ER indicates error of data. The QS6612 provides the TX_CLK and RX_CLK as required by the MII.

In addition, two signals COL and CRS are used to indicate COLlision status and Carrier Sense status. COL is asserted asynchronously whenever QS6612 is transmitting and receiving at the same time in a half-duplex operation mode. In the full-duplex mode, COL is inactive. CRS is also asserted asynchronously whenever there is activity on either the transmitter or the receiver. In the full-duplex mode, CRS is asserted only when there is activity on the receiver.

The QS6612 supports two speeds on the MII. In the 100BaseTX mode the QS6612 outputs 25MHz TX_CLK and RX_CLK and employs the full set of MII signals. In the 10BaseT mode the TX_CLK and RX_CLK are reduced down to 2.5MHz when valid data in transferred across the MII.

Serial Management Interface

The Serial Management Interface (SMI) can be used to control the physical layer and to obtain status from it through an MII interface. This mechanism corresponds to the MII specification for 100BaseX (Clause 22), and supports registers 0 through 6. Additional "vendor-specific" registers are implemented within the range of 16 to 31 as allowed by the specification.

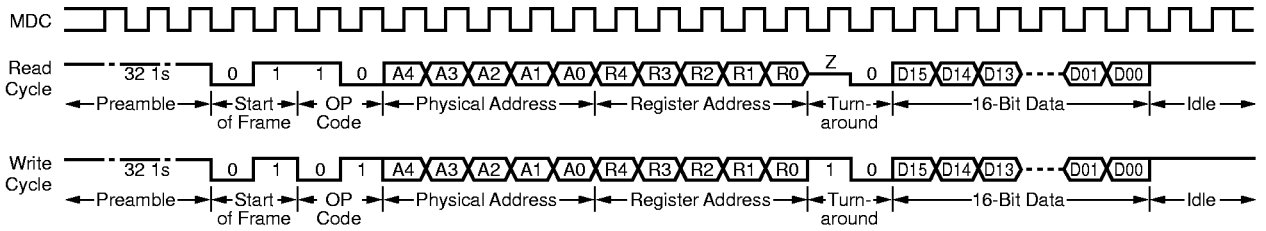
There are 2 signals in this interface: MDC and MDIO. MDC is a periodic clock provided by the station management device. MDIO is a bi-directional, open-drain signal that conveys a command word, or returns a status word serially.

MDC is guaranteed to have edge transitions no closer than 160ns. They may be arbitrarily far apart. The minimum cycle time is 400ns. It is intended that this interface be suitable for bit-serial manipulation ("bit-banging") by a host processor through an I/O port.

MDIO is pulled up resistively and is otherwise undriven between command and status accesses. The inter-access condition looks like one or more '1' bits to this device. To initiate either writing of a command word or retrieval of the status word, the station manager will drive a sequence of bits (as shown below) onto the MDIO line, clocking each into the QS6612 with a rising edge of MDC after MDIO has been given sufficient time to settle.

The frame structure that appears on MDIO with respect to MDC is as follows:

Figure 9. SMI Interface Signal Framing



Each MII management data frame is 64 bits long. The first 32 bits are preamble (PRE) consisting of 32 contiguous logic one bits on MDIO and 32 corresponding clock cycles on MDC. The start of frame (ST) is indicated by a <01> pattern. The next field with the operation code (OP): <10> indicates READ from MII management register operation, and <01> indicates WRITE to MII management register operation. The next two fields are PHY device address (AAAAA) and MII management register address (RRRRR). The PHY device address for QS6612 is provided by the 5 I/O pins called PHYAD<4:0>.

During READ operation, a 2 bit turnaround (TA) time spacing between Register Address field and Data field is provided for MDIO to avoid contention. Z stands for high impedance state. Following the turnaround time, a 16-bit data is read from or written into MII management registers of the QS6612.

SMI Interrupt Logic

The Management interface supports an interrupt capability that is not a part of the IEEE 802.3 specification. It generates an active low interrupt signal on the MDINT* output pin whenever the following status/error signals are asserted. Reading the Inter-

rupt Source register (Register 29) shows the source of the interrupt, and clears the interrupt output signal. The Interrupt Mask register (Register 30) enables each source by asserting the corresponding mask bit; at reset, all bits are masked (negated).

ThunderLAN Interrupt Support

The TI ThunderLAN MAC implements a proprietary interrupt scheme that allows the PHY device to signal an interrupt to the MAC via the MDIO pin. The QS6612 supports this mode of operation by programming Reg. 30.15 bit to a "1."

The clock cycle at the end of a transaction is used to disable the PHY management entity from driving the MDIO line after a register write. The interrupt is signaled to the host by driving MDIO low one clock cycle after the last data bit is transferred to/from the PHY, for the half of the MDCLK cycle when it is high.

The following shows the timing diagram of this mode of operation.

Figure 10. MINT Waveforms for MDIO and MDCLK

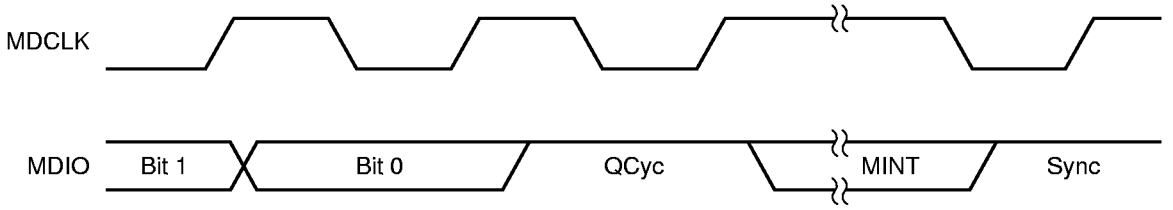


Table 8. Interrupt Source Table

Interrupt Source	Register Bit No.	Source/Mask Reg. Bit No.
Auto-Negotiate Complete	1.5	6
Remote Fault Detected	1.4	5
Link Status*	1.2	4
Auto-Negotiation LP Acknowledge	5.14	3
Parallel Detection Fault	6.4	2
Auto-Negotiation Page Received	6.1	1
Receive Error Detected	n/a	0

* Link Status generates an interrupt when *negated (link down),* not when asserted.

SMI Register Format

The following registers are supported (register numbers are in decimal):

The Physical Address of the PHY (Reg. 17.7:3) is set using the pins defined as PHYAD[4:0]. These input signals are strapped externally and sampled as reset is negated.

A detailed definition of the Serial Management registers is shown in Tables 10 through 20.

Table 9. Supported SMI Registers

Register No.	Description	Group
0	Basic Control Register	Basic
1	Basic Status Register	Basic
2	PHY Identifier 1	Extended
3	PHY Identifier 2	Extended
4	Auto-Negotiation Advertisement Register	Extended
5	Auto-Negotiation Link Partner Ability Register	Extended
6	Auto-Negotiation Expansion Register	Extended
17	Mode Control Register	Vendor-specific
27	Factory Test Register	Vendor-specific
28	Miscellaneous Control Register	Vendor-specific
29	Interrupt Source Register	Vendor-specific
30	Interrupt Mask Register	Vendor-specific
31	100BaseTX PHY Control Register	Vendor-specific

Table 10. Register 0 — Basic Control

Address	Name	Description	Mode	Default
0.15	Reset	1 = software reset Bit is self-clearing	RW/SC	0
0.14	Loop-back	1 = loop-back mode 0 = normal operation	RW	0
0.13	Speed Select	1 = 100Mbps 0 = 10Mbps Ignored if auto-negotiate is enabled (Reg. 0.12 = 1) Default is 1 when MODE[2:0] = 000, 001, 010, 011 or 100	RW	Set by MODE[2:0]
0.12	Auto-Negotiation Enable	1 = enable auto-neg. process (overrides Reg. 0.13 and Reg. 0.8) 0 = disable auto-negotiate process Default is 1 when MODE[2:0] = 111 or 100 Default is 0 when MODE[2:0] = 000, 001, or 101	RW	Set by MODE[2:0]
0.11	Power-Down	1 = power-down mode 0 = normal operation	RW	0
0.10	Isolate	1 = electrical isolation of PHY from MII and TX± 0 = normal operation Default is 1 when MODE[2:0] = 110	RW	Set by MODE[2:0]
0.9	Restart Auto-Negotiation	1 = restart auto-negotiate process 0 = normal operation Bit is self-clearing	RW/SC	0
0.8	Duplex Mode	1 = full-duplex 0 = half-duplex Default is High when MODE[2:0] = 001 or 011	RW	Set by MODE[2:0]
0.7	Collision Test	1 = enable COL test 0 = disable COL test	RW	0
0.6:0	*Reserved*		RW	0

Table 11. Register 1 — Basic Status

Address	Name	Description	Mode	Default
1.15	100BaseT4	0 = no T4 ability 1 = T4 ability	RO	0
1.14	100BaseX Full-duplex	1 = capable of 100BaseX full-duplex 0 = not capable of 100BaseX full-duplex	RO	1
1.13	100BaseX Half-duplex	1 = 100BaseX with half-duplex 0 = no 100BaseX with half-duplex	RO	1
1.12	10BaseT Full-duplex	1 = 10Mbps with full-duplex 0 = no 10Mbps with full-duplex ability	RO	1
1.11	10BaseT Half-duplex	1 = 10Mbps with half-duplex 0 = no 10Mbps with half-duplex ability	RO	1
1.10:6	*Reserved*		RO	0
1.5	Auto-Negotiate Complete	1 = auto-negotiate process completed 0 = auto-negotiate process not completed	RO	0
1.4	Remote Fault (Far end Fault)	1 = remote fault 0 = no remote fault	RO/LH	0
1.3	Auto-Negotiate Ability	1 = able to perform auto-negotiate 0 = unable to perform auto-negotiate	RO	Set by MODE[2:0]
1.2	Link Status	1 = link is up 0 = link is down	RO/LL	0
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/LH	0
1.0	Extended Capabilities	1 = supports extended capabilities registers	RO	1

Table 12. Register 2 — PHY Identifier 1

Address	Name	Description	Mode	Default
2.15:0	PHY ID Number*	Assigned to the 21st through 6th bits of the Organizationally Unique Identifier (OUI) respectively	RW	00 (0) 0000 (0) 0110 (6) 0000 (0) 01 (4)

*Quality Semiconductor OUI is 006050 (hex).

Table 13. Register 3 — PHY Identifier 2

Address	Name	Description	Mode	Default
3.15:10	PHY ID Number*	Assigned to the 5th through 0th bits of the OUI	RW	01 (1) 0001 (1)
3.9:4	Model Number	Six bit manufacturer's model number	RW	00 (0) 0000 (0)
3.3:0	Revision	Four bit manufacturer's revision number	RW	XXXX

Table 14. Register 4 — Auto-Negotiation Advertisement

Address	Name	Description	Mode	Default
4.15	Next Page	1 = next page capable 0 = no next page ability The QS6612 does not support next page ability	RO	0
4.14	*Reserved*		RO	0
4.13	Remote Fault	1 = remote fault supported 0 = no remote fault	RW	0
4.12:10	*Reserved*		RO	0
4.9	100BaseT4	1 = T4 able 0 = no T4 ability	RO	0
4.8	100BaseTX Full-duplex	1 = TX with full-duplex 0 = no TX full-duplex ability Default is 1 when MODE[2:0] = 111	RW	Set by MODE[2:0]
4.7	100BaseTX	1 = 100BaseTX able 0 = no 100BaseTX ability	RW	1
4.6	10BaseT Full-Duplex	1 = full-duplex 10BaseT able 0 = no 10BaseT full-duplex ability Default is 1 when MODE[2:0] = 111	RW	Set by MODE[2:0]
4.5	10BaseT	1 = 10BaseT able 0 = no 10BaseT ability Default is 1 when MODE[2:0] = 111	RW	Set by MODE[2:0]
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	00001

Table 15. Register 5 — Auto-Negotiation Link Partner Ability

Address	Name	Description	Mode	Default
5.15	Next Page	1 = next page capable 0 = no next page ability The QS6612 does not support next page ability	RO	0
5.14	Acknowledge	1 = link code word received from partner 0 = link code word not yet received	RO	0
5.13	Remote Fault	1 = remote fault detected 0 = no remote fault	RO	0
5.12:10	*Reserved*		RO	0
5.9	100BaseT4	1 = 100BaseT4 able 0 = no 100BaseT4 ability	RO	0
5.8	100BaseTX Full-Duplex	1 = full-duplex 100BaseTX able 0 = no full-duplex 100BaseTX ability	RO	0
5.7	100BaseTX	1 = 100BaseTX able 0 = no 100BaseTX ability	RO	0
5.6	10BaseT Full-Duplex	1 = full-duplex 10BaseT able 0 = no full-duplex 10BaseT ability	RO	0
5.5	10BaseT	1 = 10BaseT able 0 = no 10BaseT ability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	00001

Table 16. Register 6 — Auto-Negotiation Expansion

Address	Name	Description	Mode	Default
6.15:5	*Reserved*		RO	0
6.4	Parallel Detection Fault	1 = fault detected by parallel detection 0 = no fault detected by parallel detection	RO/LH	0
6.3	Link Partner Next Page Able	1 = link partner has next page ability 0 = link partner does not have next page ability	RO	0
6.2	Next Page Able	1 = local device has next page ability 0 = local device does not have next page ability	RO	0
6.1	Page Received	1 = new page received 0 = new page not yet received	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = link partner has auto-negotiate ability 0 = link partner does not have auto-negotiate ability	RO	0

Table 17. Register 17 — Mode Control

Address	Name	Description	Mode	Default
17.15:13	*Reserved*		RO	0
17.15.12	*Reserved*		RW	undefined
17.11	BTEXT	1 = reduces 10BT squelch level for extended cable length 0 = normal squelch level for 10BT	RW	0
17.10:9	*Reserved*		RO	0
17.8	Factory Test	1 = activates test mode 0 = normal operation	RW	0
17.7:3	Physical Address	Five bit PHY address	R0	Set by PHYAD[4:0]
17.2	Factory Test	1 = activates test mode 0 = normal operation	RW	0
17.1	NLP Disable	1 = disable Link Pulse Transmit and Test 0 = enable Link Pulse functions	RW	0
17.0	SQE Disable	1 = disable SQE 0 = enable SQE	RW	0

Register 27 — Reserved for Factory Test

Each bit set in this register signals the source of the interrupt.

The Management interface supports an interrupt capability that is not a part of the IEEE 802.3 specification. It generates an active low interrupt signal on the MDINT* output pin whenever the following status/error signals are asserted. Reading the Interrupt Source register (Register 29) shows the source of the interrupt, and clears the interrupt output signal. The Interrupt Mask register (Register 30) enables each source by asserting the corresponding mask bit. At reset, all bits are masked (negated).

Table 18. Register 29 — Interrupt Source

Address	Name	Description	Mode	Default
29.15:7	*Reserved*		RO	0
29.6	Reg. 1.5	1 = auto-negotiation complete 0 = not a source of interrupt	RO	0
29.5	Reg. 1.4*	1 = remote fault detected 0 = not a source of interrupt	RO	0
29.4	Reg. 1.2*	1 = link status negated (link down) 0 = not a source of interrupt	RO	0
29.3	Reg. 5.14	1 = auto-negotiation LP acknowledge 0 = not a source of interrupt	RO	0
29.2	Reg. 6.4*	1 = parallel detection fault 0 = not a source of interrupt	RO	0
29.1	Reg. 6.1*	1 = auto-negotiation page received 0 = not a source of interrupt	RO	0
29.0	*Reserved*		RO	0

*Register bits 1.2 and 1.4 are cleared when Register 1 is read, and bits 6.1 and 6.4 are cleared when Register 6 is read.

Table 19. Register 30 — Interrupt Mask*

Address	Name	Description	Mode	Default
30.15	Interrupt Mode	1 = supports ThunderLAN interrupt 0 = normal interrupt operation	RW	0
30.14:7	*Reserved*		RO	0
30.6:0	Mask Bits	1 = interrupt source enabled 0 = interrupt source is masked	RW	000000

*See Interrupt Source Table for bit assignments.

*See Interrupt Source Table for bit assignments.

Table 20. Register 31 — BaseTX PHY Control

Address	Name	Description	Mode	Default
31.15	Force FEF Transmit	1 = force transmit of Far End Fault (FEF) 0 = do not force transmit of FEF	RW	0
31.14	*Reserved*		RO/SC	0
31.13	*Reserved*		RW	0
31.12	Auto-Negotiate Complete	1 = auto-negotiate process completed 0 = auto-negotiate process not completed This bit is a copy of Register 1.5	RO	0
31.11	*Reserved**		RW	1
31.10	*Reserved**		RW	0
31.9	RLBEN	1 = enable remote loop-back 0 = disable remote loop-back	RW	0
31.8	DCREN	1 = enable DC restoration 0 = disable DC restoration	RW	Set by MODE[2:0]
31.7	*Reserved*		RO	1
31.6	4B5BEN	1 = enable 4B/5B encoding/decoding 0 = disable 4B/5B encoding/decoding	RW	Set by PCSEN
31.5	Transmit Isolate	1 = force QS6612 to isolate from line and MII 0 = normal operation Default is 1 when MODE[2:0] = 110	RW	Set by MODE[2:0]
31.4:2	Operation Mode Indication (OPMODE)	[000] = still in auto-negotiate [001] = 10BaseT half-duplex [010] = 100BaseX half-duplex [011] = repeater mode [100] = reserved [101] = 10BaseT full-duplex [110] = 100BaseX full-duplex [111] = PHY/MII isolate, auto-negotiate disabled	RO	000
31.1	MLT-3 Disable	1 = disable MLT-3 encoding 0 = enable MLT-3 encoding	RW	0
31.0	Scramble Disable	1 = disable data scrambling 0 = enable data scrambling Set by PCSEN Default is 0 when MODE[2:0] = 000 or 001	RW	Set by PSCEN or MODE[2:0]

* Bits 31.11 and 31.10 must always be written as 1 and 0 respectively.

Note: RW = read/write RO = read-only SC = self-clearing LL = latch low LH = latch high

PHY Identify Format

Serial Management Registers 2 and 3 contain information relating to identification of the PHY, including the IEEE assigned Organizationally Unique Identifier (OUI) and model/revision data. The OUI can be written by software to any value desired. The model and revision numbers are available to be utilized by the vendor as desired.

Mode Selection

In addition to Auto-Negotiation, the QS6612 can be forced into a specific mode on reset by configuring the MODE pins. The logic values of the MODE pins are latched on rising edge of reset to set the default value of various registers. The Registers affected are shown below. The values can be modified by writing into the registers.

The definition of the MODE inputs are shown below:

Table 21. MODE Pin Effects

MODE		Register	Default Register Bit Values												
			0				1	4			17	31			
[2,1,0]	MODE Definitions	Bit	8	10	12	13	3	5	6	8	1	0	1	5	8
000	Force 10BaseT Half-duplex operation without Auto-Negotiate.		0	0	0	1	0	x	x	x	1	0	1	0	0
001	Force 10BaseT Full-duplex operation without Auto-Negotiate.		1	0	0	1	0	x	x	x	1	0	1	0	0
010	Force 100BaseTX Half-duplex operation with Auto-Negotiate disable. CRS is active during Transmit and Receive.		0	0	0	1	1	0	0	1	0	P	0	0	1
011	Force 100BaseTX Full-duplex operation with Auto-Negotiation disable. CRS is only active during Receive.		1	0	0	1	1	0	0	1	0	P	0	0	1
100	Force 100BaseTX Half-duplex advertisement with Auto-Negotiate enable. CRS is active during Transmit and Receive		0	0	1	1	1	0	0	0	0	P	0	0	1
101	Repeater Mode — Auto-Negotiate enable, advertise 100BaseTX Half-duplex, CRS and LED_ACT active on Receive only.		0	0	1	1	1	0	0	0	0	P	0	0	1
110	Isolate MII and TX±.		0	1	0	1	1	1	1	0	0	P	0	1	1
111	All capable Auto-Negotiate enable.		0	0	1	0	1	1	1	1	0	P	0	0	1

Note: x = does not effect register bit P = controlled by PCSEN pin

Repeater Operation

Repeater Mode (101) can be used for 100BaseTX repeater designs. In repeater mode, the CRS and the LED_ACT are only active when the QS6612 is receiving data. Auto-Negotiation is enabled, but it only advertises half-duplex 100BaseTX mode.

If Auto-Negotiation is not needed, Mode 011 (100BaseT full-duplex) can be selected so that the CRS is activate on receive only. This functionality is equivalent to the full-duplex mode operation of the part. In this mode the Activity LED must be connected to the repeater controller chip and not the QS6612 LED_ACT, since the LED_ACT of the QS6612 will be active on both transmit and receive in full-duplex mode.

In repeater designs all the transmit clocks must be synchronized with the Repeater Controller transmit clock. This master clock can be supplied to the QS6612 X1 input pin. The QS6612 TX_CLK is not used in the repeater application.

Loop-back Operation

The QS6612 provides internal local loop-back function for both the 100BaseTX and 10BaseT operation and a remote loop-back function for the 100BaseTX operation. While loop-back is active, transmitter and receiver function as in normal mode with the exception that collision detection is disabled. The source of local loop-back control is Register 0 (bit 14). The source of remote loop-back control is bit 9 of Register 31.

The 100BaseTX local loop-back starts at the MII's TXD inputs and routes transmitted data at the output of NRZ to NRZI conversion module back to the receiving path's clock and data recovery module, and connects to the MII's RXD outputs. This loop-back covers the transmit and receive path excluding the MLT-3 and equalizer.

The 100BaseTX remote loop-back routes receiving data at the output of the clock and data recovery module to the transmitting path's NRZI to MLT-3 conversion module. This loop-back covers the MLT-3 transceiver, the equalizer, and the output wave-shaper.

When the 10BaseT local loop-back is activated the QS6612 sends serial data from the MII transmit data input through the encoder, and back through the phase-locked loop and decoder to the MII receive data output. The transmit driver is in the idle state during loop-back mode and the receiver circuitry and collision detection are disabled. Transmit data is always looped back during the 10BaseT half-duplex operation, simulating the physical broadcast characteristic of 802.3 coaxial cable networks. Transmit data is not looped back during the 10BaseT full-duplex operation.

When in loop-back mode, the QS6612 TX± lines are tri-stated and isolated from the network.

Reset and Power-Down Operation

The QS6612 can be reset in two ways.

When MII Control Register 0 Bit 15 (0.15) is set to logical one, it will also reset the entire chip and then self-clear the bit to logical zero. This is the software reset signal that powers down the analog circuitry but leaves the digital circuitry operational.

The QS6612 can also be reset via the I/O pin RESET*. Reset operation will take place whenever a Low signal of at least 100µs is applied to the RESET*. This is the hardware reset signal.

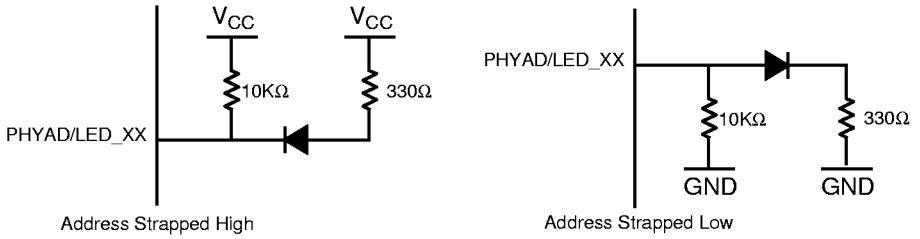
When the RESET pin is held low, all analog and digital circuitry is shut down for minimal power consumption. The RESET pin power-down mode allows the QS6612 to be completely powered down when not being used in a system.

The power consumption of the QS6612 is significantly reduced by the device's built-in power-down features. Separate power supply lines are used to power the 10BaseT circuitry and the 100BaseTX circuitry, therefore the two circuits can be turned-on and turned-off independently. Whenever the QS6612 is set to operate in a 100BaseTX mode, the 10BaseT circuitry is powered down, and vice versa. This way no unnecessary power is wasted.

LED Pin Connections

The QS6612 supports four status LEDs. The LED pins are shared with four PHYAD pins (PHYAD[0-3]). These pins can be externally strapped as "high" or "low" to encode different PHY addresses. The circuits below must be used to ensure proper operation of the LEDs.

Figure 11. Status LED Connection Schematics



ELECTRICAL CHARACTERISTICS

Table 22. Absolute Maximum Ratings and Recommended Operating Range

Absolute Maximum Ratings	
Storage Temperature	–55°C to 150°C
V_{CC} Supply Referenced to GND	–0.5V to 7.0V
Digital Input Voltage	–0.5V to V_{CC}
DC Output Voltage	–0.5V to V_{CC}
Recommended Operating Range	
Operating Temperature	0°C to 70°C
V_{CC} Supply Voltage Range	4.75V to 5.25V

In Tables 23 and 24, unless otherwise specified, T_A = 0°C to 70°C, V_{CC}/V_{CCA} = 4.75V to 5.25V.

Table 23. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Consumption						
RESET Power	PS_{RESET}	RESET pin held low V_{CC} = 5.0V		550		mW
Auto-Negotiation Power	PS_{AN}	Transmitting FLPs V_{CC} = 5.0V		725		mW
10BaseT Transmit Power	PS_{10T}	Minimum IPG, max frame length V_{CC} = 5.0V		1075		mW
100BaseT Transmit Power	PS_{100T}	Minimum IPG, max frame length V_{CC} = 5.0V		925		mW
Digital I/Os						
Output High Voltage	V_{OH}	I_{OH} = –8mA, V_{CC} = 5.0V	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 5.0V			0.4	V
Input High Voltage	V_{IH}	V_{CC} = 5.0V	2.0			V
Input Low Voltage	V_{IL}	V_{CC} = 5.0V			0.8	V
Input Current	I_{IN}	V_{CC} = 5.25V V_{IN} = 0 to 5.25V	–10		10	µA
Output Tri-state Leakage Current	$\|I_{OZ}\|$				10	µA
Crystal Oscillator						
X1 Input Threshold	V_{XTH}	V_{CC} = 5.0V		2.4		V
100BaseT Signal Detect						
Signal Detect Turn-on Threshold (post equalized)	SD_{ON}		250	300	350	mV

Table 24. AC Electrical Characteristics

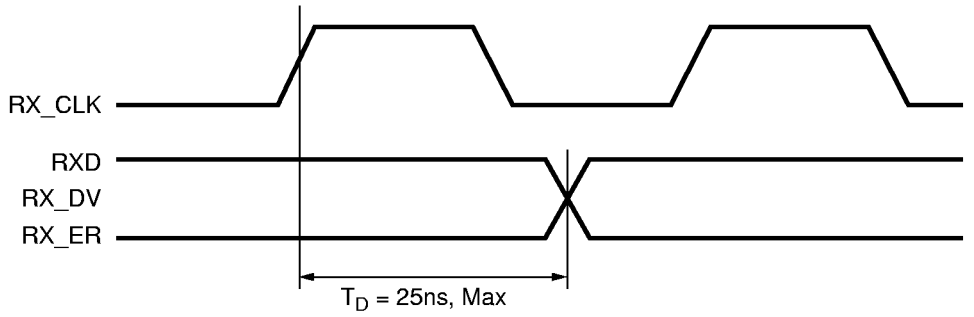
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Inputs, RX±						
RX± common mode input voltage	V_{RCM}		2.375	2.5	2.675	V
RX± differential input voltage, peak-to-peak	V_{RDM}		0.54	0.6	0.66	Vp-p
RX± differential-mode input resistance	R_{DM}	Measured between input terminals	8.5	10	11.5	KΩ
RX± common-mode input resistance	R_{CM}	Measured between one input and supply ground	8.5	10	11.5	KΩ
Differential Output TX±						
100BaseTX TX± average output current	I_{AV100}			15.3		mA
10BaseT TX± average output current	I_{AV10}			38.2		mA
Differential TX output current imbalance	ΔI_{MAX}	Relative to I_{AV100} or I_{AV10}	–5	0	5	%
Transmit MLT-3 at AUI (RJ45)						
TX driver rise and fall time	$t_{TXr/f}$	10% to 90%, into 100Ω differential at cable side	3	4	5	ns
TX differential signal amplitude			950	1000	1050	mVp-p
Transmit MLT-3 AC						
TX differential signal amplitude symmetry			98	100	102	%
TX rise & fall time symmetry		10% to 90% signal amplitude	–0.5	0	0.5	ns
TX duty cycle distortion		Peak-to-peak	–0.5	0	0.5	ns
TX signal overshoot			0		5	%
TX signal edge jitter	J_{TX}			0.4	0.7	ns
100BaseTX Frequency Synthesizer						
RXCLK jitter	J_{RX}				1	ns
Output clock duty cycle, TX_CLK/RX_CLK		Tested @ 50pF load	43	50	57	%
10BaseT Operation						
Carrier sense turn-on delay	t_{CSON}				300	ns
Carrier sense turn-off delay	t_{CSOFF}				160	ns
Decoder acquisition time	t_{DAT}				950	ns
Differential inputs rejection pulse width	t_{DREJ}		8	20	30	ns
Collision turn-on delay	t_{COLON}				900	ns
Collision turn-off delay	t_{COLOFF}				160	ns
SQE test start delay	t_{SQEON}		0.6	1.0	1.6	µs
SQE test duration	t_{SQED}		0.5	1.0	1.5	µs

Table 25. MDI and MII Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESET* low period	T_{RSTl}		100			µs
RESET* input rise time	T_{RSTr}	10% to 90% of V_{CC}			5	ns
TXD[3:0], TX_EN, TX_ER setup to TX_CLK rise	T_{SU}		10			ns
TXD[3:0], TX_EN, TX_ER hold after TX_CLK rise	T_H		3			ns
TXD[3:0],TX_EN,TX_ER setup to X1 rise	T_{SUX}		10			ns
TXD[3:0],TX_EN,TX_ER hold after X1 rise	T_{HX}		1			ns
Output access time from RX_CLK rising edge to RXD[3:0], RX_DV, RX_ER valid	T_D		22		25	ns
TX propagation delay	T_{TXPD}	From TXD[3:0] to TX±	50	52	54	ns
RX propagation delay	T_{RXPD}	From RX± to RXD[3:0]	210	215	222	ns
RX_EN turn-on delay			2.1	3.0	4.2	ns
TX_EN sampled to MDI output to first bit of /J/ with ref. to TX_CLK			39	40	42	ns
MDI input (first bit of /J/) to CRS assert			135	138	142	ns
MDI input (first bit of /T/) to CRS de-assert			218	222	229	ns
MDI input (first bit of /J/) to RX_DV rise			210	217	225	ns
MDI input (last bit of /R/) to RX_DV fall			118	122	127	ns
CRS rise to RX_DV rise			78	79	80	ns
TX_EN turn-on delay		1st TXCLK rising edge after TXEN rise to first bit of /J/	32	35	39	ns
TX_EN turn-off delay		1st TXCLK rising edge after TXEN fall to first bit of the /T/	31	34	38	ns
TX_EN sampled to CRS assert with ref. to TX_CLK rising			—	8	—	bits
TX_EN sampled to CRS de-assert with ref. to TX_CLK rising			—	12	—	bits

TIMING DIAGRAMS

Figure 12. MII Receive Timing Diagram



The MII interface timing is structured so as to guarantee 10ns setup and hold time for RXD, RX_DV, RX_ER signals relative to the rising edge of RX_CLK as seen at the MAC side of the MII. To meet this goal without requiring special hold time generators within this device, the receive signals are clocked with the falling edge of RX_CLK and then driven out. RX_CLK is also driven out, to give it comparable delay from the internal signal.

Figure 13. MII Transmit Timing Diagrams

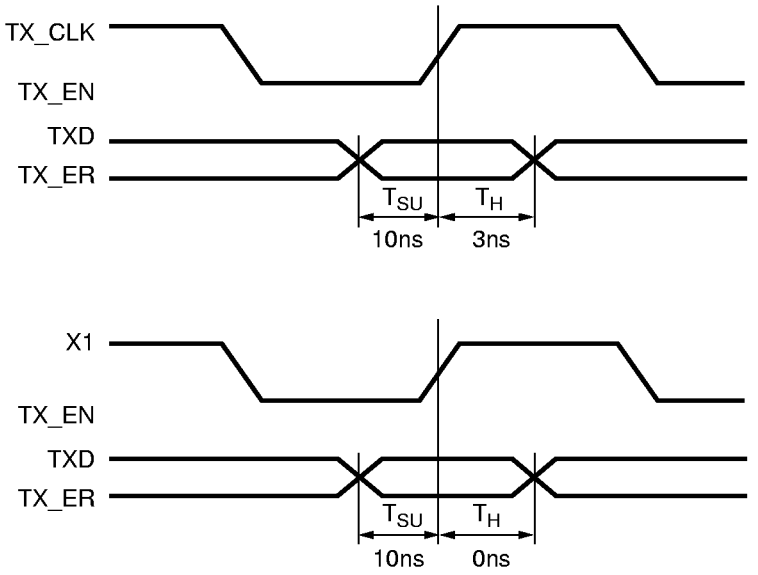


Figure 14. Serial Management Interface (SMI) WRITE/READ Timing Diagrams

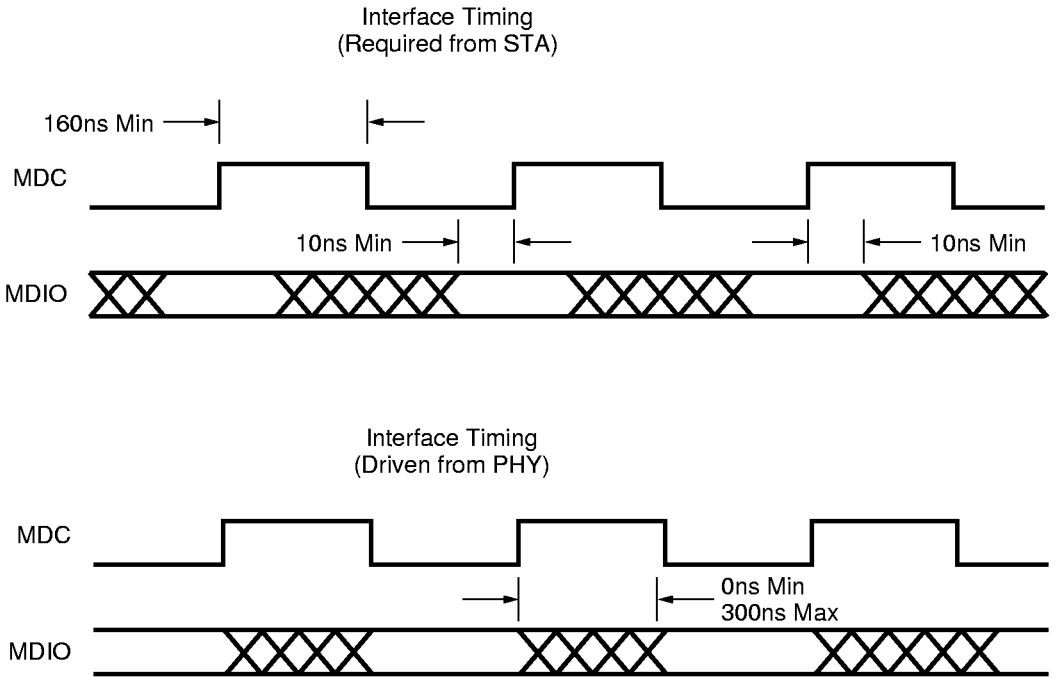
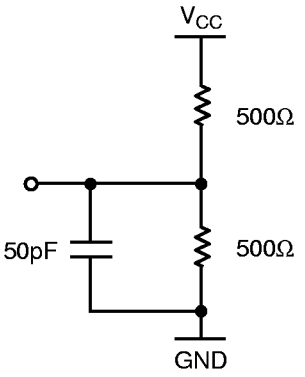


Figure 15. Digital Output and I/O Pin Test Load



PACKAGING

Figure 16. Low Profile Quad Flatpack Outline (10x10x1.4mm)

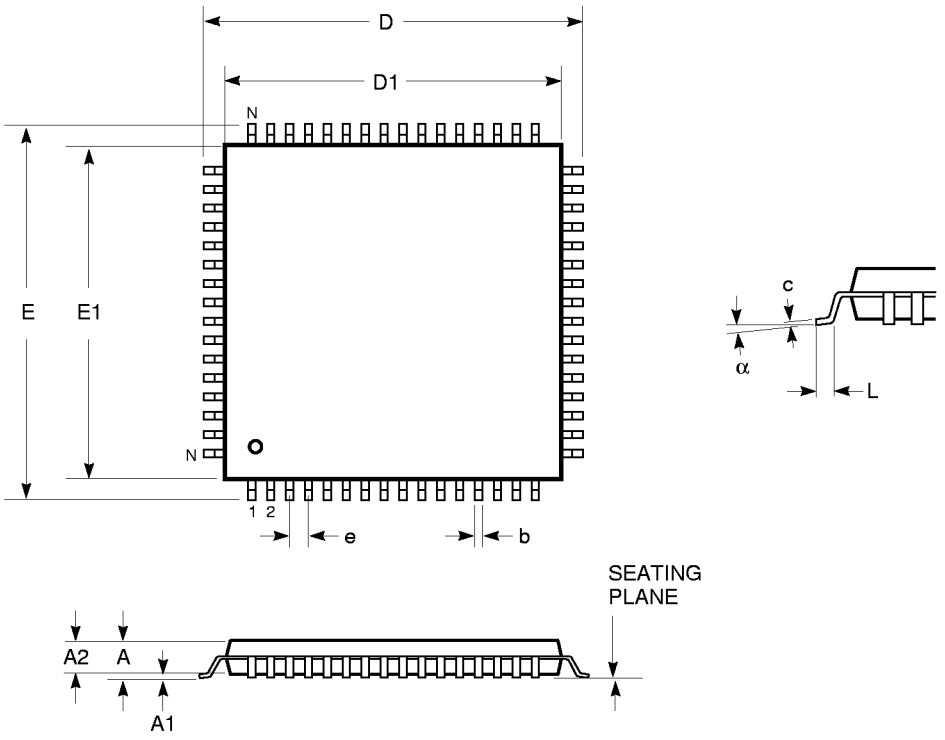


Table 26. LQFP Package Dimenmsions

N	A	A1	A2	B	D	D1	E	E1	e	L	L1
64	1.60 Max.	0.05 Min. 0.15 Max.	1.40 ±0.05	0.22 ±0.05	12.00 ±0.25	10.00 ±0.10	12.00 ±0.25	10.00 ±0.10	0.50	0.60 ±0.15	1.00 ±0.12

Table 27. QS6612 Tape and Reel Dimensions

Package Style	Lead Count	"W" Tape Width	"P0" Pitch	"A0" Cavity Width	"B0" Cavity Length	"K0" Cavity Height	Qty/ Reel
TQFP “LF”	64L	24	16	12.4	12.4	1.7	1500

All dimensions are in millimeters (mm) and are compliant with the Standard EIA-481-A, "Taping of Surface Mount Components for Automatic Placement." Reel diameter is 13 inches.

Table 28. TFQP “LF” Package Thermal Characteristics

Air Flow (f.p.m.)	0	100	200	300	400
Theta-JA (°C/W)	45.61	40.30	33.35	31.16	29.43
Theta-JC (°C/W)	14.60	—	—	—	—

Table 29. 4B/5B Code Table

Code	Symbol	Receiver Interpretation	Transmitter Interpretation
11110	0	0 0000 (data)	0 0000 (data)
01001	1	1 0001 (data)	1 0001 (data)
10100	2	2 0010 (data)	2 0010 (data)
10101	3	3 0011 (data)	3 0011 (data)
01010	4	4 0100 (data)	4 0100 (data)
01011	5	5 0101 (data)	5 0101 (data)
01110	6	6 0110 (data)	6 0110 (data)
01111	7	7 0111 (data)	7 0111 (data)
10010	8	8 1000 (data)	8 1000 (data)
10011	9	9 1001 (data)	9 1001 (data)
10110	A	A 1010 (data)	A 1010 (data)
10111	B	B 1011 (data)	B 1011 (data)
11010	C	C 1100 (data)	C 1100 (data)
11011	D	D 1101 (data)	D 1101 (data)
11100	E	E 1110 (data)	E 1110 (data)
11101	F	F 1111 (data)	F 1111 (data)
11111	I	IDLE	Sent after /T/R until TX_EN goes high
11000	J	First nibble of Start Of Packet (SOP), 0101 if following IDLE, else receiver error (RX_ER goes high)	Single symbol sent after TX_EN goes high
10001	K	Second nibble of SOP, 0101 if following /J, else receiver error (RX_ER goes high)	Single symbol sent following /J after TX_EN goes high
01101	T	First nibble of End of Packet (EOP). CRS goes high if /T is followed by /R, else receiver error (RX_ER goes high)	Single symbol sent after TX_EN goes low
00111	R	Second nibble of EOP. CRS goes high if /R is preceded by /T, else receiver error (RX_ER goes high)	Single symbol sent following /T after TX_EN goes low
00100	H	Transmit Error Symbol	Sent continuously while TX_ER is high
00110 11001 00000 00001 00010 00011 00101 01000 01100 10000	V	INVALID, receive error (RX_ER goes high) if received while RX_DV is high	INVALID (never transmitted)