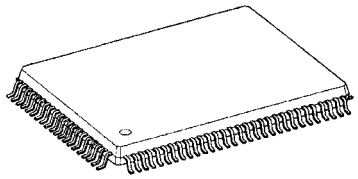
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6B07

COLUMN DRIVER FOR A DOT MATRIX LCD

The T6B07 is an 80-channel-output column driver for an STN dot matrix LCD. The T6B07 features 28-V LCD drive voltage and a 10-MHz maximum operating frequency. The T6B07 is able to drive LCD panels with a duty ratio of up to 1/240. It is recommended for use with the T6B08.



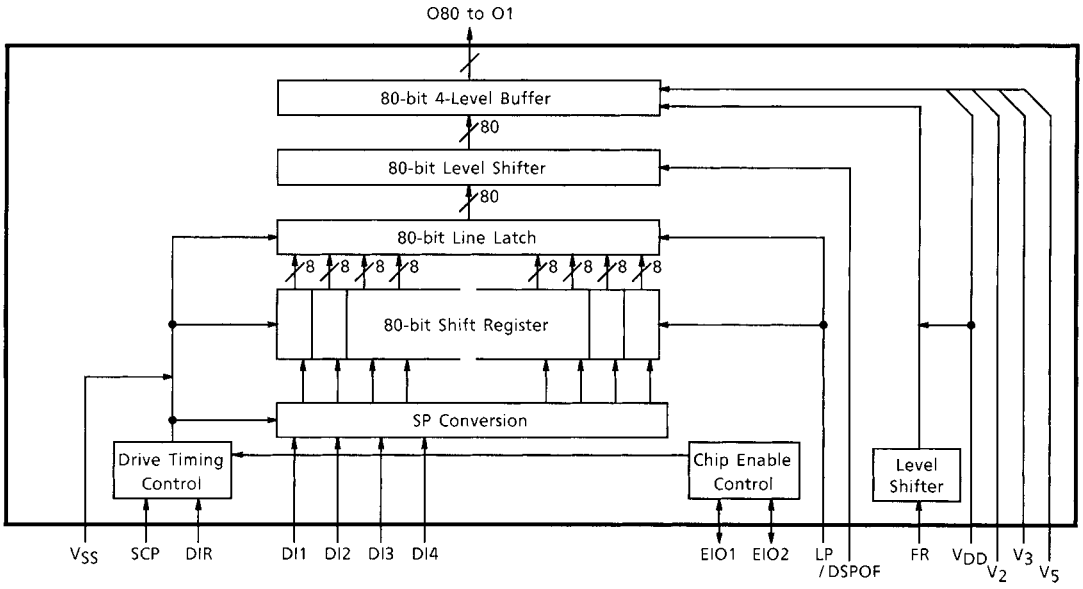
QFP100-P-1420-0.65A

Weight:1.60 g (typ.)

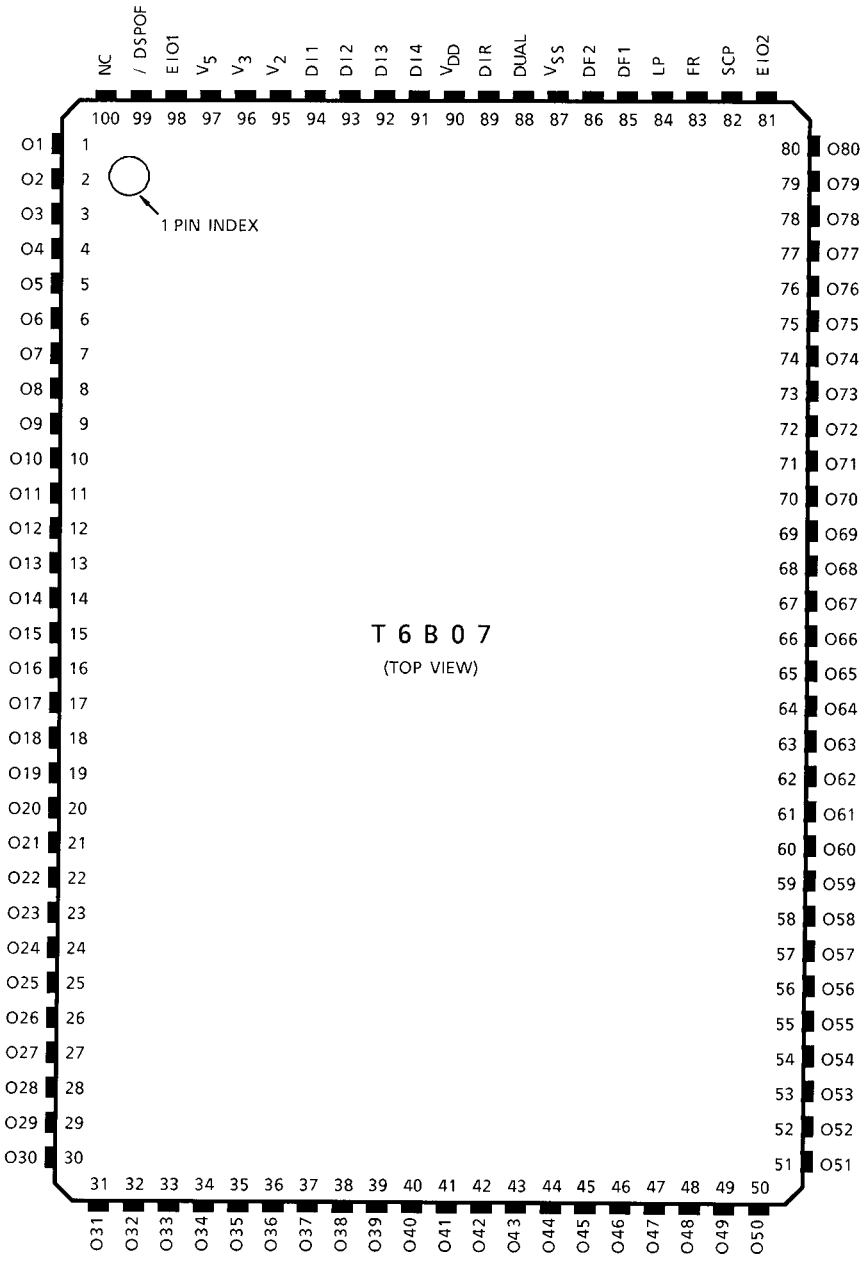
Features

- Display duty application : to 1/240
- LCD drive signal : 80
- Data transfer : 1, 2, 4-bit bidirectional
- Operating frequency : 10 MHz
- LCD drive voltage : 11 to 28 V (max 30 V)
- Operating voltage : 3.0 to 5.5 V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 2.2 kΩ (max) (12.8 V, 1/9 bias)
- Display-off function : When /DSPOF is L, all LCD drive outputs (O1 to O80) remain at the V_{DD} level.
- Low power consumption : Cascade connections and auto enable transfer functions are available.

Block Diagram



Pin Assignment



Pin Functions

<table>
<tr><th>Pin Name</th><th>I / O</th><th>Functions</th><th>Level</th></tr>
<tr><td>O1 to O80</td><td>Output</td><td>Output for LCD drive signal</td><td>V_{DD} to V_5</td></tr>
<tr><td>DI1 to DI4</td><td>Input</td><td>Input for shift data</td><td rowspan="9">V_{DD} to V_{SS}</td></tr>
<tr><td>SCP</td><td>Input</td><td>(Shift Clock Pulse)
Input for shift clock pulse</td></tr>
<tr><td>FR</td><td>Input</td><td>(Frame)
Input for frame signal</td></tr>
<tr><td>LP</td><td>Input</td><td>(Latch Pulse)
Input for shift clock pulse
Display data is latched on the rising edge of LP.</td></tr>
<tr><td>DUAL</td><td>Input</td><td>(Dual Mode)
Terminal for dual input mode or single input mode select</td></tr>
<tr><td>DIR</td><td>Input</td><td>(Direction)
Input for data flow direction select</td></tr>
<tr><td>DF1, DF2</td><td>Input</td><td>(Data Format)
Input for selection data format (1−bit, 2−bit, 4−bit)</td></tr>
<tr><td>EIO1, EIO2</td><td>I / O</td><td>(Input / output for ENABLE signal)
At cascade connection of the T6B07, connect output pin to enable pin (input) of next LSI externally.
<table>
<tr><th>DUAL</th><th>DIR</th><th>EIO2</th><th>EIO1</th></tr>
<tr><td>L</td><td>L</td><td>OUT</td><td>IN</td></tr>
<tr><td>L</td><td>H</td><td>IN</td><td>OUT</td></tr>
<tr><td>H</td><td>L</td><td>OUT</td><td>IN</td></tr>
<tr><td>H</td><td>H</td><td>OUT</td><td>IN</td></tr>
</table></td></tr>
<tr><td>/ DSPOF</td><td>Input</td><td>(Display Off)
/ DSPOF = L : Display−off mode, (O1 to O80) remain at the V_{DD} level.
/ DSPOF = H : Display−on mode, (O1 to O80) are operational.</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for internal logic (5 V)</td><td rowspan="5">—</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Power supply for internal logic (0 V)</td></tr>
<tr><td>V_2</td><td>—</td><td>Power supply for LCD drive circuit</td></tr>
<tr><td>V_3</td><td>—</td><td>Power supply for LCD drive circuit</td></tr>
<tr><td>V_5</td><td>—</td><td>Power supply for LCD drive circuit</td></tr>
</table>

Relation Between FR, Data Input and Output Level

F R	Data Input (DIO1, DIO2)	/ DSPOF	Output Level
L	L	H	V_2
L	H	H	V_{DD}
H	L	H	V_3
H	H	H	V_5
*	*	L	V_{DD}

*: Don’t care

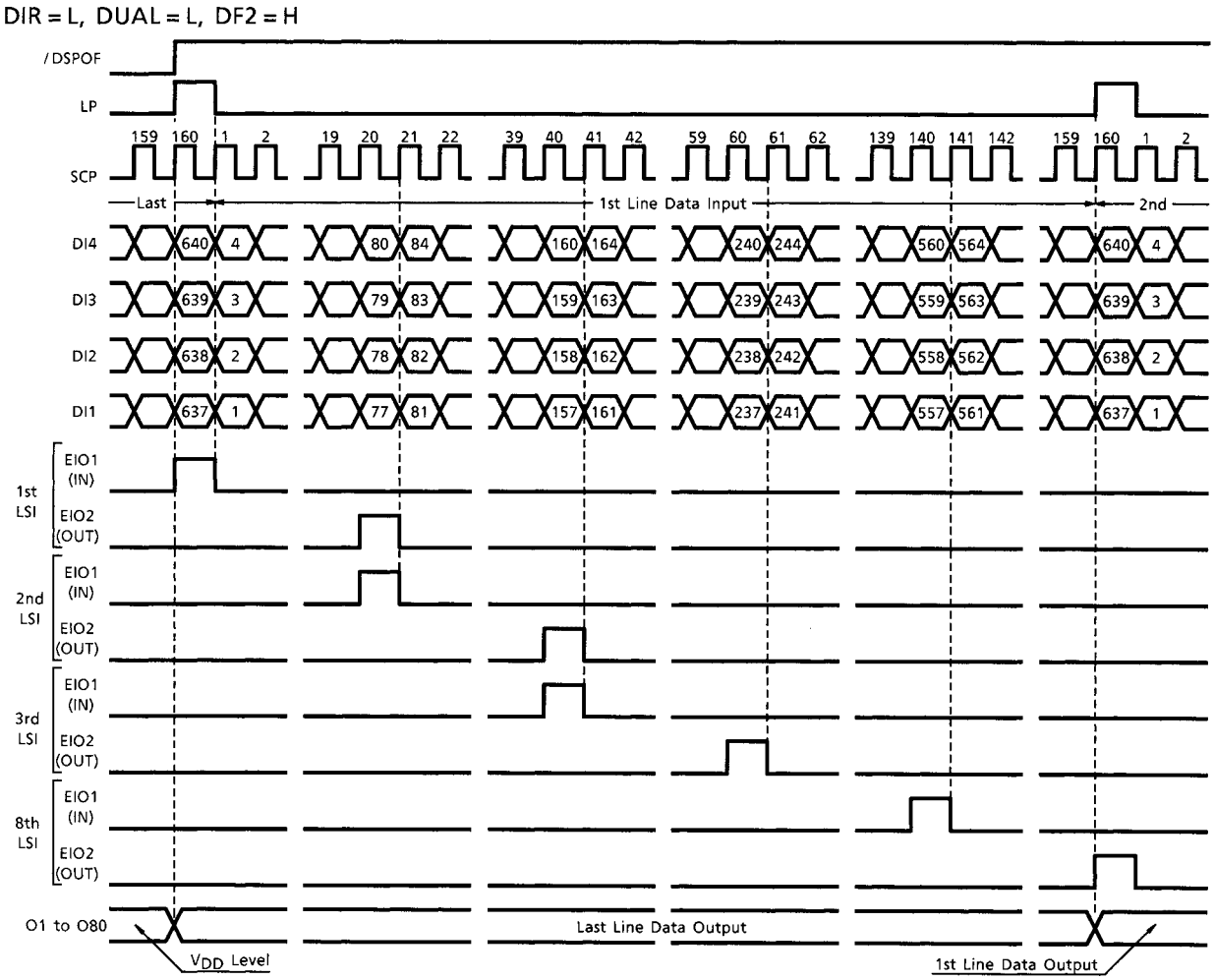
Data Input Format

DF1	DF2	DUAL	DIR	bits	DATA INPUT				DATA FORMAT			
					DI1	DI2	DI3	DI4	Ⓛ DI1 Ⓕ	Ⓛ DI2 Ⓕ	Ⓛ DI3 Ⓕ	Ⓛ DI4 Ⓕ
L	L	L	L	1-bit	OPEN	OPEN	OPEN	IN	—	—	—	O80,O79···O2,O1
L	L	L	H		IN	OPEN	OPEN	OPEN	O1,O2···O79,O80	—	—	—
L	L	H	L		OPEN	OPEN	OPEN	IN	—	—	—	O80,O79···O42,O41
L	L	H	H		IN	OPEN	OPEN	IN	O1,O2···O39,O40	—	—	O80,O79···O42,O41
H	L	L	L	2-bit	OPEN	OPEN	IN	IN	—	—	O79,O77···O3,O1	O80,O78···O4,O2
H	L	L	H		IN	IN	OPEN	OPEN	O1,O3···O77,O79	O2,O4···O78,O80	—	—
H	L	H	L		OPEN	OPEN	IN	IN	—	—	O79,O77···O43,O41	O80,O78···O44,O42
H	L	H	H		IN	IN	IN	IN	O1,O3···O37,O39	O2,O4···O38,O40	O79,O77···O43,O41	O80,O78···O44,O42
*	H	L	L	4-bit	IN	IN	IN	IN	O77,O73···O5,O1	O78,O74···O6,O2	O79,O75···O7,O3	O80,O76···O8,O4
*	H	L	H		IN	IN	IN	IN	O1,O5···O73,O77	O2,O6···O74,O78	O3,O7···O75,O79	O4,O8···O76,O80
*	H	H	L		IN	IN	IN	IN	O77,O73···O45,O41	O78,O74···O46,O42	O79,O75···O47,O43	O80,O76···O48,O44
*	H	H	H	DON'T USE								

Ⓛ→LAST DATA

Ⓕ→FIRST DATA

Timing Diagram



Absolute Maximum Ratings
(Ensure that the Following Conditions are Maintained, $V_{DD} \geq V_2 \geq V_3 \geq V_5$, V_{SS} = 0 V)

Item	Symbol	Pin Name	Rating	Unit
Supply Voltage 1	V_{DD}	V_{DD}	−0.3 to 7.0	V
Supply Voltage 2	V_2	V_2	V_{DD} − 30.0 to V_{DD} + 0.3	V
Supply Voltage 3	V_3	V_3	V_{DD} − 30.0 to V_{DD} + 0.3	V
Supply Voltage 4	V_5	V_5	V_{DD} − 30.0 to V_{DD} + 0.3	V
Input Voltage	V_{IN}	(Note 1)	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	—	−20 to 75	°C
Storage Temperature	T_{stg}	—	−55 to 125	°C

Note 1: SCP, FR, LP, DIR, DF1, DF2, DUAL, DI1 to DI4, / DSPOF

Electrical Characteristics
DC Characteristics
Test Conditions (1) (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, V_5 = (V_{DD} − 28) to (V_{DD} − 11) V, Ta = − 20 to 75°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Supply Voltage 1		—	—	—	4.5	5.0	5.5	V	V_{DD}
Supply Voltage 2		V_5	—	—	V_{DD} −28	—	V_{DD} −11	V	V_5
Input Voltage	H Level	V_{IH}	—	—	V_{DD} −0.8	—	V_{DD}	V	SCP, FR, LP, DIR, DUAL, DF1, DF2, DI1 to DI4, / DSPOF
	L Level	V_{IL}		—	0	—	0.8		
Output Voltage	H Level	V_{OH}	—	I_{OH} = −0.5 mA	V_{DD} −0.5	—	—	V	EIO1, EIO2
	L Level	V_{OL}		I_{OL} = 0.5 mA	—	—	0.5		
Output Resistance	H Level	R_{OH}	—	V_{OUT} = V_{DD} − 0.5 V (Note 2)	—	1.2	2.2	kΩ	O1 to O80
	M Level	R_{OM}	—	V_{OUT} = V_2 ± 0.5 V (Note 2)	—	1.2	2.2		
		R_{OM}	—	V_{OUT} = V_3 ± 0.5 V (Note 2)	—	1.2	2.2		
	L Level	R_{OL}	—	V_{OUT} = V_5 + 0.5 V (Note 2)	—	1.2	2.2		
Current Consumption (Note 3)		I_{SS}	—	V_{DD} = 5.5 V V_5 = −22.5 V f_{FR} = 35 Hz f_{SCP} = 2.5 MHz V_{IH} = 5.5 V, V_{IL} = 0 V Input Data: every bit inverted	—	400	700	μA	V_{SS}
Current Consumption (Note 4)		I_{SS}	—	As mentioned above	—	100	200	μA	V_{SS}

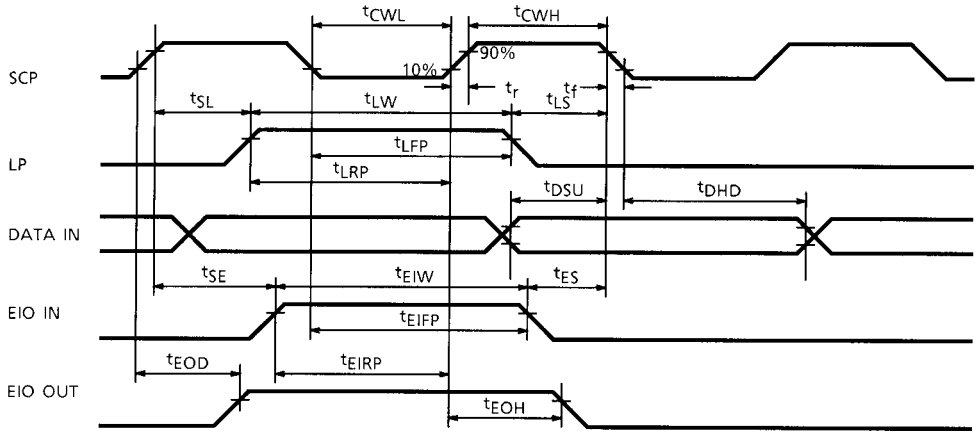
Note 2: V_{DD} = 3.0 V, V_5 = −7.8 V, V_2 = V_{DD} − 2 / 9 (V_{DD} − V_5), V_3 = V_{DD} − 7 / 9 (V_{DD} − V_5)
Note 3: Internal data receiver operating
Note 4: Internal data receiver sleeping

Test Conditions (2) (**Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V, V_5 = (V_{DD} − 28) to (V_{DD} − 11) V, Ta = − 20 to 75°C**)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Supply Voltage 1		—	—	—	3.0	3.3	5.5	V	V_{DD}
Supply Voltage 2		V_5	—	—	V_{DD} −28	—	V_{DD} −11	V	V_5
Input Voltage	H Level	V_{IH}	—	—	V_{DD} −0.6	—	V_{DD}	V	SCP, FR, LP, DIR, DUAL, DF1, DF2, DI1 to DI4, / DSPOF
	L Level	V_{IL}		—	0	—	0.6		
Output Voltage	H Level	V_{OH}	—	I_{OH} = −0.5 mA	V_{DD} −0.5	—	—	V	EIO1, EIO2
	L Level	V_{OL}		I_{OL} = 0.5 mA	—	—	0.5		
Output Resistance	H Level	R_{OH}	—	V_{OUT} = V_{DD} − 0.5 V (Note 5)	—	1.2	2.2	kΩ	O1 to O80
	M Level	R_{OM}	—	V_{OUT} = V_2 ± 0.5 V (Note 5)	—	1.2	2.2		
		R_{OM}	—	V_{OUT} = V_3 ± 0.5 V (Note 5)	—	1.2	2.2		
	L Level	R_{OL}	—	V_{OUT} = V_5 + 0.5 V (Note 5)	—	1.2	2.2		
Current Consumption (Note 6)		I_{SS}	—	V_{DD} = 5.5 V V_5 = −2.5 V f_{FR} = 35 Hz f_{SCP} = 2.5 MHz V_{IH} = 5.5 V, V_{IL} = 0 V Input Data: every bit inverted	—	400	700	μA	V_{SS}
Current Consumption (Note 7)		I_{SS}	—	As mentioned above	—	100	200	μA	V_{SS}

Note 5: V_{DD} = 3.0 V, V_5 = −9.8 V, V_2 = V_{DD} −2 / 9 (V_{DD} − V_5), V_3 = V_{DD} −7 / 9 (V_{DD} − V_5)
Note 6: Internal data receiver operating
Note 7: Internal data receiver sleeping

AC Characteristics



Test Conditions (1) (**Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, $V_0 = V_{DD}$, $V_5 = (V_{DD} - 28)$ to $(V_{DD} - 11)$ V, Ta = −20 to 75°C**)

Item	Symbol	Test Condition	Min	Max	Unit
Operating Frequency	t_{SCP}	—	—	10.0	MHz
SCP Pulse Width	t_{CWH}	—	40	—	ns
	t_{CWL}	—	40	—	
Data Set−up Time	t_{DSU}	—	15	—	
Data Hold Time	t_{DHD}	—	5	—	
SCP Rise / Fall Time	t_r, t_f	—	—	(Note 9)	
LP Set−up Time	t_{LRP}	—	5	—	
LP Hold Time	t_{LFP}	—	15	—	
LP Pulse Width	t_{LW}	—	15	—	
SCP−Rise−to−LP−Rise Time	t_{SL}	—	10	—	
LP−Fall−to−SCP−Fall Time	t_{LS}	—	17	—	
EIO IN Set−up Time	t_{EIRP}	—	5	—	
EIO IN Hold Time	t_{EIFP}	—	15	—	
EIO IN Pulse Width	t_{EIW}	—	15	—	
SCP−Rise−to−EIO−Rise Time	t_{SE}	(Note 8)	0	—	
EIO−Fall−to−SCP−Fall Time	t_{ES}	(Note 8)	20	—	
EIO OUT Data Delay Time	t_{EOD}	—	—	55	
EIO OUT Hold Time	t_{EOH}	—	—	30	

Note 8: C_L = 10 pF

Note 9: t_r, $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leq 50$ ns

Test Conditions (2) (**Unless Otherwise Noted** V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V, $V_0 = V_{DD}$, $V_5 = (V_{DD} - 28)$ to $(V_{DD} - 11)$ V, Ta = −20 to 75°C)

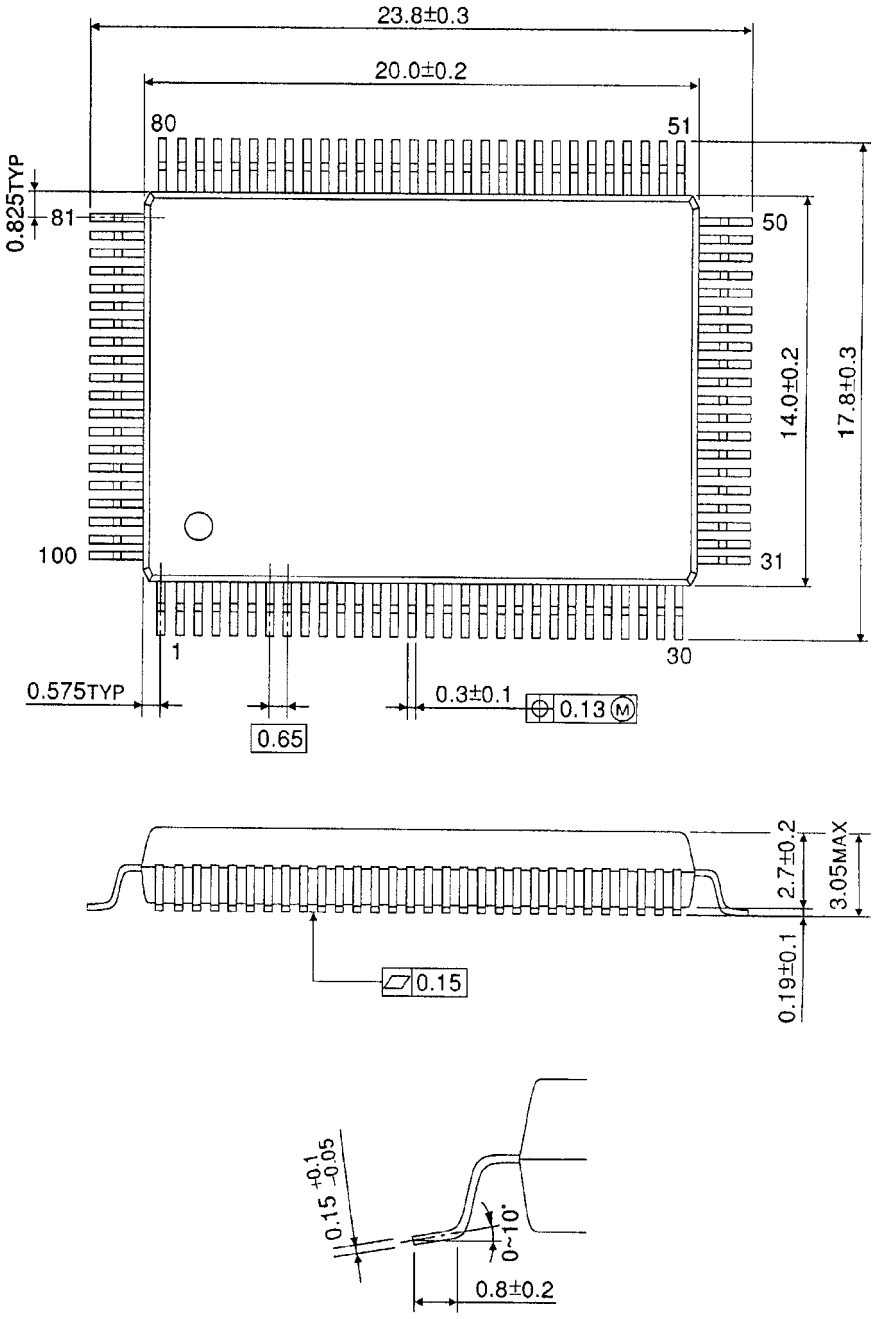
Item	Symbol	Test Condition	Min	Max	Unit
Operating Frequency	t_{SCP}	—	—	6.5	MHz
SCP Pulse Width	t_{CWH}	—	50	—	ns
	t_{CWL}	—	50	—	
Data Set−up Time	t_{DSU}	—	30	—	
Data Hold Time	t_{DHD}	—	10	—	
SCP Rise / Fall Time	t_r, t_f	—	—	(Note 11)	
LP Set−up Time	t_{LRP}	—	8	—	
LP Hold Time	t_{LFP}	—	30	—	
LP Pulse Width	t_{LW}	—	30	—	
SCP−Rise−to−LP−Rise Time	t_{SL}	—	20	—	
LP−Fall−to−SCP−Fall Time	t_{LS}	—	40	—	
EIO IN Set−up Time	t_{EIRP}	—	10	—	
EIO IN Hold Time	t_{EIFP}	—	30	—	
EIO IN Pulse Width	t_{EIW}	—	30	—	
SCP−Rise−to−EIO−Rise Time	t_{SE}	(Note 10)	0	—	
EIO−Fall−to−SCP−Fall Time	t_{ES}	(Note 10)	33	—	
EIO OUT Data Delay Time	t_{EOD}	—	—	80	
EIO OUT Hold Time	t_{EOH}	—	—	43	

Note10: C_L = 10 pF

Note11: t_r, $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leq 50$ ns

Package Dimensions

QFP100-P-1420-0.65A Unit : mm



Weight : 1.60g (Typ.)

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