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PRELIMINARY DATA

4 WORD X 4 BIT REGISTER FILE (3-STATE)

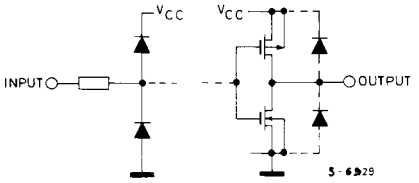
DESCRIPTION

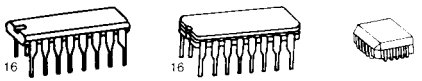
The M54/74HC670 is a high speed CMOS 4 WORD X 4 BIT REGISTER FILE (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC/74HC670 is a 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed
  t_{PD} = 17 ns (Typ) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}|$ = I_{OL} = 4 mA (Min.)
- Balanced Propagation Delays
  t_{PLH} = t_{PHL}
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 54/74LS670

INPUT AND OUTPUT EQUIVALENT CIRCUIT

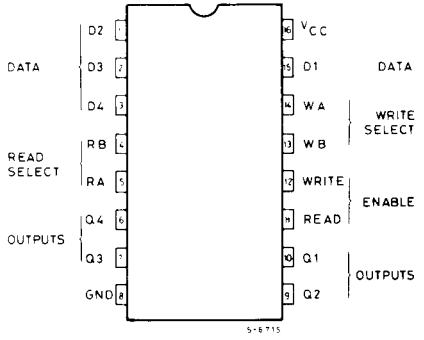




B1	F1	C1
Plastic Package	Ceramic Package	Chip Carrier

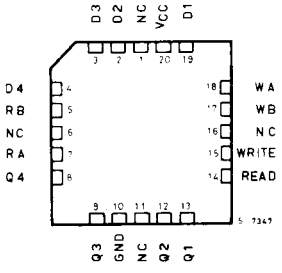
ORDERING NUMBERS: M54HC670 F1
M74HC670 B1
M74HC670 F1
M74HC670 C1

PIN CONNECTIONS
(top view)



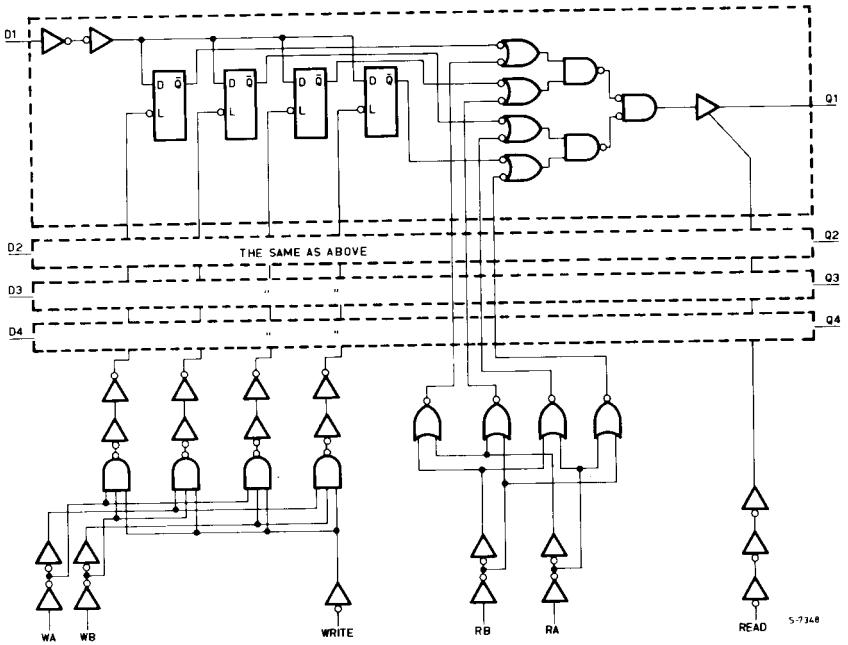
Dual in line

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM



TRUTH TABLE

WRITE FUNCTION

WRITE INPUTS			WORD			
WS	WA	GW	0	1	2	3
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
*	*	H	Q0	Q0	Q0	Q0

READ FUNCTION

READ INPUTS			OUTPUTS			
RB	RA	GR	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
*	*	H	Z	Z	Z	Z

Note: A, *: Don't Care. Z: High Impedance
B, (Q = D) = The four select internal flip-flop outputs will assume the state applied to the four external data inputs.
C, Q0 = The level of Q before the indicated input conditions were established.
D, W0B1 = The first bit of word 0, etc.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
Tstg	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_I	I_O	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	or		—	0	0.1	—	0.1	—	0.1	
		4.5	V_{IL}	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{OZ}	3-State Output Off-State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND		—	—	±0.5	—	±5		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND I_O = 0		—	—	4	—	40		80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	CL (pF)	54HC and 74HC			Unit
			MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time	15		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (READ-QN)	15		17	27	ns
t_{PLH} t_{PHL}	Propagation Delay Time (WEN-QN)	15		19	30	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DN-QN)	15		16	26	ns
$t_{W(L)}$	Minimum Pulse Width (WEN)	15		8	15	ns
t_s	Minimum Set-up Time (DATA-WEN)	15		—	10	ns
t_s	Minimum Set-up Time (WADD-WEN)	15		—	0	ns
t_h	Minimum Hold Time (DATA-WEN)	15		—	5	ns
t_h	Minimum Hold Time (WADD-WEN)	15		—	0	ns
t_{PZL} t_{PZH}	3-STATE Output Enable Time	15		9	15	ns
t_{PLZ} t_{PHZ}	3-STATE Output Disable Time	5		9	15	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Q	2.0		—	22	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{PLH} t_{PHL}	Propagation Delay Time (RA-Q)	2.0		—	67	160	—	195			ns
		4.5		—	20	32	—	39			
		6.0		—	17	28	—	34			
t_{PLH} t_{PHL}	Progation Delay Time (WE-Q)	2.0		—	76	175	—	210			ns
		4.5		—	22	35	—	42			
		6.0		—	19	30	—	36			
t_{PLH} t_{PHL}	Progation Delay Time (D-Q)	2.0		—	63	150	—	180			ns
		4.5		—	19	30	—	36			
		6.0		—	17	26	—	31			
$t_{W(L)}$	Minimum Pulse Width	2.0		—	16	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time (D-WE)	2.0		—	—	50	—	60			ns
		4.5		—	—	10	—	12			
		6.0		—	—	9	—	11			
t_s	Minimum Set-up Time (WA-WE)	2.0		—	—	0	—	0			ns
		4.5		—	—	0	—	0			
		6.0		—	—	0	—	0			
t_h	Minimum Hold Time (D-WE)	2.0		—	—	25	—	30			ns
		4.5		—	—	5	—	6			
		6.0		—	—	4	—	5			
t_h	Minimum Hold Time (WA-WE)	2.0		—	—	0	—	0			ns
		4.5		—	—	0	—	0			
		6.0		—	—	0	—	0			
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0		—	32	39	—	110			ns
		4.5		—	11	18	—	22			
		6.0		—	10	16	—	19			
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0		—	29	105	—	130			ns
		4.5		—	15	21	—	26			
		6.0		—	17	18	—	22			
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance			—	44	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$