agere systems

Product Brief
April 2002

CSP1037—AC-Link Soft Modem Chip Set

Features

- Two-chip AC-link modem solution
  - — CSP1037
  - — CSP1037B
- Data mode capabilities:
  - — ITU-T V.92*: 56000 bits/s—28000 bits/s
  - — ITU-T V.90*: 56000 bits/s—28000 bits/s
  - — ITU-T V.34: 33600 bits/s—2400 bits/s
  - — V.44, V.42, V.42bis, and *MNP*® Class 5 data compression
  - — V.32terbo, V.32bis, and fallbacks
  - — High compression throughput due to parallel access directly to the host PC
- FAX mode capabilities:
  - — ITI-T T.31 class 1 FAX
  - — ITU-T V.34: 33600 bits/s—2400 bits/s (TCM)
  - — ITU-T V.17: 14400 bits/s, 12000 bits/s, 7200 bits/s (TCM)
  - — ITU-T V.29: 9600 bits/s, 7200 bits/s (QAM)
  - — ITU-T V.27ter: 4800 bits/s, 2400 bits/s (DPSK)
  - — ITU-T V.21 Channel 2: 300 bits/s (FSK)
- Complete DAA includes the following:
  - — AC‘97/MC‘97 2.2 compliant
  - — International line interface
  - — Compliant with FCC, CTR21, JATE, and other PTTs
  - — 3.3 V to 5 V power supply
  - — 2400 V isolation
  - — Integrated ring detector
  - — Integrated analog front end (AFE)
  - — 2-wire to 4-wire hybrid
  - — Low-power standby mode
  - — Low-profile SOIC packages
- Operating system support:
  - — *Windows*® 98, 98SE, 2000, *NT*® 4.0, ME, *XP*™
  - — PC 2001compliant
  - — ACPI compliant
- Applications:
  - — Modem riser cards (MR)
  - — Modem daughter cards (MDC)
- Packaging options:
  - — SOIC: for standard MR and MDC applications
  - — TSSOP: for small foot print applications

Introduction

The CSP1037 chip set is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet international telephone line requirements. The CSP1037 chip set is available in two 16-pin small outline packages (AC‘97 interface on SCP and telephone line interface on CSP1037B). The chip set eliminates the need for an AFE, an isolation transformer, relays, optoisolators, and a 2-wire to 4-wire hybrid. The CSP1037 chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. SCP complies with AC‘97/MC‘97 Interface Specification Rev. 2.2.

The CSP1037 set is an ITU-T recommendation V.92/V.44 solution. V.92 and V.44 have four innovative features designed to improve modem performance in the internet environment. The features are as follows:

- Modem fast connect: faster start-up times.
- Modem on hold†: switch between modem and an incoming phone call without losing the data connections.
- PCM upstream: send data to central site at rates approaching 48 kbits/s.
- Data compression enhancement focused on today’s internet traffic.

* Actual speeds over U.S. telephone lines vary and are less than 56K, due to current FCC regulations and line conditions.
† Modem on hold functionality requires call waiting services.

Functional Description

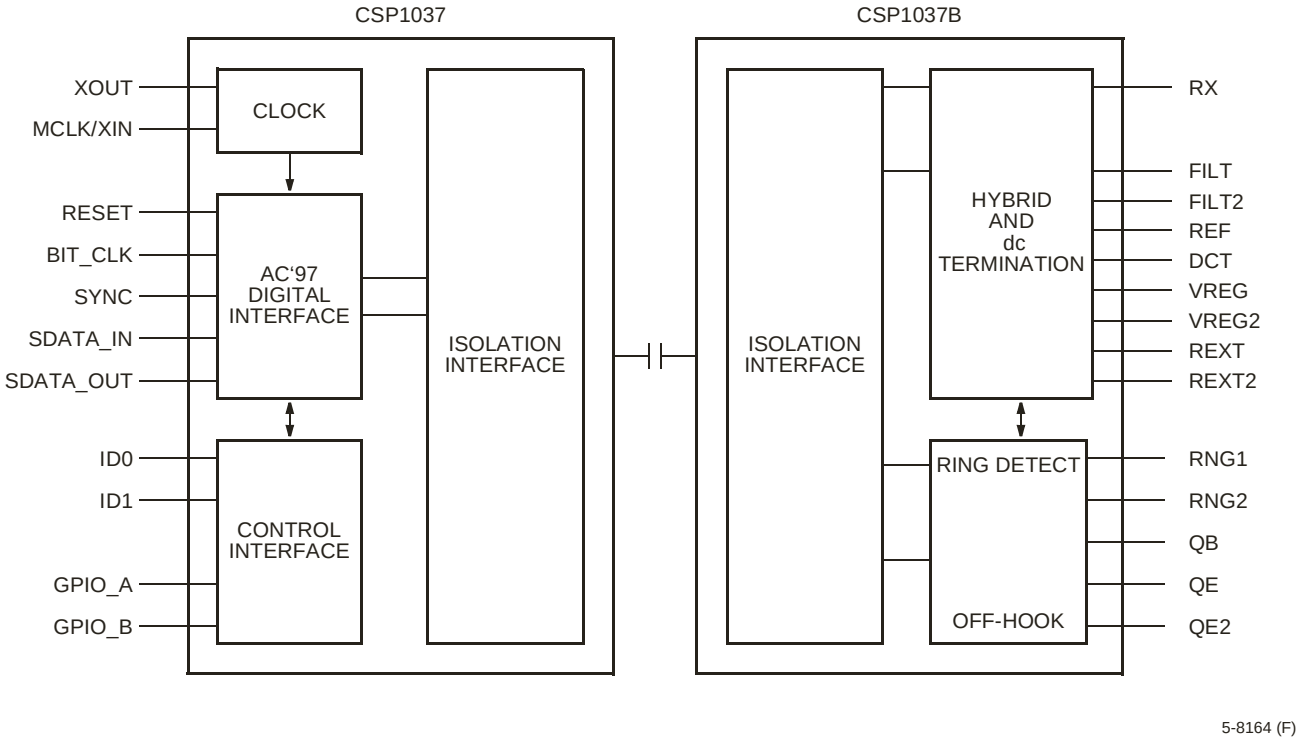

Figure 1. Functional Block Diagram

The CSP1037 chip set is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet international telephone line requirements. The CSP1037 chip set is available in two 16-pin small outline packages (AC'97 interface on CSP1037 and telephone line interface on CSP1037B). The chip set eliminates the need for an AFE, an isolation transformer, relays, optoisolators, and a 2-wire to 4-wire hybrid. The CSP1037 chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The CSP1037 complies with AC'97/MC'97 Interface Specification Rev. 2.1.

The chip set is fully programmable to meet worldwide telephone line interface requirements, including those described by CTR21, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the CSP1037 chip set include ac termination, dc termination, ringer impedance, and ringer threshold. The CSP1037 chip set has been designed to meet stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

The CSP1037 chip set achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Agere's proprietary signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common-mode interference, or noise coupling. All transmit, receive, control, and ring detect data are communicated through this barrier.

V.92 and V.90 Technology

ITU-T recommendations V.92 and V.44 are the new international standards for analog modems. They improve the features of the former standards V.90 and V.42bis with simple yet powerful changes designed to enhance the internet experience. The new features of V.92 are as follows:

- Fast connect, which decreases start-up times on recognized connections.
- Modem on hold*, which allows the user to place the modem on hold when an incoming call is identified, when call waiting services are available.
- PCM upstream, which increases the upstream transmission rate up to 48 kbits/s under the best line conditions.

V.44 updates the older compression standardf V.42bis. V.42bis was created ten years ago and predates the World Wide Web. V.44 addresses the content changes from the last ten years and can provide significantly increased throughput.

Although the central-site architecture is beginning to move towards V.92, most of the existing infrastructure only supports V.90 equipment. The CSP1037 chip set supports both V.92 and V.90 with a fallback to V.34 for connections where a V.92 or V.90 connectionis not negotiated.

AC-Link

The AC-Link is a bidirectional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams and control register access employing a time-division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into twelve outgoing and twelve incoming data streams, each with 20-bit sample resolution.

The AC-link serial interconnect defines a digital data and control pipe between the controller and the codec. The AC-link supports twelve 20-bit slots at 48 kHz on SDATA_IN and SDATA_OUT. The TDM slot-based architecture supports a per-slot valid tag infrastructure that is the source of each slot's data sets or clears to idicate the validity of the slot data within the current frame. For modern AFE, data streams at a variety of required sample rates can be supported.

Isolation Barrier

The CSP1037 chip set achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with proprietary signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common-mode interference, or noise coupling. All transmit, receive, control, and ring detect data are communicated through this barrier.

The communications link is disabled by default. The PR bits in register 3Eh must be cleared, and the sample rate must be set in register 40h/42h. No communication between SCP and the CSP1037B can occur until these conditions are set.

* This feature is dependant on the country specific call waiting service. Not all countries are supported.

Ordering Information

Table 1. CSP1037 Ordering Information

Device	Package	Comcode	Remarks
CSP1037	SOIC, 16-pin, small-outline	108500117	—
CSP1037B	SOIC, 16-pin, small-outline	108500109	For international use
CSP1037-16T	TSSOP, 16-pin, thin shrink small-outline	109061416	Extended temperature: 0—90 °C
CSP1037B-16T	TSSOP, 16-pin, thin shrink small-outline	109061390	Extended temperature: 0—90 °C
CSP1037-16T70*	TSSOP, 16-pin, thin shrink small-outline	700023261	Commercial grade: 0—70 °C
CSP1037B-16T70*	TSSOP, 16-pin, thin shrink small-outline	700023262	Commercial grade: 0—70 °C

* All specifications for commercial grade and extended temperature parts are the same as the specifications for the SOIC package except for the pin configuration of the CSP1037. The SOIC and TSSOP pin configurations for the CSP1037B are the same for both packages.

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