ZL70250

Ultra Low Power RF Transceiver

Shortform Data Sheet

January 2010

Features

- Ultra Low Power
  - Tx & Rx current: <2 mA
  - Standby current: <500 nA
  - Supply: 1.2 V to 1.8 V typical
- Radio Frequency
  - IC range: 795-965 MHz
  - North American ISM band: 902-928 MHz
  - European SRD bands: 863-870 MHz
- Radio Performance
  - Bit rate: up to 186 kbits/s (raw)
  - Tx power: up to +2 dBm
  - Rx sensitivity: -90 dBm at full rate
- Very few external components
  - Only crystal & bias resistor
- Standard interfaces
  - SPI data port
  - 2-wire control port
- MAC
  - Digital RSSI and Blocker Indicator
  - Clear Channel Assessment
  - Sniff with automatic receive or standby
  - Automatic Clear-to-Send, Turn-around and Standby
  - Receiver AGC
  - Packetization
  - Preample & sync
  - Whitening

Ordering Information

Pb-free Solder bumped die - ZL70250UDJ4
QFN-40; 6mm x 6mm (for evaluation only)

Applications

- Battery powered Applications in Body Area Networks
- Applications relying on energy harvesting
- Short range communications with very long battery life
- Wireless sensors
- Remote controls
- Voice communication

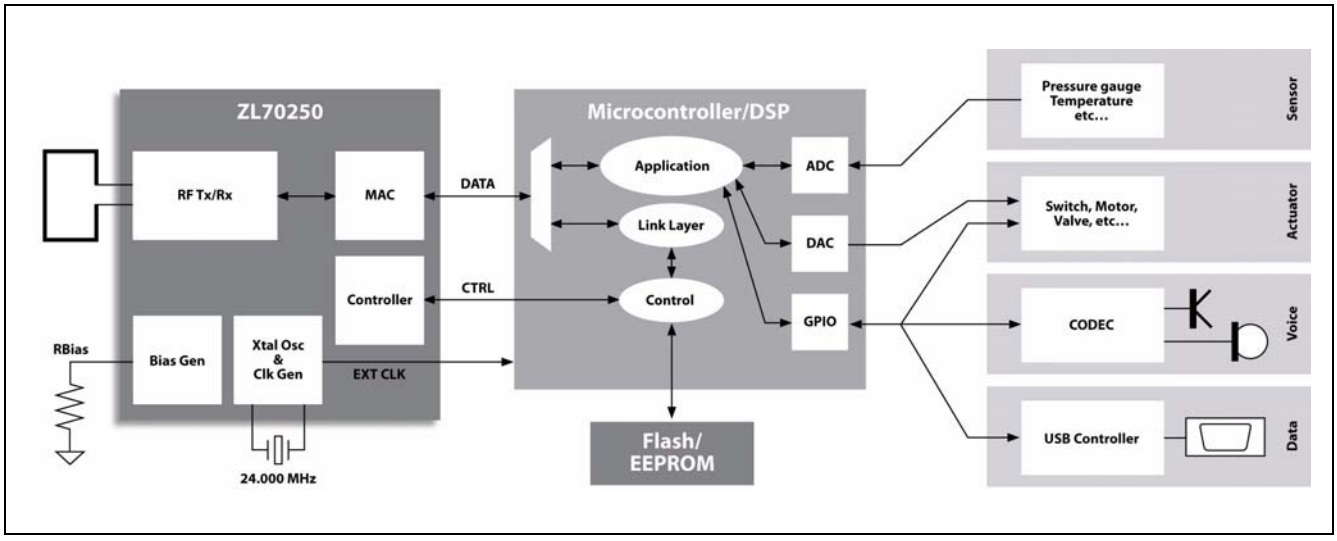

Figure 1 - ZL70250 Typical Applications

Description

The ZL70250 ultra low-power radio frequency (RF) transceiver provides a wireless link in applications where power consumption is of primary importance. The transceiver's ultra low-power requirements allows the use of a miniature button cell battery or energy-harvesting methods, enabling devices with extremely small form factor.

The availability of the transceiver as bumped die combined with the extremely low number of external components also contributes in minimizing the application footprint.

The ultra low-power IC operates in unlicensed frequency bands between 795 – 965 MHz and offers data rates up to 186 kbps to support voice communication. Duty cycling can be employed for applications that require lower average payload to further reduce power consumption.

The device includes the RF transceiver as well as a Media Access Controller (MAC) that performs most link support functions including Received Signal Strength Indication (RSSI), Clear Channel Assessment (CCA), sniff, preamble & sync, packetization and whitening. The device uses standard interfaces, enabling easy integration with a standard microcontroller or Digital Signal Processor (DSP).

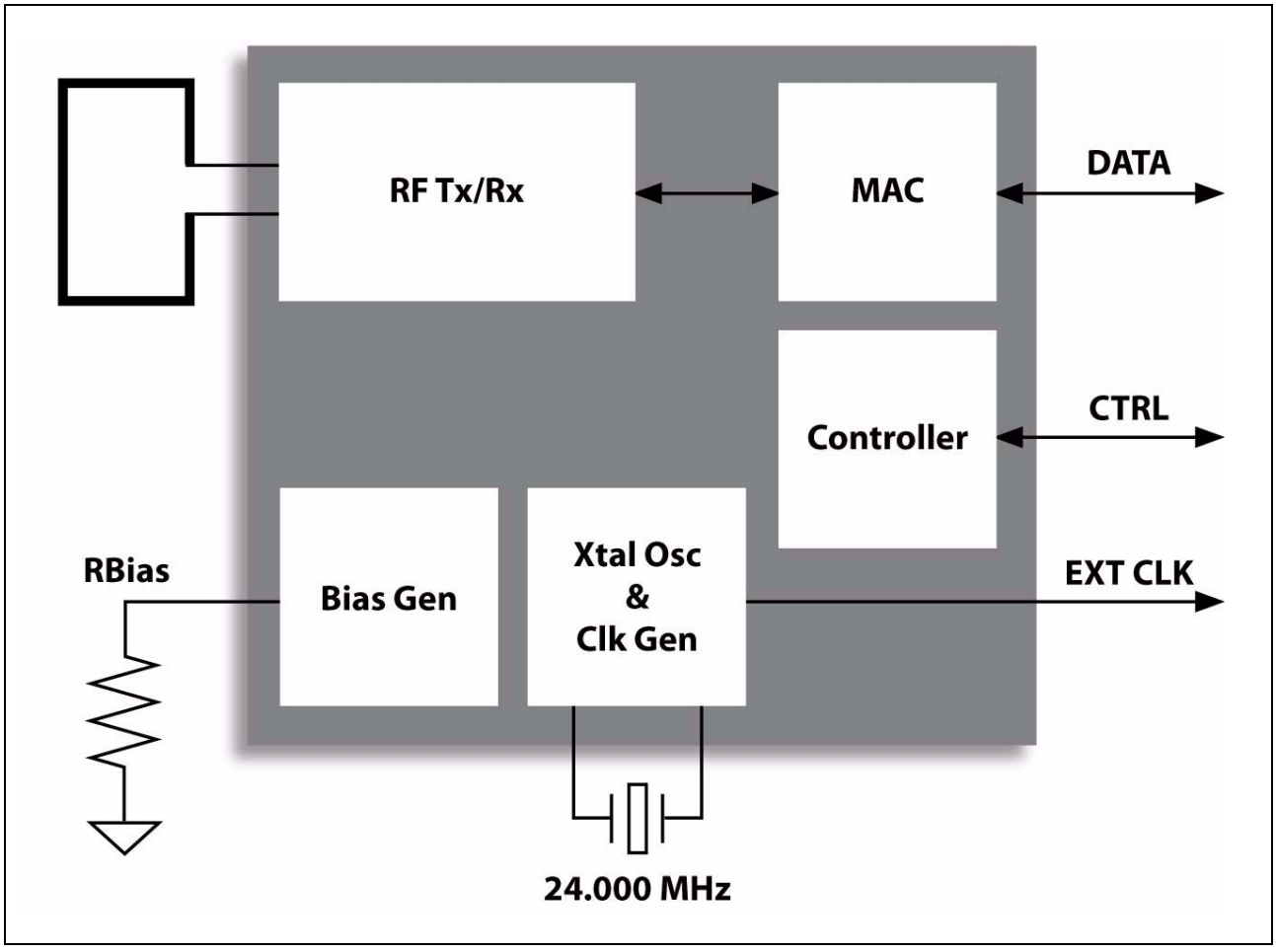

Figure 2 - Simplified Block Diagram

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List of Figures

1.0 Change Summary

Changes from January 2008 Issue to January 2010 Issue.

Page	Item	Change
15	6.1, “Pinout“	Updated the description for AMX and VDDTEST pins.

2.0 Introduction

The ultra low-power ZL70250 RF transceiver IC (Integrated Circuit) makes RF telemetry possible in applications where very low power requirements made it unrealistic until now. As illustrated below, end-applications may include wireless sensors, Body Area Networks - principally on-body sensors - or voice communication.

With a typical current consumption below 2 mA in both transmit (-10 dBm) and receive, and a data rate up to 186 kbit/s, the ZL70250 IC enables bi-directional RF links with an impressive efficiency of 13nJ/bit over a range up to a couple hundred meters.

The output power is programmable and can be reduced down to -25 dBm to save power in cases where the link budget allows it or increased up to +2 dBm for more range or to allow for system losses, like a very small antenna or body tissue absorption.

In order to achieve the minimum possible power consumption, the ZL70250 offers a large number of optimization parameters, all available to the user via the control interface. To streamline the setup and optimization process, most parameters have an on-chip automatic trim capability. The frequency tuning is also highly automated.

Despite its very low power consumption, the ZL70250 also includes a highly flexible MAC (Media Access Controller) that offers all the basic functions needed to implement a link layer with the minimum amount of data transfer between the ZL70250 and its controller. Some of the capabilities are listed below:

- Digital RSSI and Blocker Indicator
- Clear Channel Assessment
- Transmit with automatic Clear to Send
- Sniff with automatic receive or standby
- Receiver AGC (programmable)
- Preamble and Sync
- Whitening
- Packetization with programmable size for both transmit and receive
- Automatic standby after receive
- Automatic turn-around for bi-directional data transfer

The ZL70250 is also highly integrated: beside the antenna and, in some cases, its matching network, only a crystal and a reference resistor are required. Available as a 2 mm x 3 mm bumped die, the IC enables applications with a very small footprint.

3.0 Regulatory Compliance

The ZL70250 IC is designed for low emissions to help the final product comply with FCC Part 15 and the European pr ETS 300-220. However, because the standards apply to the complete end product and not the IC alone, the end product manufacturer is responsible for EMC testing and meeting EMC standards in all countries in which the system is sold.

The following regulations also apply.

EN301 357 - 1,2

EN301 489 - 1,9

4.0 Interface Specifications

4.1 Control Port

4.1.1 Functional Description

The Control Port is used to program the ZL70250 RF transceiver.

At the bit level the ZL70250 control interface is a standard 2-wire slave with a max speed of 400 KHz. The bit level protocol is shown in Section 4.1.2, “Bit-level Protocol“ below.

The ZL70250 Control Port differs slightly from the standard 2-wire protocol at the byte sequencing level due to the addition of some extra functionality.

4.1.2 Bit-level Protocol

The figure below shows the basic bit protocol for a transfer on the 2-wire bus. The first byte provides a 7-bit Device ID, and 1 bit for Read/Write indication. All byte transfers are 9-bits, with the 9th bit being the acknowledge bit. At the bit level, the ZL70250 2-wire protocol is identical to a standard 2-wire protocol.

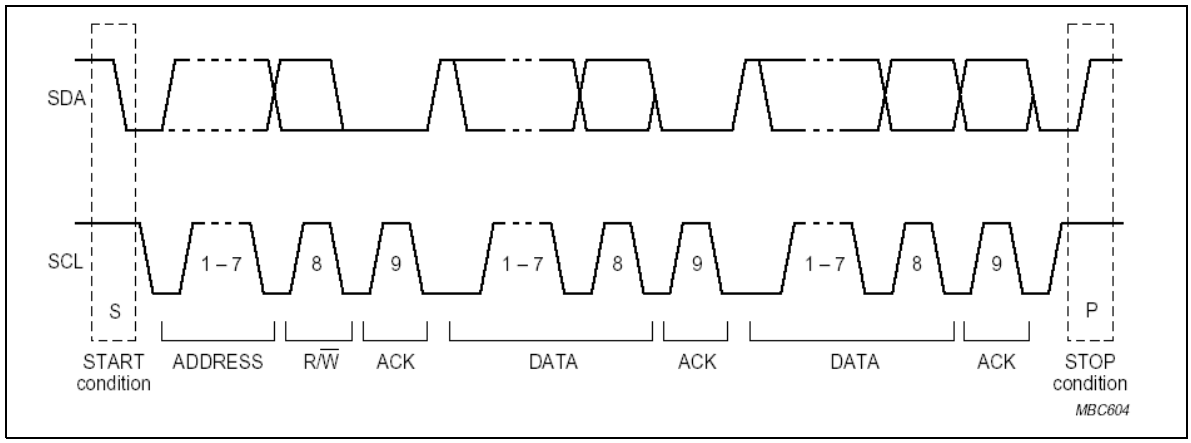


Figure 3 - Bit-level Protocol

4.2 Data Port

4.2.1 Functional Description

The Data Port controls the transfer of data between the ZL70250 RF transceiver and the controller.

The Data Port is configurable as SPI or various PCM modes. For PCM, both wide Frame Sync and narrow Frame Sync are supported. In PCM mode, the Clock and Frame Sync can be any polarity. In both SPI and PCM Modes, ZL70250 is the Master, and data is clocked in and out at the fixed bit rate of the RF Interface.

The Data Port supports 5 basic modes of operation:

- bi-directional transmit/receive of multiple packets
- transmit one packet
- transmit multiple packets
- receive one packet
- receive multiple packets

In both SPI and PCM mode, data_out is not tri-stated. This implies that outgoing and incoming traffic needs to happen on separate lines.

DATA PORT SPI External AC Specifications						
Parameter	**Sym.**	**Conditions**	**Min.**	**Nom**	**Max.**	**Unit**
Rise Time (20% - 80%)	T_R	C_{LOAD} = 200pF R_{PULLUP} = 8kΩ			50	nS
Fall Time (80% - 20%)	T_F	C_{LOAD} = 200pF I_{LOAD} = 1mA			50	nS
Clock Period	T_{CP}	Receive Mode	4.45	5.37	6.30	uS
Clock Low	T_{CL}	Receive Mode	2.63	2.68	2.73	uS
Clock High	T_{CH}	Receive Mode	1.73	2.68	3.63	uS
Rx Data Setup	T_{RSU}	Receive Mode	1.50	2.68		uS
Rx Data Hold	T_{RH}	Receive Mode	-100			nS
Rx Data Out	T_{RCO}	Receive Mode			200	nS
Tx Data Setup	T_{TSU}	Transmit Mode	200			nS
Tx Data Out	T_{TCO}	Transmit Mode			1000	nS
Tx Data Hold	T_{TH}	Transmit Mode	-1000			nS

Table 1 - Data Port, SPI Timing Specifications

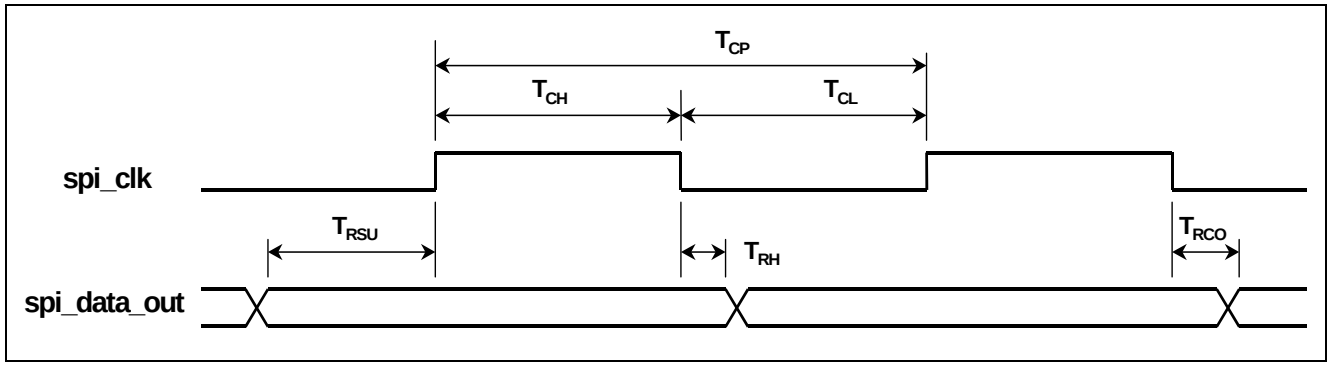


Figure 4 - SPI Receive Timing, ZL70250 to Controller

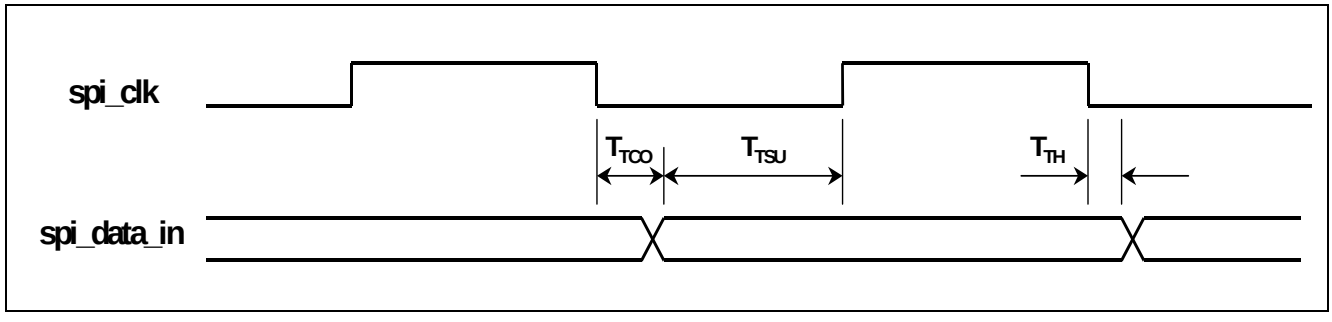


Figure 5 - SPI Transmit Timing, Controller to ZL70250

4.2.2 SPI Data Packet

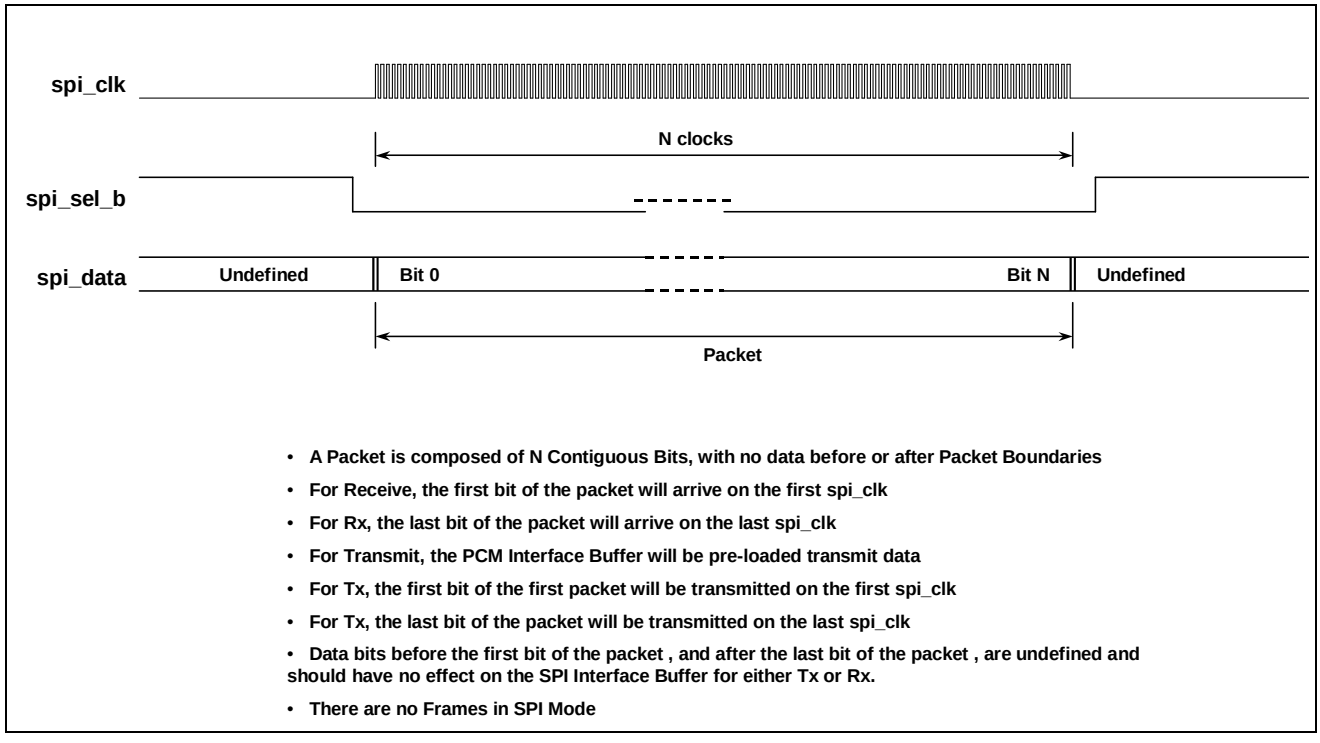


Figure 6 - SPI Data Packet

4.2.3 SPI Functional Timing Diagrams

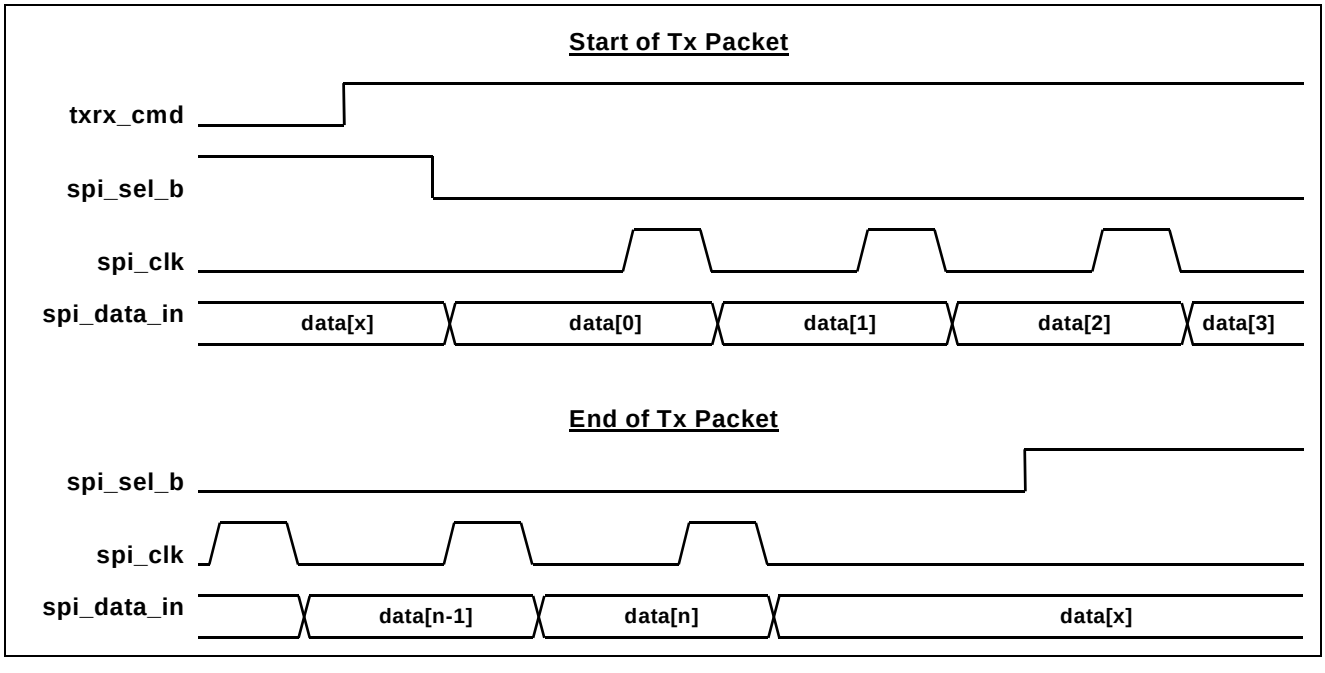


Figure 7 - Functional SPI Transmit Timing, Controller to ZL70250

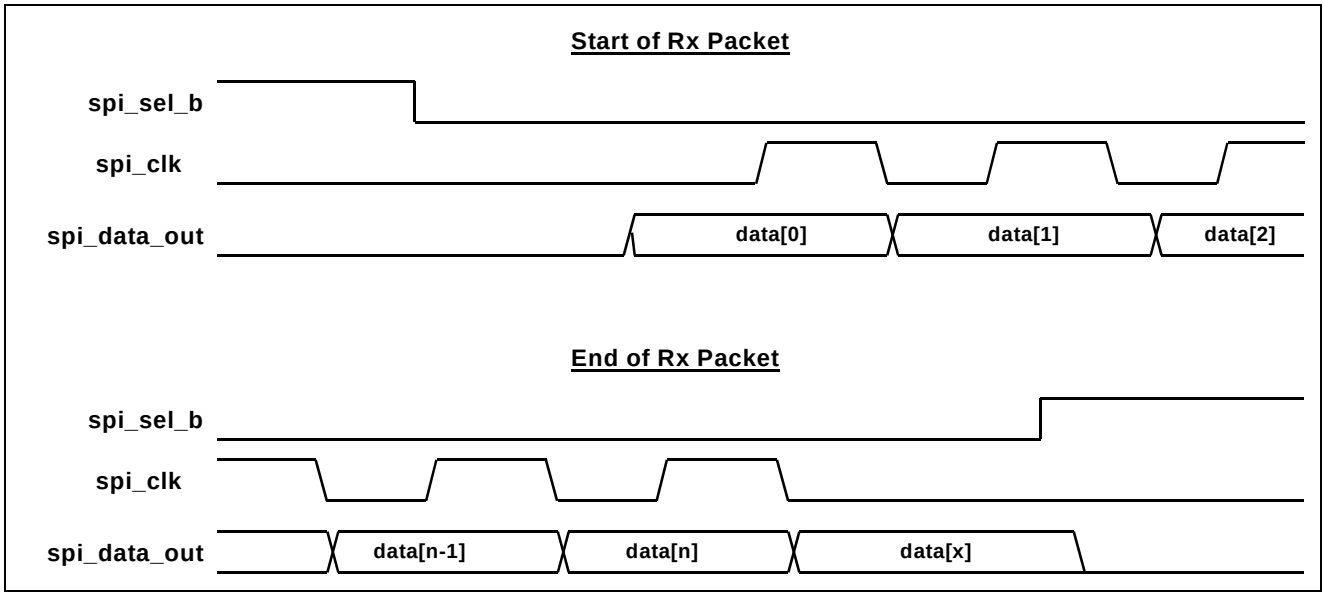


Figure 8 - Functional SPI Receive Timing, ZL70250 to Controller

4.2.4 PCM Data Packet

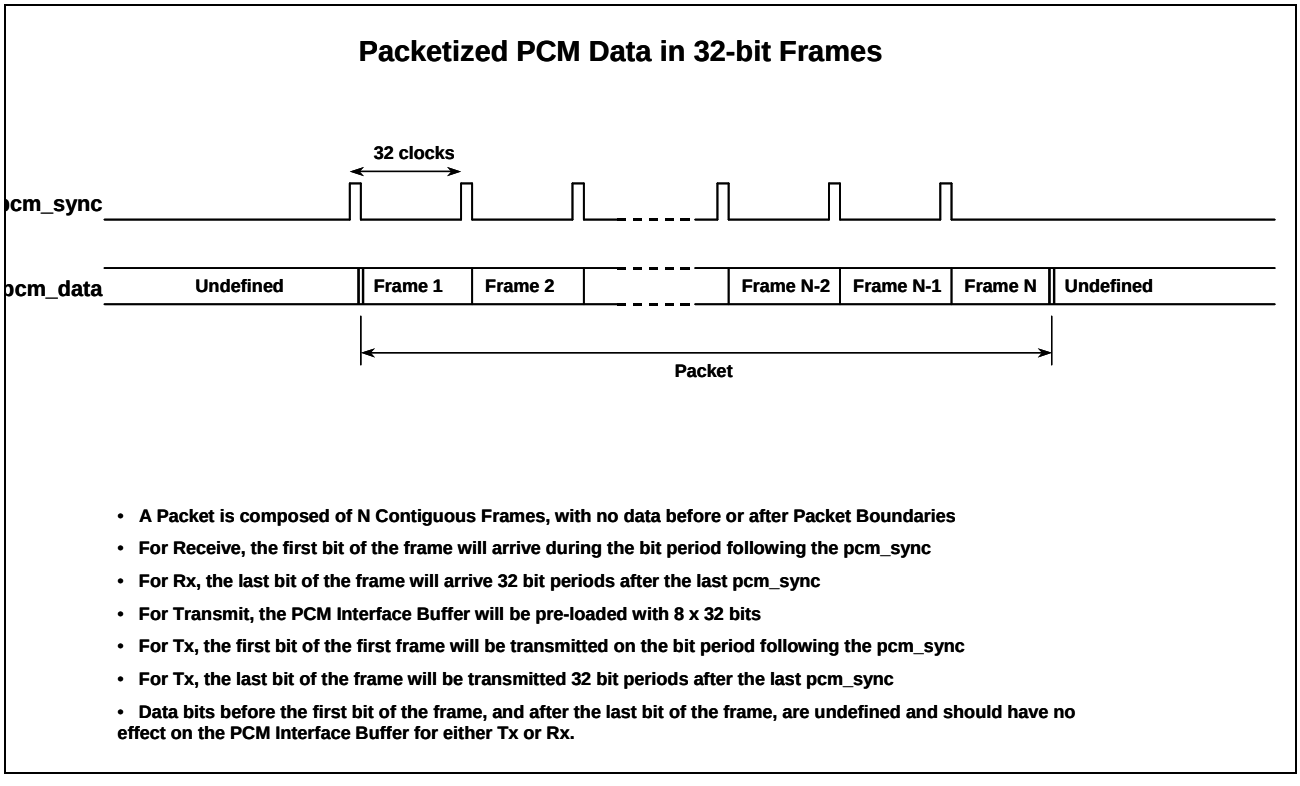


Figure 9 - PCM Data Packet with 32 Bit Frame

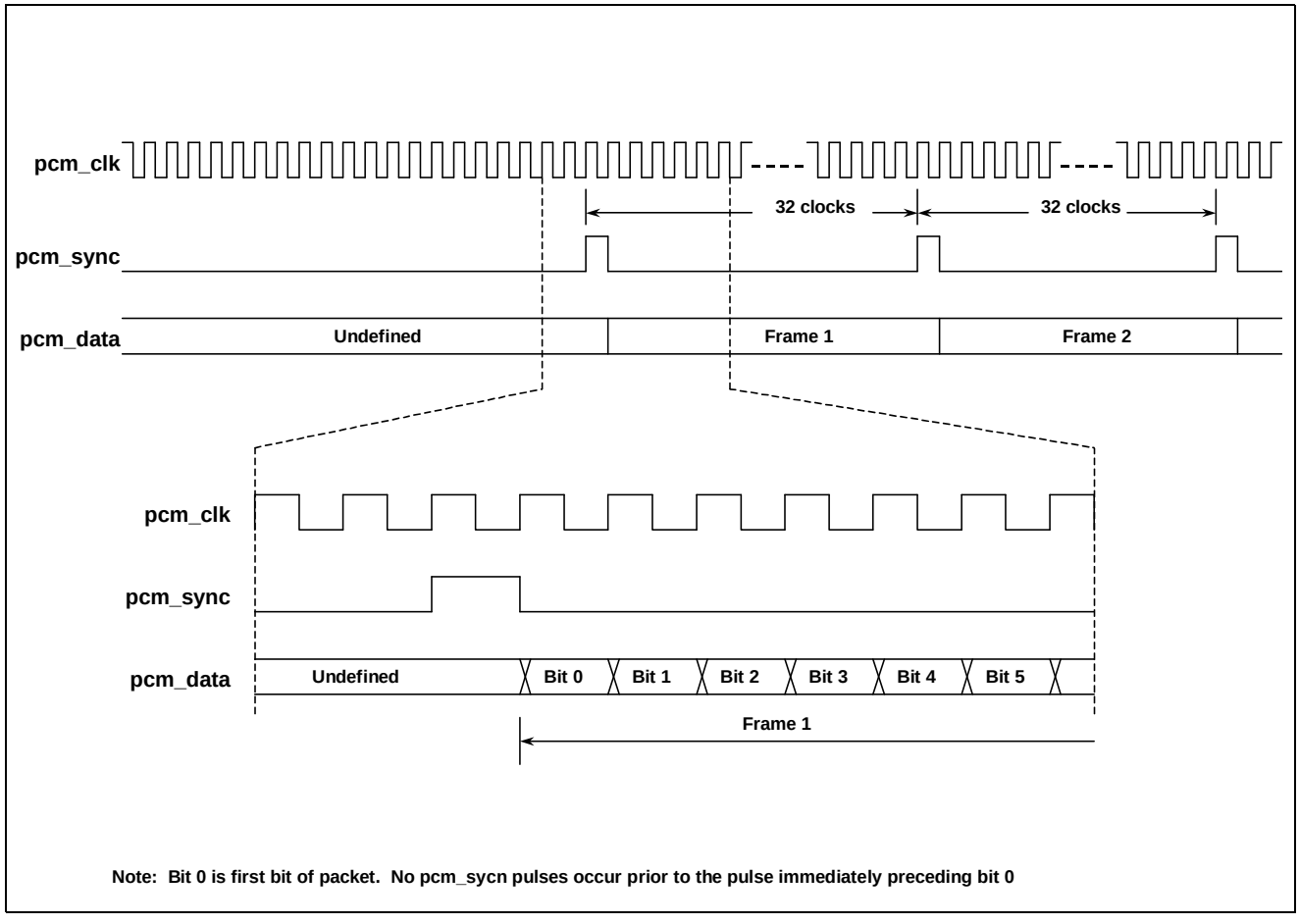


Figure 10 - PCM Start of Packet

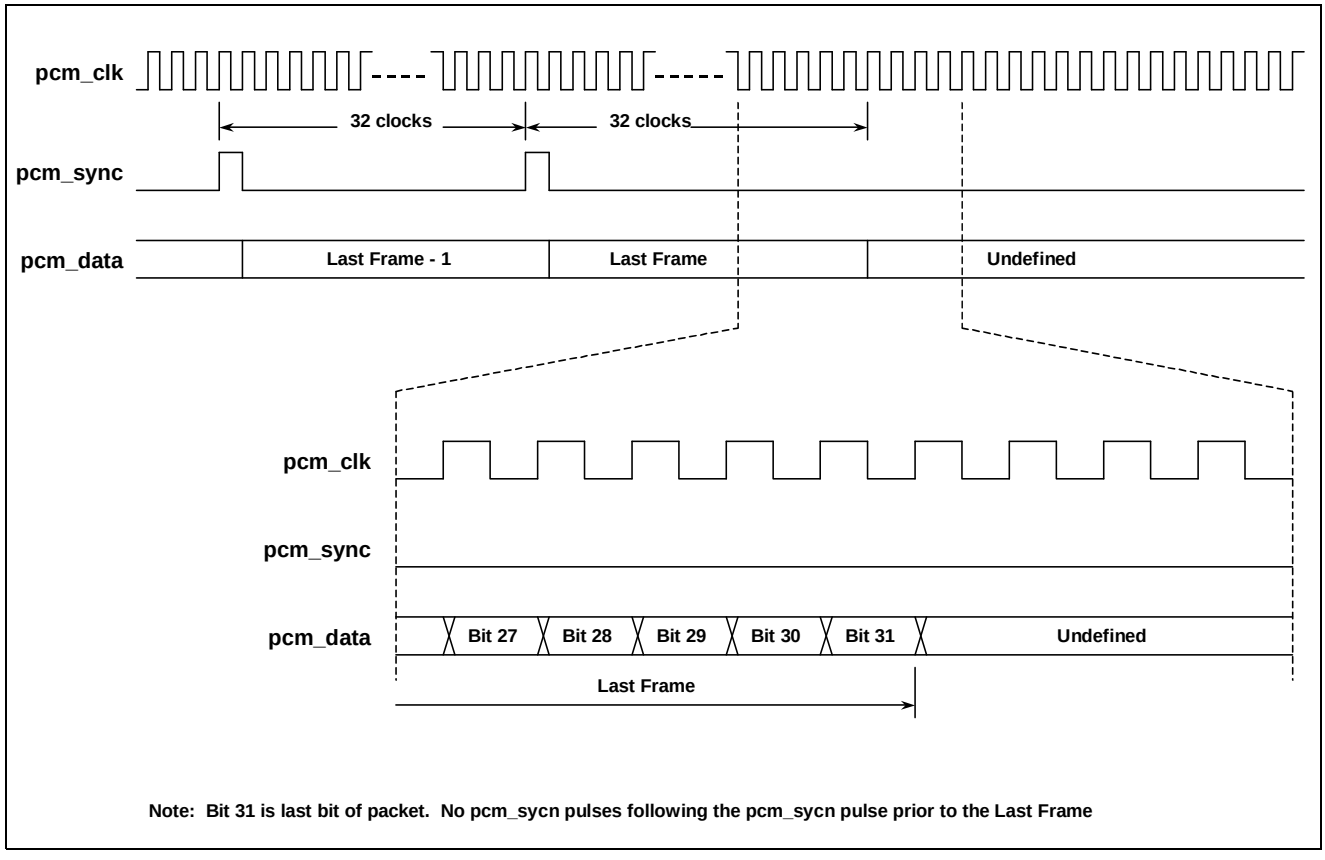


Figure 11 - PCM End of Packet

5.0 Electrical Specifications

5.1 Maximum Ratings

Characteristics	Symbol	Maximum Ratings	Unit	Notes
Supply Voltage	Vdd	2.5V	V	
Reverse Supply Voltage		0.3	V	at least 20 mA at -1.5 V
Input Voltage	Vin	RF: -0.3 to Vdd + 1.5V Analog: -0.3 to 2.5V Digital: -0.3 to 2.5V	V peak referred to VSS	
Storage Temperature	Tstg	-40 to +85	°C	
Electro Static Discharge[1]	ESD	500 RF pads, 1.5 K all others	V	(Note 1)

Note 1: Applied one at a time. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Human body model.

Table 2 - Maximum Ratings

5.2 Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	Vdd_sp	1.1	1.2 - 1.8	2	V	Full specs
Supply Voltage	Vdd_op	1.0	1.2 - 1.8	2	V	Operational
Operating Temperature	Top	-10		70	°C	

Table 3 - Operating Conditions

5.3 Digital I/O DC Specifications

Parameter	Sym.	Conditions	Min.	Nom	Max.	Unit
Output High	V_{OH}	DOUTB = VSS R_{PULLUP} = 8KΩ	VDD - 0.01			V
Output Low	V_{OL}	DOUTB = VDD I_{LOAD} = 1mA			VSS + 0.1	
Input High	V_{IH}		[VDD-VSS]*0.8			V
Input Low	V_{IL}				[VDD-VSS]*0.2	V
Input Current	I_{LEAK}	SSI_{IO} = VDD or VSS	-1		1	µA

Table 4 - Digital I/O DC Specifications

5.4 Dynamic Characteristics

The specified performance of the ZL70250 are valid over a supply range of 1.1 Volts to 2 Volts. ZL70250 continues to operate such that it can receive and transmit at some range over a supply range of 1.0 Volts to 2 Volts. Additionally, all other functions operate correctly over the same supply voltage range.

Parameter	Min.	Typ.	Max.	Units and Notes
Operating Frequency Range	795		965	MHz
Standby current		0.5	5	uA (all circuits disabled or reset_b=0)
Reference Frequency		24.000 24.576		MHz
Symbol Rate		181.818 186.182		KSps (24.000MHz Xtal) KSps (24.576MHz Xtal)
Channel Separation		300 303.407		kHz (24.000MHz Xtal) kHz (24.576MHz Xtal)
Power up		3	5	ms (from RESET_B release, assuming VDD is settled)
Receiver Parameters				
Sensitivity	-90			dBm (Input level resulting in BER of 10^{-3}) Min depends on load conditions.
Input Current at 1.25 volts		1.9		mA (continuous RX mode)
RSSI Range		40		dB Note: Digital, 32 levels of 2 dB
Transmitter Parameters				
Input Current at 1.25 volts		2.0		mA (continuous TX mode)
Output Power	-25	-10	2	dBm (max depends on load conditions)

Table 5 - Dynamic Characteristics

6.0 Mechanical Specifications

6.1 Pinout

Pin #	Pin Name	I/O	A/D	Function	Connection
1	vssh	PWR	A	Ground for power amp	Ground, 0 V
2	unused				Open
3	vssa	PWR	A	Analog ground	Ground, 0 V
4	vdda	PWR	A	Analog supply voltage	Supply, 1.2 V - 1.8V
5	rbias	I	A	Bias resistor used in trim	Connect external 50 kΩ to ground.
6	amx0	I	A	Analog test bus input	Tie to ground for normal operation.
7	amx1	I	A	Analog test bus input	Tie to ground for normal operation.
8	amx2	O	A	Analog test bus output	Tie to ground for normal operation.
9	amx3	O	A	Analog test bus output	Tie to ground for normal operation.
10	vddtest	PWR	A	Supply voltage for test buffers	Tie to ground for normal operation.
11	xtal1	I	A	Crystal connection or external clock input when clksel is high.	Connect to crystal
12	xtal2	I	A	Crystal connection, leave open when using external clock source.	Connect to crystal
13	unused				Open
14	digital_test	I	D	test control	Internal 1 MΩ pulldown when driven high, 100 kΩ pulldown when low, leave open or tie to ground for normal operation.
15	reset_b	I	D	Reset when low, all circuits off (including the wclk so do not use wclk for uP and then control the reset_b with the uP). When the chip comes out of reset the programmable registers will be at default conditions, crystal oscillator and wclk on, everything else off.	Connect to uP or other reset network. Internal 1 MΩ pulldown when driven high, 100 KΩ pulldown when driven low.
16	txrx_stat	O	D	Transmit/receive mode indicator for controlling a Tx/Rx switch during normal operation	Connect to Tx/Rx switch or leave open.
17	wclk/dtbi1	O/I	D	Programmable clock output for normal operation, crystal frequency/n, where n=(4-30)	Can be used to clock uP (minimize load capacitance) or leave open and disable through SSI port.
18	scantst	I	D	Test control input	Internal 1 MΩ pulldown when driven high, 100 kΩ pulldown when low, leave open or tie to ground for normal operation
19	ssi_clk	I	D	Serial control bus clock (similar to 2-wire) ZL70250 is slave.	From uP serial port

Pin #	Pin Name	I/O	A/D	Function	Connection
20	ssi_data	I/O	D	Data input or open drain output for serial port data (similar to 2-wire) ZL70250 is slave.	External pull-up resistor required, value depends on load capacitance.
21	spi_clk	O	D	SPI master clock. Can be configured for PCM clock. See programmer's manual.	Connect to SPI or PCM uP port
22	spi_data_in	I	D	SPI data input. Can be configured for PCM data input. See programmer's manual.	Connect to SPI or PCM uP port
23	spi_data_out	O	D	SPI data output. Can be configured for PCM data output. See programmer's manual.	Connect to SPI or PCM uP port
24	spi_sel_b	O	D	SPI frame output. Can be configured for PCM frame output. See programmer's manual.	Connect to SPI or PCM uP port
25	txrx_cmd	I	D	Transmit/receive control, see programmer's manual	Control input from uP
26	irq_dtbo1	O	D	Interrupt to uP, test output - see table [below]	Connect to uP
27	vddd	PWR	A	Supply voltage for digital section	Supply, 1.2 V - 1.8 V
28	vssd	PWR	A	Ground for digital section	Ground, 0 V
29	test_dtbo0	O	D	Dedicated digital test output	Leave open or connect to testpoint.
30	test_dtbo1	O	D	Dedicated digital test output	Leave open or connect to testpoint.
31	clksel	I	D	Selects crystal oscillator when low and external clock signal when high (bypasses internal osc.)	Internal 1 MΩ pulldown when driven high, 100 kΩ pulldown when low, leave open or tie to ground for normal operation.
32	life_test/dtbi0	I	D	Selects life test mode control or serves at a digital test input	Internal 1 MΩ pulldown when driven high, 100 kΩ pulldown when low, leave open or tie to ground for normal operation.
33	vssa2	PWR	A	Analog ground	Ground, 0V
34	unused				Open
35	ant2	O	A	Power amp output (differential current)	Connect to antenna tuned to resonate at high impedance (>1k Ω for best results)
36	ant3	O	A	Power amp output (differential current)	Connect to antenna tuned to resonate at high impedance (>1k Ω for best results)
37	unused				Open

Pin #	Pin Name	I/O	A/D	Function	Connection
38	ant1	I	A	RF input amplifier (differential high impedance, internal AC coupled), Internally connected to antenna tuning capacitor bank.	Connect to antenna tuned to resonate at high impedance (>1k Ω for best results)
39	ant4	I	A	RF input amplifier (differential high impedance, internal AC coupled) Internally connected to antenna tuning capacitor bank.	Connect to antenna tuned to resonate at high impedance (>1k Ω for best results)
40	unused				Open

Note on pulldowns: Most of the digital input pads have built in pull down resistors so that if the pin is not used for normal operation no connection to the pin is required thus reducing the traces on small hybrid assemblies. If the input is used, the pull down resistor value is switched depending on the input state. If the pin is driven high, the resistor is switched to 1 MΩ to reduce the amount of pull down current. If the input is driven low or left unconnected, the pull down resistor value is 100 kΩ.

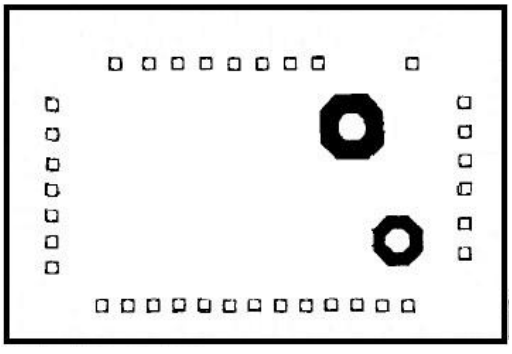
6.2 Package Mechanical Specifications

6.2.1 Solder Bumped Die

Die Size (SAW step pitch)	3.125 x 1.898 mm.
Backgrind Specification	Backgrind to 0.228 mm + / - 0.025 mm
Bump specification	electroplated, Pb-free 97.5% Sn / 2.5% Ag - 80 um bump height

Note: the saw blade has usually a 50 um thickness. The final chip is therefore smaller than the dimensions shown above by approximately 50 um.

Bumps coordinates:



Orientation:

X is the long dimension. Y is the short dimension.

X and Y dimensions are in um.

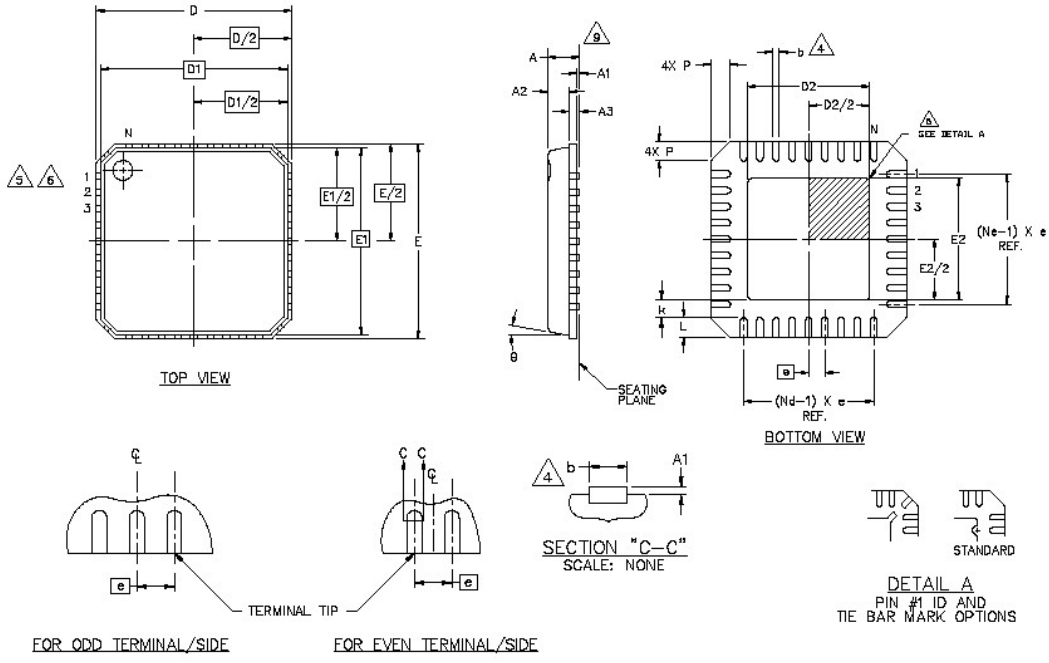
The reference (X=0, Y=0) is in the center of the die.

The largest on-chip inductor is in the positive X and positive Y quadrant.

Note: PCB pattern needs to be flipped.

vssh_p	X=	1093.5	Y=	840.0
vssa_p	X=	432.0	Y=	841.0
vdda_p	X=	232.0	Y=	840.0
rbias_p	X=	32.0	Y=	840.0
amx0_p	X=	-168.0	Y=	840.0
amx1_p	X=	-368.0	Y=	840.0
amx2_p	X=	-568.0	Y=	840.0
amx3_p	X=	-768.0	Y=	840.0
vddtest_p	X=	-1008.0	Y=	840.0
xtal1_p	X=	-1453.5	Y=	560.0
xtal2_p	X=	-1453.5	Y=	360.0
digital_test_p	X=	-1453.615	Y=	150.0
reset_b_p	X=	-1453.615	Y=	-30.0
txrx_stat_dtbo0_p	X=	-1453.615	Y=	-210.0
wclk_dtbi1_p	X=	-1453.615	Y=	-390.0
scantst_p	X=	-1453.615	Y=	-570.0
ssi_clk_p	X=	-1107.5	Y=	-840.115
ssi_data_p	X=	-927.5	Y=	-840.115
spi_clk_p	X=	-747.5	Y=	-840.115
spi_data_in_p	X=	-567.5	Y=	-840.115
spi_data_out_p	X=	-387.5	Y=	-840.115
spi_sel_b_p	X=	-207.5	Y=	-840.115
txrx_cmd_p	X=	-27.8	Y=	-840.115
surf_irq_dtbo1_p	X=	152.2	Y=	-840.115
vddd_p	X=	332.2	Y=	-840.115
vssd_p	X=	512.2	Y=	-841.46
test_dtbo0_p	X=	692.2	Y=	-840.115
test_dtbo1_p	X=	872.2	Y=	-840.115
clksel_p	X=	1052.2	Y=	-840.115
life_test_dtbi0_p	X=	1453.615	Y=	-480.0
vssa2_p	X=	1454.5	Y=	-270.0
ant2_p	X=	1453.5	Y=	-30.0
ant3_p	X=	1453.5	Y=	170.0
ant1_p	X=	1453.5	Y=	370.0
ant4_p	X=	1453.5	Y=	570.0

6.2.2 QFN-40 (for evaluation only)



COMMON DIMENSIONS						
PKG	36L 6x6			40L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	0.80	0.00	0.65	0.80
A3	0.20 REF			0.20 REF		
b	0.18	0.23	0.30	0.18	0.23	0.30
D	5.90	6.00	6.10	5.90	6.00	6.10
D1	5.75 BSC			5.75 BSC		
E	5.90	6.00	6.10	5.90	6.00	6.10
E1	5.75 BSC			5.75 BSC		
e	0.50 BSC			0.50 BSC		
k	0.25	-	-	0.25	-	-
L	0.50	0.60	0.75	0.30	0.40	0.50
N	36			40		
Nd	6			10		
Ne	6			10		
P	0.24	0.42	0.60	0.24	0.42	0.60
θ	10°	11°	12°	10°	11°	12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G3666-1	3.55	3.70	3.85	3.55	3.70	3.85
G4066-1	3.95	4.10	4.25	3.95	4.10	4.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).
12. LEADS TO BE COPLANAR 0.08 mm

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