

## NMOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

### DESCRIPTION

The Fujitsu MB8118 is a fully decoded dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8118 to be housed in a standard 16-pin DIP. Pin outs conform to the JEDEC approved pin out.

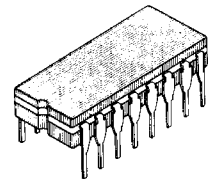
### FEATURES

- 16,384 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Address access time:
  - 100 ns max (MB8118-10)
  - 120 ns max (MB8118-12)
- Cycle time:
  - 235 ns min (MB8118-10)
  - 270 ns min (MB8118-12)
- Low power:
  - 182mW max (MB8118-10)
  - 160mW max (MB8118-12)
  - 16.5mW max (Standby)
- +5V single power supply, ±10% tolerance
- On chip substrate bias generator

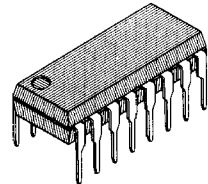
The MB8118 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs are TTL compatible; the output is three-state TTL.

- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- Hidden refresh capability
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write,  $\overline{\text{RAS}}$ -only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- Pin compatible with Intel 2118 and MCM4517

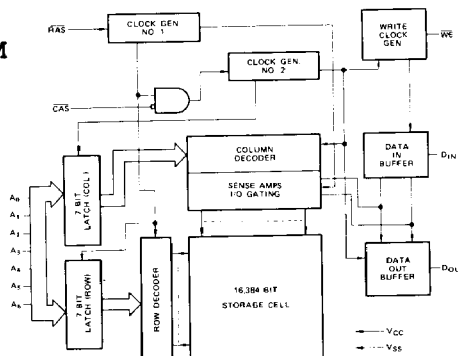


CERAMIC PACKAGE  
DIP-16C-C03

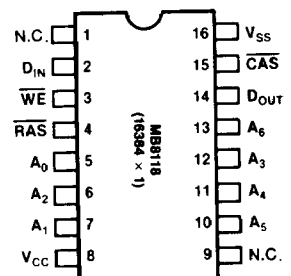


PLASTIC PACKAGE  
DIP-16P-M01

### MB8118 BLOCK DIAGRAM



### PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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**MB8118-10/MB8118-12**

**ABSOLUTE MAXIMUM RATINGS** (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7	V
Voltage on V <sub>CC</sub> pin relative to V <sub>SS</sub>	V <sub>CC</sub>	-1 to +7	V
Storage temperature	T <sub>STG</sub>	Ceramic	-55 to +150
		Plastic	-55 to +125
Power dissipation	P <sub>D</sub>	1.0	W
Short circuit output current	—	50	mA

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

(Referenced to V<sub>SS</sub>)

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	0°C to +70°C
	V <sub>SS</sub>	0	0	0	V	
Input High Voltage, all inputs	V <sub>IH</sub>	2.4	—	6.5	V	
Input Low Voltage, all inputs	V <sub>IL</sub>	-1.0	—	0.8	V	

**CAPACITANCE** (T<sub>A</sub> = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A <sub>0</sub> ~ A <sub>6</sub> , D <sub>IN</sub>	C <sub>IN1</sub>	—	—	5	pF
Input Capacitance R <sub>AS</sub> , C <sub>AS</sub> , W <sub>E</sub>	C <sub>IN2</sub>	—	—	8	pF
Output Capacitance D <sub>OUT</sub>	C <sub>OUT</sub>	—	—	7	pF

**STATIC CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10		MB8118-12		Unit
			Min	Max	Min	Max	
<b>OPERATING CURRENT</b>	□						
Average Power Supply Current (R <sub>AS</sub> , C <sub>AS</sub> cycling; t <sub>RC</sub> = Min)		I <sub>CC1</sub>	—	33	—	29	mA
<b>STANDBY CURRENT</b>							
Average Power Supply Current (R <sub>AS</sub> = C <sub>AS</sub> = V <sub>IH</sub> , D <sub>OUT</sub> = High Impedance)		I <sub>CC2</sub>	—	3.0	—	3.0	mA
<b>REFRESH CURRENT</b>	□						
Average Power Supply Current (R <sub>AS</sub> cycling, C <sub>AS</sub> = V <sub>IH</sub> ; t <sub>RC</sub> = Min)		I <sub>CC3</sub>	—	25	—	22	mA
<b>PAGE MODE CURRENT</b>	□						
Average Power Supply Current (R <sub>AS</sub> = V <sub>IL</sub> , C <sub>AS</sub> cycling; t <sub>PC</sub> = Min)		I <sub>CC4</sub>	—	25	—	22	mA
<b>INPUT LEAKAGE CURRENT</b>							
Input Leakage Current, any input (0V ≤ V <sub>IN</sub> ≤ 5.5V) (Input pins not under test = 0V, 4.5V ≤ V <sub>CC</sub> ≤ 5.5V, V <sub>SS</sub> = 0V)		I <sub>IL</sub>	-10	10	-10	10	μA
<b>OUTPUT LEAKAGE CURRENT</b> (Data out is disabled, 0V ≤ V <sub>OUT</sub> ≤ 5.5V)		I <sub>OL</sub>	-10	10	-10	10	μA
<b>OUTPUT LEVEL</b>							
Output Low Voltage (I <sub>OL</sub> = 4.2 mA)		V <sub>OL</sub>	—	0.4	—	0.4	V
<b>OUTPUT LEVEL</b>							
Output High Voltage (I <sub>OH</sub> = -5 mA)		V <sub>OH</sub>	2.4	—	2.4	—	V

Note: □ I<sub>CC</sub> is dependent on output loading. Specified values are obtained with the output open.

**DYNAMIC CHARACTERISTICS** NOTES 1,2,3  
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10			MB8118-12			Unit
			Min	Typ	Max	Min	Typ	Max	
Time Between Refresh		t <sub>REF</sub>	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t <sub>RC</sub>	235	—	—	270	—	—	ns
Read-Write Cycle Time		t <sub>RWC</sub>	285	—	—	320	—	—	ns
Page Mode Cycle Time		t <sub>PC</sub>	125	—	—	145	—	—	ns
Access Time from RAS	④ ⑤	t <sub>RAC</sub>	—	—	100	—	—	120	ns
Access Time from CAS	⑤ ⑥	t <sub>CAC</sub>	—	—	55	—	—	65	ns
Output Buffer Turn Off Delay		t <sub>OFF</sub>	0	—	45	0	—	50	ns
Transition Time		t <sub>T</sub>	3	—	50	3	—	50	ns
RAS Precharge Time		t <sub>RP</sub>	110	—	—	120	—	—	ns
RAS Pulse Width		t <sub>RAS</sub>	115	—	10000	140	—	10000	ns
RAS Hold Time		t <sub>RSH</sub>	70	—	—	85	—	—	ns
CAS Precharge Time (all cycles except page mode)		t <sub>CPN</sub>	50	—	—	55	—	—	ns
CAS Precharge Time (Page mode only)		t <sub>CP</sub>	60	—	—	70	—	—	ns
CAS Pulse Width		t <sub>CAS</sub>	55	—	10000	65	—	10000	ns
CAS Hold Time		t <sub>CSH</sub>	100	—	—	120	—	—	ns
RAS to CAS Delay Time	⑦ ⑧	t <sub>RCD</sub>	25	—	45	25	—	55	ns
CAS to RAS Precharge Time		t <sub>CRP</sub>	0	—	—	0	—	—	ns
Row Address Set Up Time		t <sub>ASR</sub>	0	—	—	0	—	—	ns
Row Address Hold Time		t <sub>RAH</sub>	15	—	—	15	—	—	ns
Column Address Set Up Time		t <sub>ASC</sub>	0	—	—	0	—	—	ns
Column Address Hold Time		t <sub>CAH</sub>	15	—	—	15	—	—	ns
Column Address Hold Time Referenced to RAS		t <sub>AR</sub>	60	—	—	70	—	—	ns
Read Command Set Up Time		t <sub>RCS</sub>	0	—	—	0	—	—	ns
Read Command Hold Time		t <sub>RCH</sub>	0	—	—	0	—	—	ns
Write Command Set Up Time	⑨	t <sub>WCS</sub>	0	—	—	0	—	—	ns
Write Command Hold Time		t <sub>WCH</sub>	30	—	—	35	—	—	ns
Write Command Hold Time Referenced to RAS		t <sub>WCR</sub>	75	—	—	90	—	—	ns
Write Command Pulse Width		t <sub>WP</sub>	30	—	—	35	—	—	ns
Write Command to RAS Lead Time		t <sub>RWL</sub>	60	—	—	65	—	—	ns
Write Command to CAS Lead Time		t <sub>CWL</sub>	45	—	—	50	—	—	ns
Data In Set Up Time		t <sub>DS</sub>	0	—	—	0	—	—	ns
Data In Hold Time		t <sub>DH</sub>	30	—	—	35	—	—	ns
Data In Hold Time Referenced to RAS		t <sub>DHR</sub>	75	—	—	90	—	—	ns
CAS to WE Delay	⑩	t <sub>CWD</sub>	55	—	—	65	—	—	ns
RAS to WE Delay	⑩	t <sub>RWD</sub>	120	—	—	120	—	—	ns
Read Command Hold Time Referenced to RAS		t <sub>RRH</sub>	20	—	—	25	—	—	ns

**Notes:**

- ① An initial pause of 200μs is required. Then several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- ② Dynamic measurements assume t<sub>T</sub> = 5ns.
- ③ V<sub>IH</sub> (min) and V<sub>IL</sub> (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
- ④ Assumes that t<sub>RCD</sub> < t<sub>RCD</sub> (max). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds the value shown.
- ⑤ Assumes that t<sub>RCD</sub> > t<sub>RCD</sub> (max).
- ⑥ Measured with a load equivalent to 2 TTL loads and 100pF.

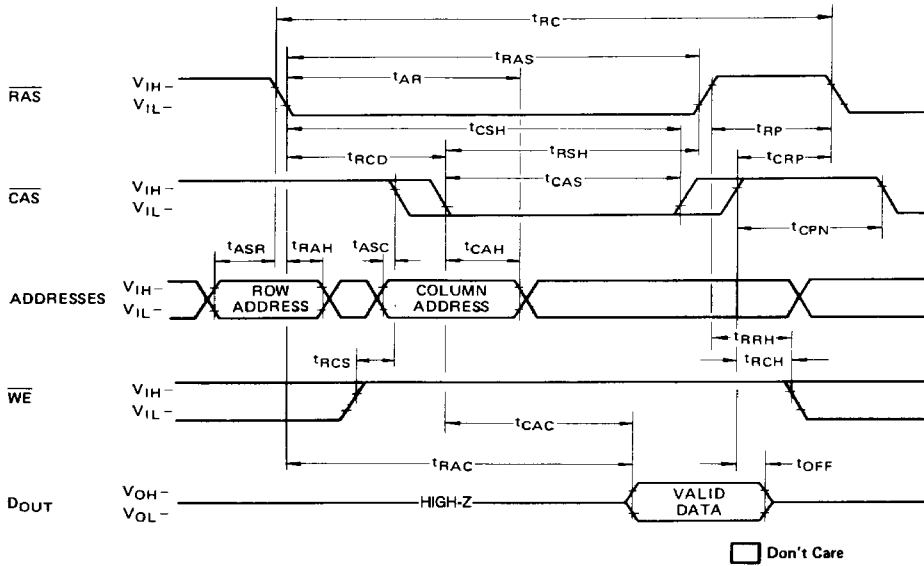
⑦ Operation within the t<sub>RCD</sub> (max) limit insures that t<sub>RCD</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.

⑧ t<sub>RCD</sub> (min) = t<sub>RAH</sub> (min) + 2t<sub>T</sub> (t<sub>T</sub> = 5ns) + t<sub>ASC</sub> (min).

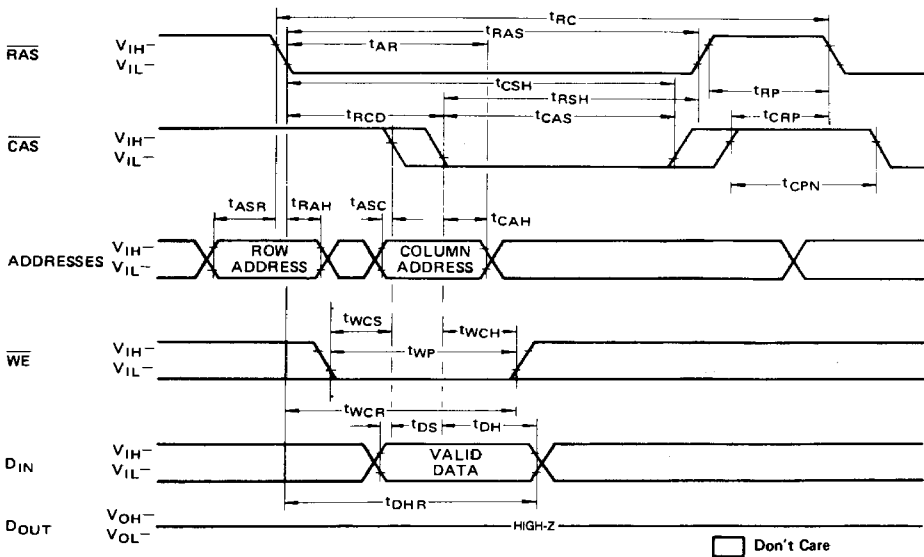
⑨ t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t<sub>WCS</sub> > t<sub>WCS</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If t<sub>CWD</sub> > t<sub>CWD</sub> (min) and t<sub>RWD</sub> > t<sub>RWD</sub> (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

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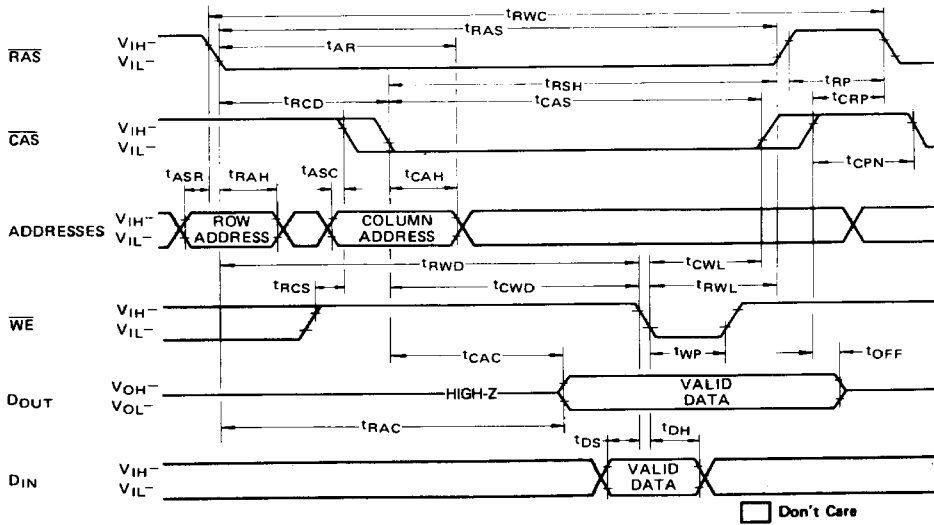
READ CYCLE TIMING DIAGRAM



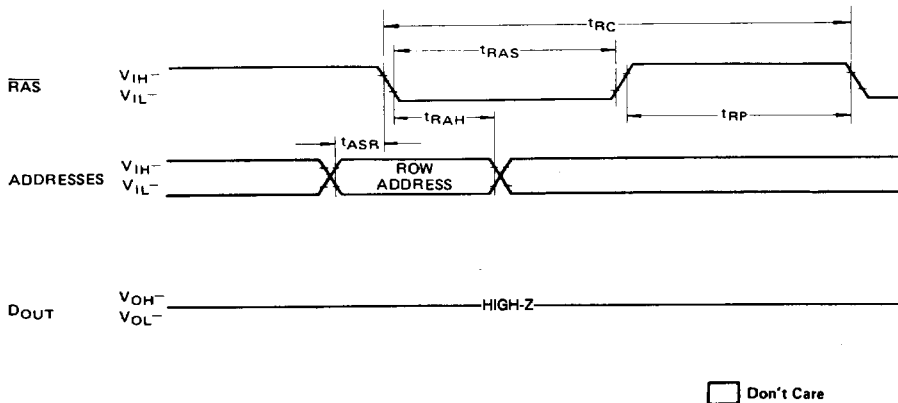
WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE

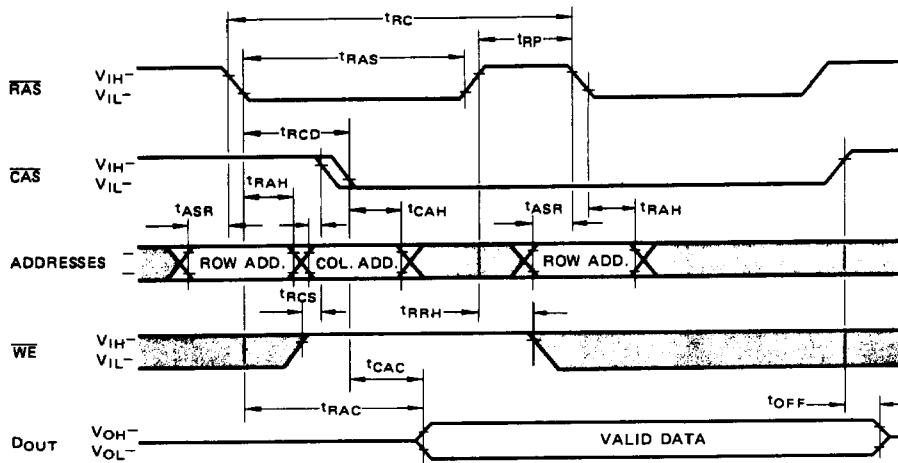


"RAS-ONLY" REFRESH CYCLE  
NOTE:  $\overline{CAS} = V_{IH}$ , WE = Don't care





HIDDEN RAS-ONLY REFRESH CYCLE TIMING DIAGRAM



Don't Care

**DESCRIPTION**

**Address Inputs**

A total of fourteen binary input address bits are required to decode any one of 16,384 storage cell locations within the MB8118. Seven row-address bits are established on the input pins (A<sub>0</sub> through A<sub>6</sub>) and latched with the Row Address Strobe (RAS). Seven column-address bits are established on the input pins and latched with the Column Address Strobe (CAS). All input addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (t<sub>RAH</sub>) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

**Write Enable**

The read mode or write mode is selected with the WE input. A logic "high" on WE dictates read mode; logic "low" dictates write mode. Data input is disabled when read mode is selected. WE can be driven by standard TTL circuits without a pull-up resistor.

**Data Input:**

Data is written into the MB8118 during a write or read-write cycle. The last falling edge of

WE or CAS is a strobe for the Data In (D<sub>IN</sub>) register. In a write cycle, if WE is brought low (write mode) before CAS, D<sub>IN</sub> is strobed by CAS, and the set-up and hold times are referenced to CAS. In a read-write cycle, WE will be delayed until CAS has made its negative transition. Thus D<sub>IN</sub> is strobed by WE, and set-up and hold times are referenced to WE.

**Data Output**

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until CAS is brought low. In a read cycle, or a read-write cycle, the output is valid after t<sub>RAC</sub> from transition of RAS when t<sub>RCD</sub> (max) is satisfied, or after t<sub>CAC</sub> from transition of CAS when the transition occurs after t<sub>RCD</sub> (max). Data remains valid until CAS is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

**Page-Mode**

Page-mode operation permits latching the row-address into the MB8118 and maintaining RAS at a logic "low" throughout all successive memory operations in which the

row-address doesn't change. This saves the power required by a RAS cycle. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

**RAS-Only Refresh**

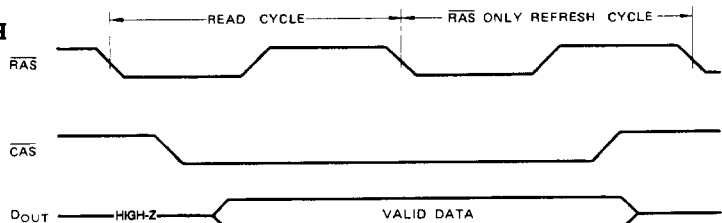
Refresh of the dynamic memory is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. RAS-only refresh prevents any output during refresh because the output buffer is in the high impedance state since CAS is at V<sub>IH</sub>. Strobing each of the 128 row-addresses with RAS will cause all bits in the memory to be refreshed. RAS-only refresh results in a substantial reduction in power dissipation.

**Hidden Refresh**

RAS-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

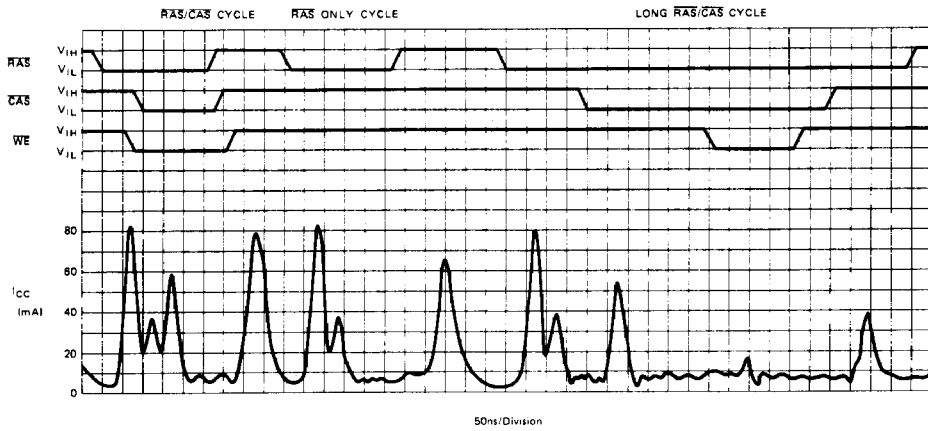
Hidden Refresh is performed by holding CAS at V<sub>IL</sub> from a previous memory read cycle. (See Figure 1 below)

**FIG. 1-HIDDEN REFRESH**

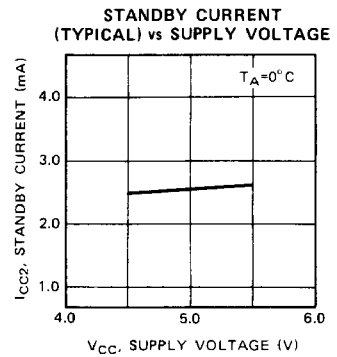
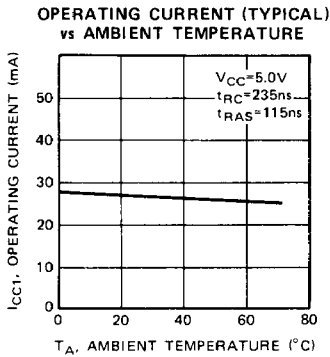
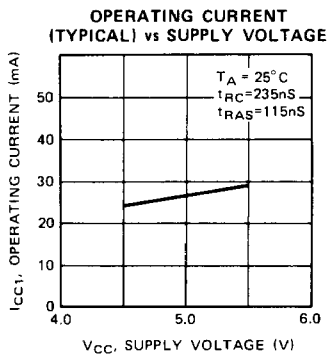
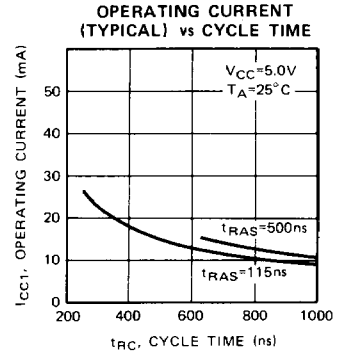
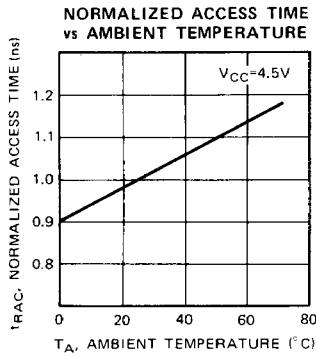
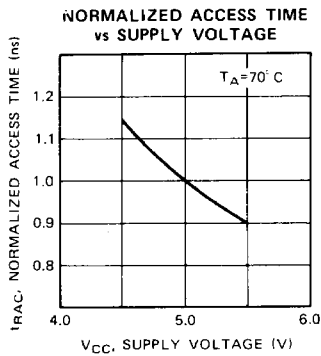


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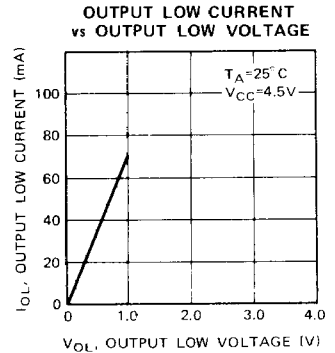
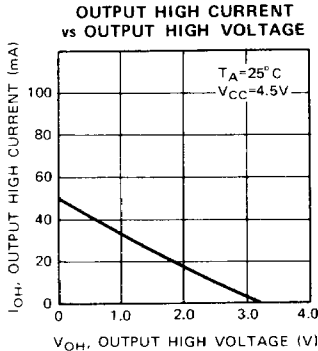
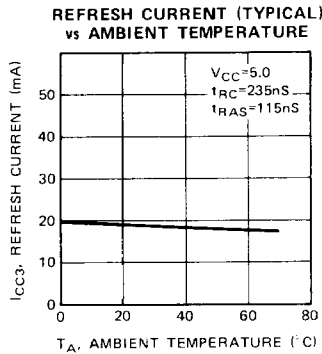
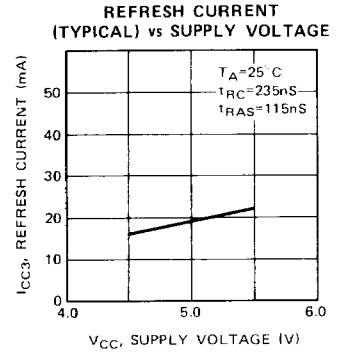
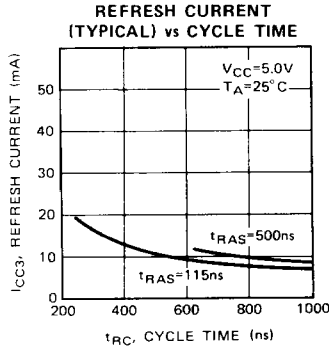
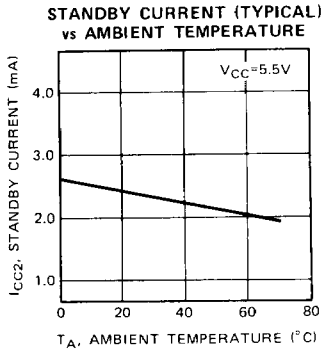
FIG. 2 — CURRENT WAVEFORMS ( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )



TYPICAL CHARACTERISTICS CURVES

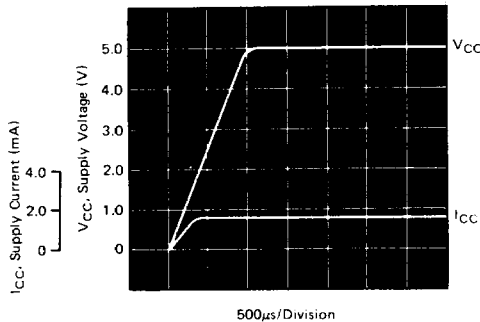


TYPICAL CHARACTERISTICS CURVES (continued)

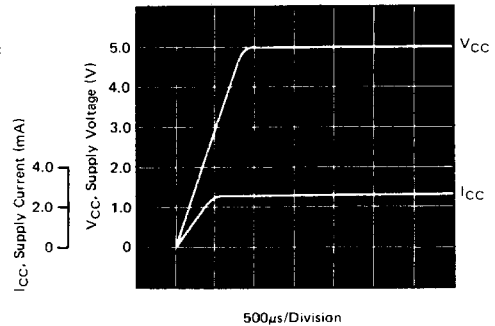


TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP

1)  $\overline{RAS}=V_{CC}, \overline{CAS}=V_{CC}$

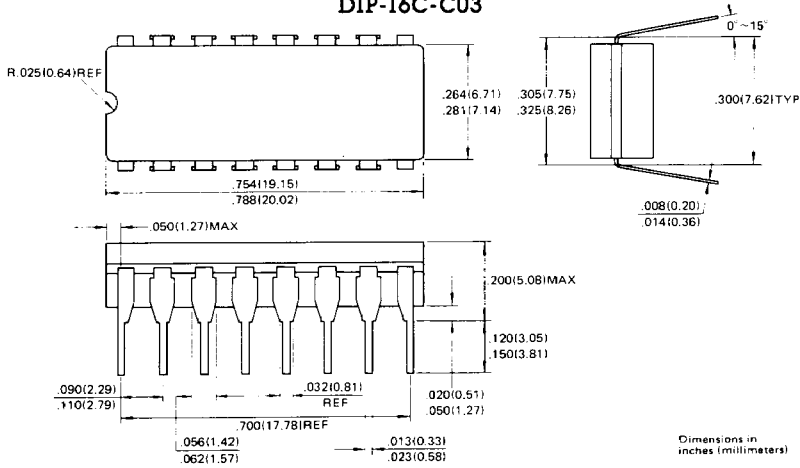


2)  $\overline{RAS}=V_{SS}, \overline{CAS}=V_{SS}$



**PACKAGE DIMENSIONS** Dimensions in inches (millimeters)

**16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE  
DIP-16C-C03**



**16-LEAD PLASTIC DUAL IN-LINE PACKAGE  
DIP-16P-M01**

