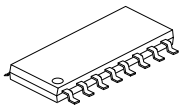
U74HC4040

CMOS IC

12-BIT ASYNCHRONOUS BINARY COUNTERS



SOP-16

■ DESCRIPTION

The **U74HC4040** devices are 12-stage asynchronous binary counters, with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low.

The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

■ FEATURES

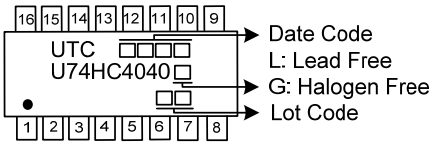
* Wide Operating Voltage Range of 2V to 6V
* Low Power Consumption, 8μA Maximum ICC
* Typical t_{PD} = 12 ns
* ±4mA Output Drive at 5V

■ ORDERING INFORMATION

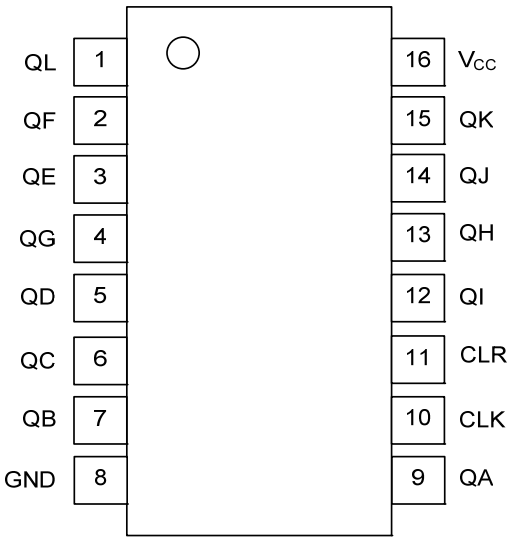
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC4040L-S16-R	U74HC4040G-S16-R	SOP-16	Tape Reel

U74HC4040G-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

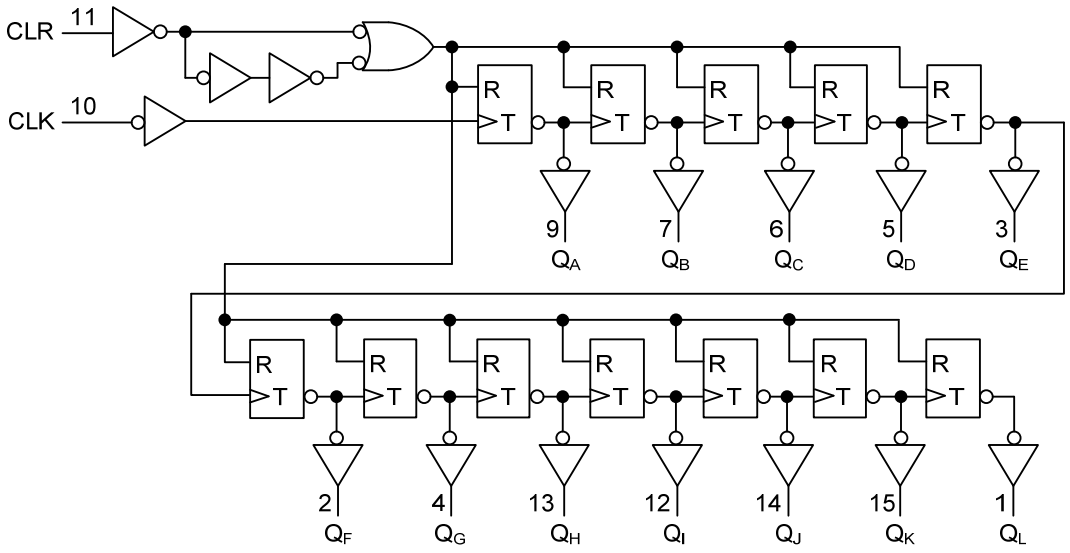


■ FUNCTION TABLE

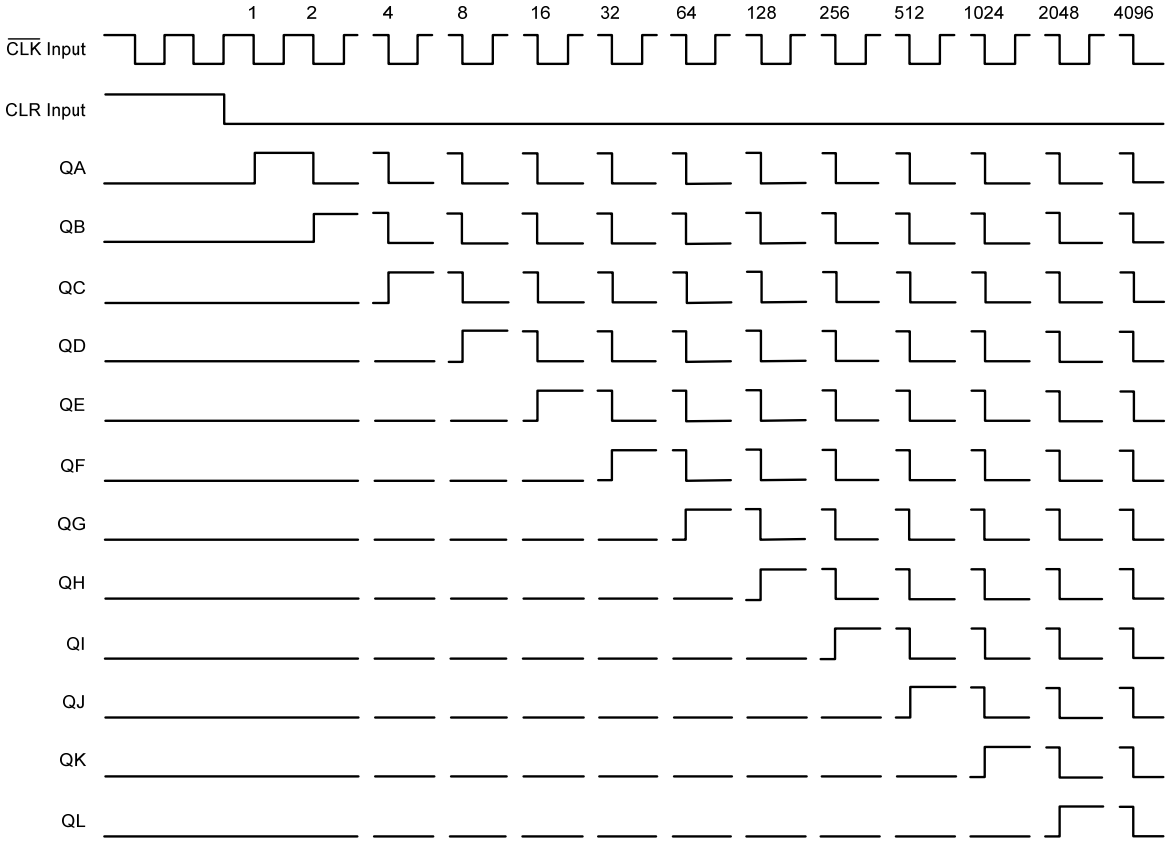
INPUTS		FUNCTION
CLK	CLR	Q0 to Q11
↑	L	No Change
↓	L	Advance to next stage
X	H	All Outputs L

Note: H = HIGH voltage level, L = LOW voltage level, X = don't care
↑ = LOW-to-HIGH clock transition, ↓ = HIGH-to-LOW clock transition.

■ LOGIC DIAGRAM (positive logic)



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Note 2)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ V_{CC}+0.5	V
Output Voltage	V_{OUT}	Active Mode	-0.5 ~ V_{CC}+0.5	V
Continuous V_{CC} or GND Current	I_{CC}		±50	mA
Continuous Output Current	I_{OUT}	V_{OUT}=0V ~ V_{CC}	±25	mA
Input Clamp Current	I_{IK}	V_{IN}<0V or V_{IN}>V_{CC}	±20	mA
Output Clamp Current	I_{OK}	V_{OUT}>V_{CC} or V_{OUT}<0V	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	5.0	6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+85	°C
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=2.0V			1000	ns
		V_{CC}=4.5V			500	ns
		V_{CC}=6.0V			400	ns

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=2.0V		1.5			V
		V_{CC}=4.5V		3.15			V
		V_{CC}=6.0V		4.2			V
Low-level Input Voltage	V_{IL}	V_{CC}=2.0V				0.5	V
		V_{CC}=4.5V				1.35	V
		V_{CC}=6.0V				1.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=2.0V	V_{IN}=V_{IH} or V_{IL} I_{OH}=-20μA	1.9	1.998		V
		V_{CC}=4.5V		4.4	4.499		V
		V_{CC}=6.0V		5.9	5.999		V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL} I_{OH}=-4mA		3.98	4.3		V
		V_{CC}=6.0V, V_{IN}=V_{IH} or V_{IL} I_{OH}=-5.2mA		5.48	5.8		V
Low-Level Output Voltage	V_{OL}	V_{CC}=2.0V	V_{IN}=V_{IH} or V_{IL} I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V			0.001	0.1	V
		V_{CC}=6.0V			0.001	0.1	V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=4mA			0.17	0.26	V
		V_{CC}=6.0V, V_{IN}=V_{IH} or V_{IL} I_{OL}=5.2mA			0.15	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6.0V, V_{IN}= V_{CC} or GND			±0.01	±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6.0V, V_{IN}=V_{CC} or GND, I_{OUT}=0A				8	μA
Input Capacitance	C_I	V_{CC}=2.0~6.0V, V_{IN}=V_{CC} or GND			3	10	pF

■ SWITCHING CHARACTERISTICS (C_L=50pF, T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency	f_{MAX}	V_{CC}=2.0V	5.5	10		MHz
		V_{CC}=4.5V	28	45		MHz
		V_{CC}=6.0V	33	53		MHz
Propagation Delay From Input (CLK) to Output (QA)	t_{PD}	V_{CC}=2.0V		62	150	ns
		V_{CC}=4.5V		16	30	ns
		V_{CC}=6.0V		12	26	ns
Propagation Delay From Input (CLR) to Output (Any)	t_{PHL}	V_{CC}=2.0V		63	140	ns
		V_{CC}=4.5V		17	28	ns
		V_{CC}=6.0V		13	24	ns
Propagation Delay to Output (Any)	t_t	V_{CC}=2.0V		28	75	ns
		V_{CC}=4.5V		8	15	ns
		V_{CC}=6.0V		6	13	ns

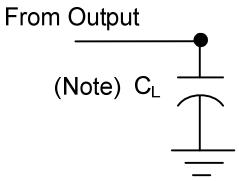
■ TIMING REQUIREMENTS (Input: t_R, t_F≤6ns; PRR≤1MHz)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency		f_{CLOCK}	V_{CC}= 2V			5.5	MHZ
			V_{CC}=4.5V			28	MHZ
			V_{CC}=6V			33	MHZ
Pulse Duration	CLK High or Low	t_W	V_{CC}= 2V	90			ns
			V_{CC}=4.5V	18			ns
			V_{CC}=6V	15			ns
Pulse Duration	$\overline{CLR}$ Low	t_W	V_{CC}= 2V	70			ns
			V_{CC}=4.5V	14			ns
			V_{CC}=6V	12			ns
Setup Time Before CLK↓		t_{SU}	V_{CC}= 2V	60			ns
			V_{CC}=4.5V	12			ns
			V_{CC}=6V	10			ns

■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

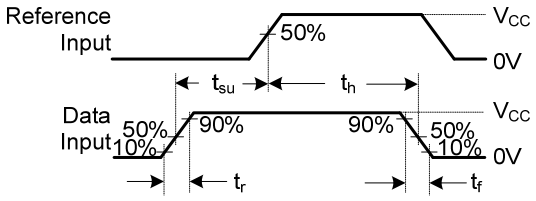
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No Load.		88		pF

■ TEST CIRCUIT AND WAVEFORMS

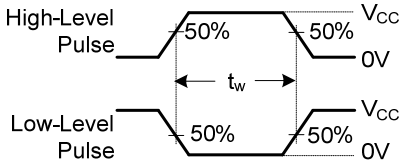


Note: C_L includes probe and jig capacitance. C_L=50pF, R_L=1KΩ.

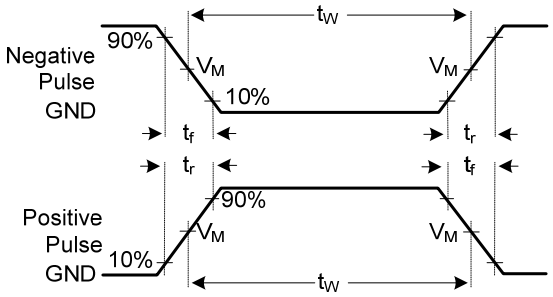
INPUT		LOAD	TEST
V_{IN}	t_r, t_f	C_L	
V_{CC}	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}



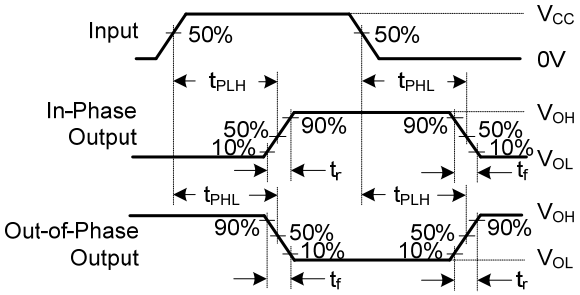
Voltage Waveforms Setup And
Hold And Input Rise And Fall Times



Voltage Waveforms Pulse Durations



Test Circuit for Measuring Switching Times



Voltage Waveforms
Propagation Delay And Output Transition Times

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O = 50Ω.