# HD66135T

## 120-Channel High-Voltage Common Driver for a Dot-Matrix STN Liquid Crystal Display

HITACHI

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### Description

The HD66135T is a 120-channel common driver for driving a dot-matrix STN liquid crystal display (LCD) panel. Since the driver uses a high-voltage (75 V) process, the operating voltage from -37.5 to +37.5 V is enabled with level VM in the center. It operates at a low logic drive voltage of 3 V. This driver is used together with segment driver HD66134ST, which is built into the shadowing correction circuit.

### Features

- Duty cycle: Up to 1/300
- LCD drive voltage: 75 V
- Number of LCD drive circuits: 120 circuits
- Operating voltage: 2.7 to 5.5 V
- Output division function (60 × 2 outputs)
- Display-off function
- Slim tape-carrier package (TCP)
  - Output lead pitch: 190 µm
  - User area: 10.5 mm
- Low output impedance: 0.5 kΩ (typ)
- Intermediate voltage I/F

## Pin Arrangement

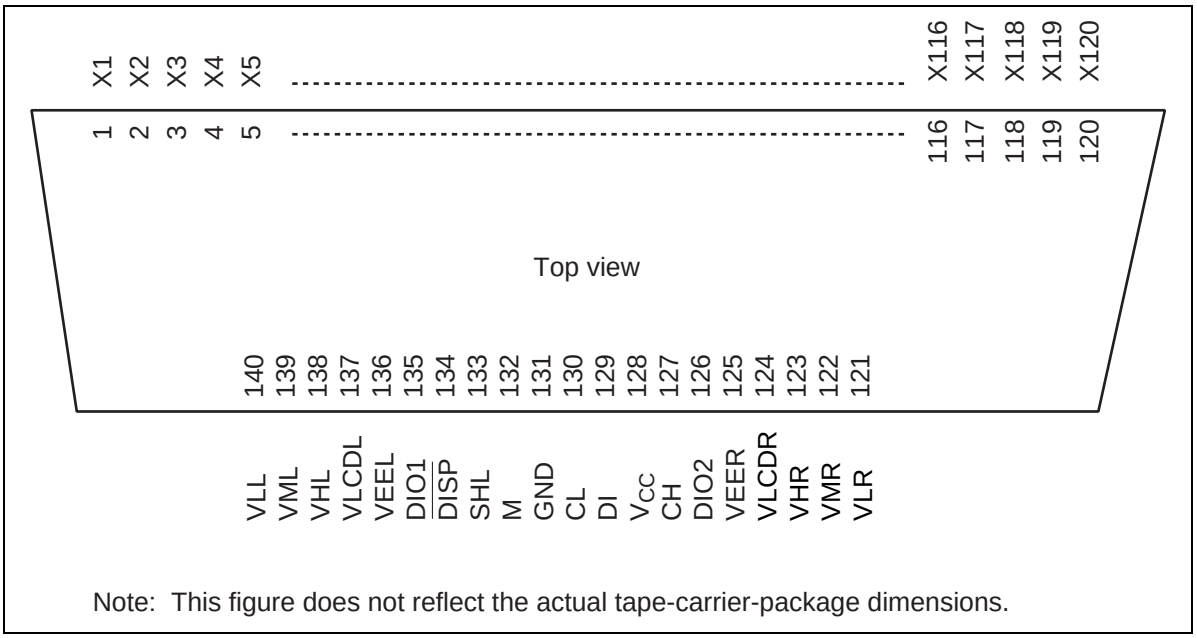


**Figure 1 Pin Arrangement**

## Block Diagram

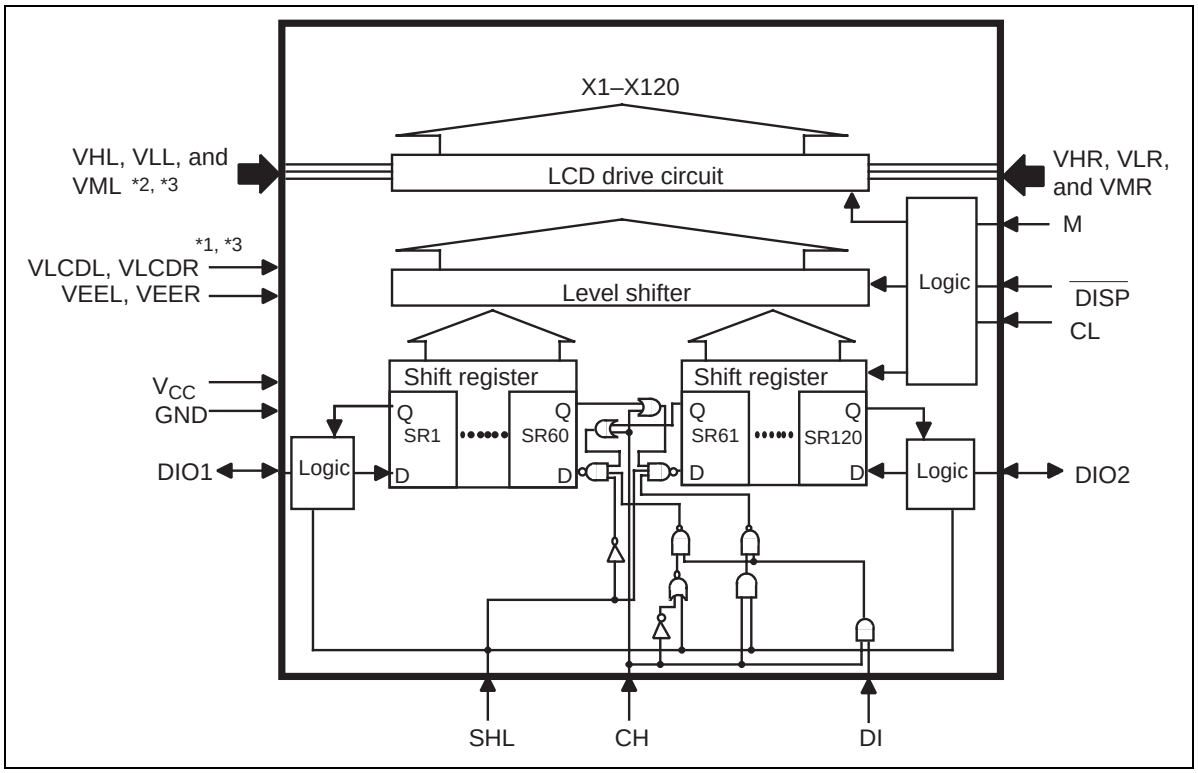


**Figure 2 Block Diagram**

Notes: 1. VLCDL and VEEL are internally connected to VLCDR and VEER, respectively.
2. VHL, VLL, and VML are internally connected to VHR, VLR, and VMR, respectively.
3. VLCDL and VLCDR are internally connected to VHL and VHR, respectively, and VEEL and VEER are internally connected to VLL and VLR, respectively.

## Block Functions

### LCD Drive Circuit

The 120-bit LCD drive circuit generates three voltage levels VH, VL, and VM, which drive the LCD panel. One of these three levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

### Level Shifter

The level shifter changes the logic control signals (5 V) into high-voltage signals for the LCD drive circuit.

### Shift Register

The 120-bit shift register shifts the data input via the DIO pin with shift clock CL. The SHL pin selects the data-shift direction.

## Pin Functions

**Table 1 Pin Functions**

| Classification | Symbol | Pin No. | Pin Name | Input/ Output | Function |
|---|---|---|---|---|---|
| Power supply | VLCDL<br>VLCDR<br>VEEL<br>VEER<br>$V_{cc}$<br>GND | 137<br>124<br>136<br>125<br>128<br>131 | VLCDL<br>VLCDR<br>VEEL<br>VEER<br>VCC<br>GND | — | VLCDL, VLCDR–VEEL, VEER: LCD drive power supply<br>VCC–GND: Logic power supply |
| | VHL<br>VHR<br>VLL<br>VLR<br>VML<br>VMR | 138<br>123<br>140<br>121<br>139<br>122 | VHL<br>VHR<br>VLL<br>VLR<br>VML<br>VMR | Input | LCD drive voltage level<br>VHL, VHR: Selection level (equivalent to VLCDL and VLCDR levels)<br>VLL, VLR: Selection level (equivalent to VEEL and VEER levels)<br>VML, VMR: Non-selection level |
| Control signal | CL | 130 | Clock | Input | Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts the data input. |
| | M | 132 | M | Input | Changes the LCD drive outputs to AC. |
| | CH | 127 | CH | Input | Selects the data-shift mode. (CH = low: 120-output mode, CH = high: 60 × 2-output mode) |
| | SHL | 133 | Shift left | Input | Selects the data-shift direction as shown in Table 2. |
| | DIO1 | 135 | Data | Input/ output | Serial input/output (shift-register-data input/output). This pin is used for serial input when SHL is high, and for serial output when SHL is low. |
| | DIO2 | 126 | Data | Input/ output | Serial input/output (shift-register-data input/output). This pin is used for serial input when SHL is low, and for serial output when SHL is high. |
| | DI | 129 | Data | Input | Serial input (shift-register-data input). In the 60 × 2-output mode, shift register data is input to pins X61 to X120 in serial when SHL is high, and to pins X1 to X60 in serial when SHL is low. This pin must be connected to GND when not used. |
| | $\overline{DISP}$ | 134 | Disp off | Input | Pins X1 to X120 are set at level VM by connecting this pin to GND. Registers are not cleared. |
| LCD drive output | X1 to X120 | 1 to 120 | X1 to X120 | Output | One of three levels VH, VL, and VM is output according to the combination of the M signal and display data when the $\overline{DISP}$ pin is connected to $V_{cc}$. See figure 3. |

**Table 2 Shift Direction of the Shift Register**

| SHL | Data-Shift Direction |
|---|---|
| High | Shift to right |
| | DIO1 → SR1 → SR2.....SR120 → DIO2 |
| Low | Shift to left |
| | DIO2 → SR120 → SR119.....SR1 → DIO1 |

Note: SR1 to SR120 correspond to the outputs of X1 to X120, respectively.

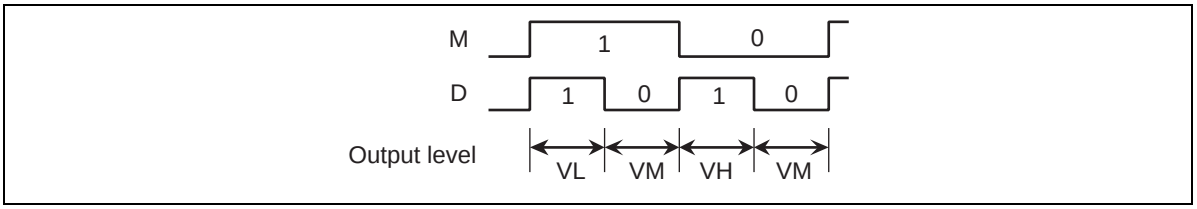


**Figure 3 Selection of the LCD Drive Output Level**

## Absolute Maximum Ratings[*1]

| Item | | Symbol | Ratings | Unit | Notes |
|---|---|---|---|---|---|
| Power supply voltage | Logic circuit | $V_{cc}$ | –0.3 to +7.0 | V | 2 and 7 |
| | LCD drive circuit | VLCD | –0.3 to +41 | V | 2 and 7 |
| | | VEE | –39 to +0.3 | V | 2 and 7 |
| Input voltage (1) | | VT1 | –0.3 to $V_{cc}$ + 0.3 | V | 2 and 3 |
| Input voltage (2) | | VH | = VLCD | V | 4 |
| Input voltage (3) | | VL | = VEE | V | 5 |
| Input voltage (4) | | VM | – 5.0 to + 10.0 | V | 6 and 7 |
| Operating temperature | | Topr | –30 to +75 | °C | |
| Storage temperature | | Tstg | –50 to +110 | °C | |

Notes: 1 If the LSI is used beyond these maximum ratings, it will be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunctions or degraded reliability.

2. The reference point is GND (0 V).
3. Applies to the CL, M, SHL, DI, $\overline{DISP}$, CH, DIO1, and DIO2 pins.
4. Applies to the VHL and VHR pins.
5. Applies to the VLL and VLR pins.
6. Applies to the VML and VMR pins.
7. Conform to the following turn-on/off sequence of the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, the LSI reliability will be affected.

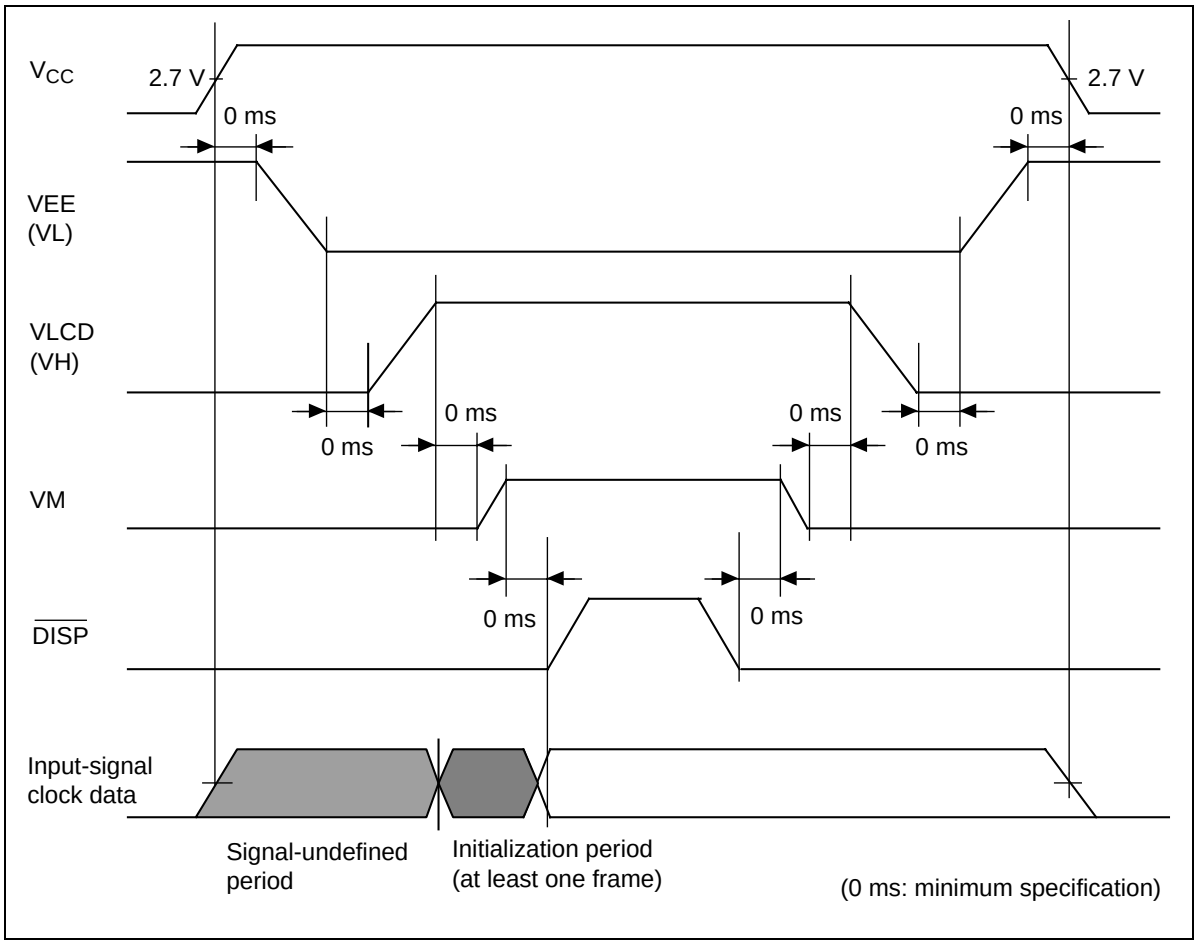


**Figure 4 Power and Signal Sequence**

7.1 Turning on the power

1)Turn on the power in the order of GND-$V_{CC}$, GND-VEE (VL), GND-VLCD (VH), and VM. Then, ground the $\overline{DISP}$ pin.

2) The LCD forcibly outputs the VM level by the DISPOFF function.

3) Even if an input signal is disturbed immediately after $V_{CC}$ is applied, the DISPOFF function has priority.

4) Input the appropriate signal to initialize the registers in the driver. The initialization period must be at least one frame.

5) The preparation for normal display is completed. Apply the $V_{CC}$ level to the $\overline{DISP}$ pin to cancel the DISPOFF function. At this time, the level of pins VEE (VL), VLCD (VH), and VM must rise to the appropriate potential.

7.2 Turning off the power

The procedure is basically the reverse of that for turning on the power.

1) Ground the $\overline{DISP}$ pin.

2) Turn off the LCD power in the order of VM, GND-VLCD (VH), and GND-VEE (VL).

3) Ground $V_{CC}$ and the input signal.

At this time, the level of pins VEE (VL), VLCD (VH), and VM must fall to 0 V. Since the DISPOFF function stops when $V_{CC}$ falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

## Electrical Characteristics

**DC Characteristics ($V_{CC}$ = 2.7 to 5.5 V, GND = 0 V, VLCD – VEE = 40 to 75 V, and Ta = –30 to +75 °C, unless otherwise stated)**

| Item | Symbol | Applicable Pins | Min. | Typ. | Max. | Unit | Conditions | Note |
|---|---|---|---|---|---|---|---|---|
| Input high-level voltage | ViH | CL, M, SHL, CH, DI, DIO1, DIO2, and $\overline{DISP}$ | 0.7 × $V_{CC}$ | — | $V_{CC}$ | V | | |
| Input low-level voltage | ViL | | 0 | — | 0.3 × $V_{CC}$ | V | | |
| Output high-level voltage | VOH | DIO1 and DIO2 | $V_{CC}$ – 0.4 | — | — | V | IOH = –0.4 mA | |
| Output low-level voltage | VOL | DIO1 and DIO2 | — | — | 0.4 | V | IOL = 0.4 mA | |
| Vi–Xj ON resistance | RON | X1 to X120, and V | — | 0.5 | 0.7 | kΩ | ION = 150 µA | 1 |
| Input leakage current (1) | IiL1 | CL, M, SHL, CH, DI, DIO1, DIO2, and $\overline{DISP}$ | –5 | — | 5 | µA | VIN = $V_{CC}$ to GND | |
| Input leakage current (2) | IiL2 | VH, VL, and VM | –25 | — | 25 | µA | | |
| Current consumption | ICC | $V_{CC}$ | — | 0.1 | 0.5 | mA | fCL = 160 kHz<br>fM = 6 kHz | 2 |
| Current consumption | ILCD | VLCD | — | 1.5 | 2.0 | mA | | |

Notes: 1. The resistance between the X pin and the V pin (one of the voltage supply pins VH, VL, and VM), when a load current is applied to one of the pins from X1 to X120; defined under the following conditions:
VLCD = VH = 36 V, VEE = VL = –30 V, VM = 3 V, and GND = 0 V.
The VH, VL, and VM voltages must be within VLCD = VH = 40.5 to 23 V, VEE = VL = –34.5 to –17 V, and 9 V > VM > –4 V.

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, ViH and ViL must be held at $V_{CC}$ and GND, respectively.

3. The voltage of each signal is shown in figure 5.

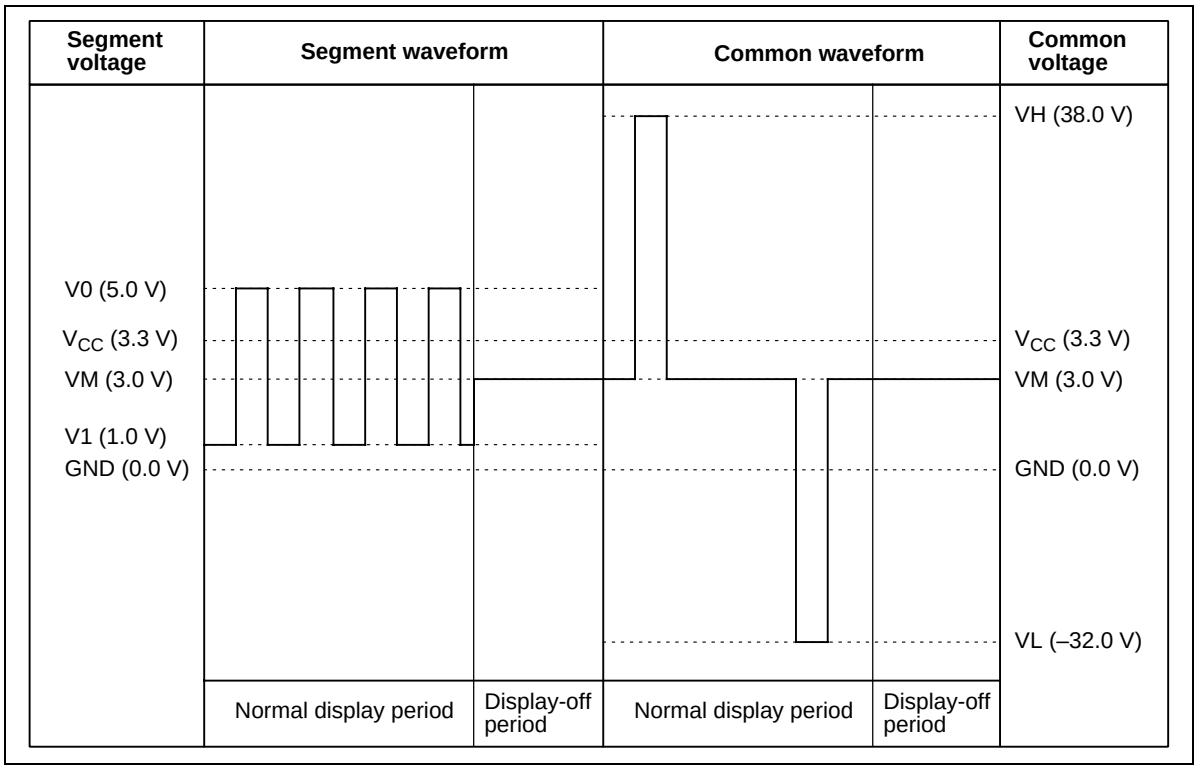


**Figure 5 Signal Voltages**

**AC Characteristics (1) ($V_{CC}$ = 2.7 to 4.5 V, GND = 0 V, VLCD – VEE = 40 to 75 V, and Ta = –30 to +75 °C)**

| Item | Symbol | Applicable Pins | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Clock cycle time | $t_{CYC}$ | CL | 400 | — | ns | |
| Clock high level width | $t_{CWH}$ | CL | 40 | — | ns | |
| Clock low level width | $t_{CWL}$ | CL | 370 | — | ns | |
| Clock rise time | tr | CL | — | 30 | ns | |
| Clock fall time | tf | CL | — | 30 | ns | |
| Data setup time | $t_{DS}$ | DI, DIO1, DIO2, and CL | 100 | — | ns | |
| Data hold time | $t_{DH}$ | DI, DIO1, DIO2, and CL | 30 | — | ns | |
| Data output delay time | $t_{DD}$ | DIO1, DIO2, and CL | — | 350 | ns | 1 |
| M setup time | $t_{MS}$ | CL and M | 20 | — | ns | |
| M hold time | $t_{MH}$ | CL and M | 20 | — | ns | |
| Output delay time (1) | $t_{pd1}$ | X (n) and CL | — | 1.2 | µs | 2 |

Notes: 1. Defined by connecting the load circuit shown in figure 6.
2. Defined by connecting the load circuit shown in figure 6.

**AC Characteristics (2) ($V_{CC}$ = 4.5 to 5.5 V, GND = 0 V, VLCD – VEE = 40 to 75 V, and Ta = –30 to +75 °C)**

| Item | Symbol | Applicable Pins | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Clock cycle time | $t_{CYC}$ | CL | 400 | — | ns | |
| Clock high level width | $t_{CWH}$ | CL | 25 | — | ns | |
| Clock low level width | $t_{CWL}$ | CL | 370 | — | ns | |
| Clock rise time | tr | CL | — | 30 | ns | |
| Clock fall time | tf | CL | — | 30 | ns | |
| Data setup time | $t_{DS}$ | DI, DIO1, DIO2, and CL | 100 | — | ns | |
| Data hold time | $t_{DH}$ | DI, DIO1, DIO2, and CL | 30 | — | ns | |
| Data output delay time | $t_{DD}$ | DIO1, DIO2, and CL | — | 150 | ns | 1 |
| M setup time | $t_{MS}$ | CL and M | 20 | — | ns | |
| M hold time | $t_{MH}$ | CL and M | 20 | — | ns | |
| Output delay time (1) | $t_{pd1}$ | X (n) and CL | — | 0.7 | µs | 2 |

Notes: 1. Defined by connecting the load circuit shown in figure 6.
2. Defined by connecting the load circuit shown in figure 6.

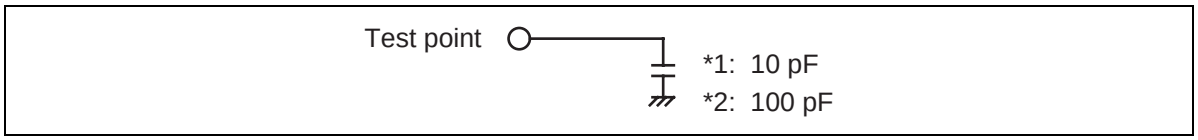


**Figure 6 Load Circuit**

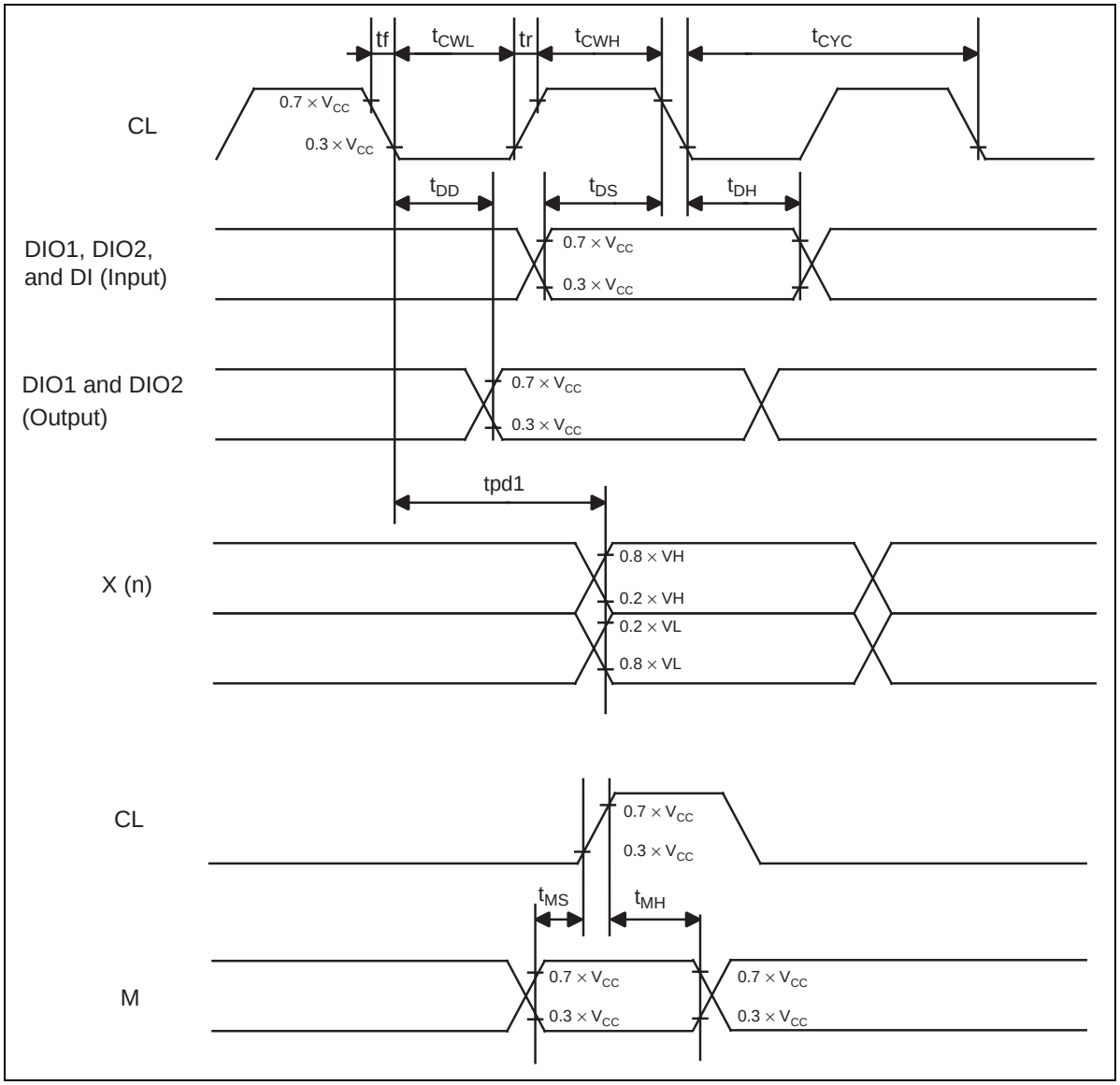


**Figure 7 AC Characteristics**