SICOFI®2-µC Two Channel Codec Filter with PCM and Microcontroller Interface

PEB 2266 Version 2.2

PEF 2266 Version 2.2

Wired Communications

Infineon technologies

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PEB 2266

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Preface

This document provides detailed programming information about the SICOFI®2-µC. It is intended for software engineers and those system designers who need detailed information on programming and configuring the device. All content applies to both the standard PEB 2266 and the extended temperature version, PEF 2266, unless specified.

Organization of this Document

This *Programmer's Reference Manua*l is organized as follows:

- Chapter 1, Overview
  Includes a general description, feature list, logic symbol, and typical applications.
- Chapter 2, Pin Descriptions
  Illustrates the Pin Configuration and provides detailed descriptions of the pins and their associated symbols and functions.
- Chapter 3, Functional Description
  Provides a detailed flow diagram, identifies the major functional blocks, and provides details on each of the programmable filter blocks.
- Chapter 4, Operational Description
  Includes a state diagram and description of the operating states of all two channels and a brief summary of transmission characteristics.
- Chapter 5, Interface Descriptions
  Discusses the Analog, PCM, Signaling, and Microcontroller Interfaces and interrupts.
- Chapter 6, Programming the SICOFI®2-µC
  Illustrates the memory structure, provides a register model and summary, and describes the command sequences and registers in detail.
- Chapter 7, Application Hints
  Indicates the support tools available for the PEB 2266 and includes a detailed discussion of the QSICOS Coefficient Calculation and Register Configuration Software.
- Chapter 8,Test Configuration
  Describes the various on-chip test features and illustrates a proposed test circuit.
- The Appendix
  Includes a glossary and an index.

Related Documentation

Additional documentation for the PEB 2266 includes a *Product Brief*, a *Product Overview*, a *Hardware Reference Manual*, and assorted *Application Notes*.

Documentation is also available for other SICOFI codec devices including the PEB 2466, PSB 2132, and PSB 2134. Documentation is available by accessing our website: http://www.infineon.com/sicofi

1 Overview

The SICOFI®2-µC is a programmable DSP-based two-channel codec filter device to fulfill worldwide voice telephony standards. An easy to use serial microcontroller interface provides access to 288 bytes of Coefficient RAM (CRAM) and to 32 registers. The values stored in the CRAM determine the filter characteristics of the embedded DSP. Writing to the registers allows control of features such as mode settings, enabling and disabling of filters, tone generators, and test loops, PCM data rates, and signaling and clock output control. Reading from the registers provides status information about the signaling inputs and level metering results.

This document provides detailed information on filter coefficient programming, register configuration settings, and the programming interface. The PEB 2266 is available for standard temperature range applications (0 °C to +70 °C); the PEF 2266 is available for extended temperature range applications (-40 °C to +85 °C).

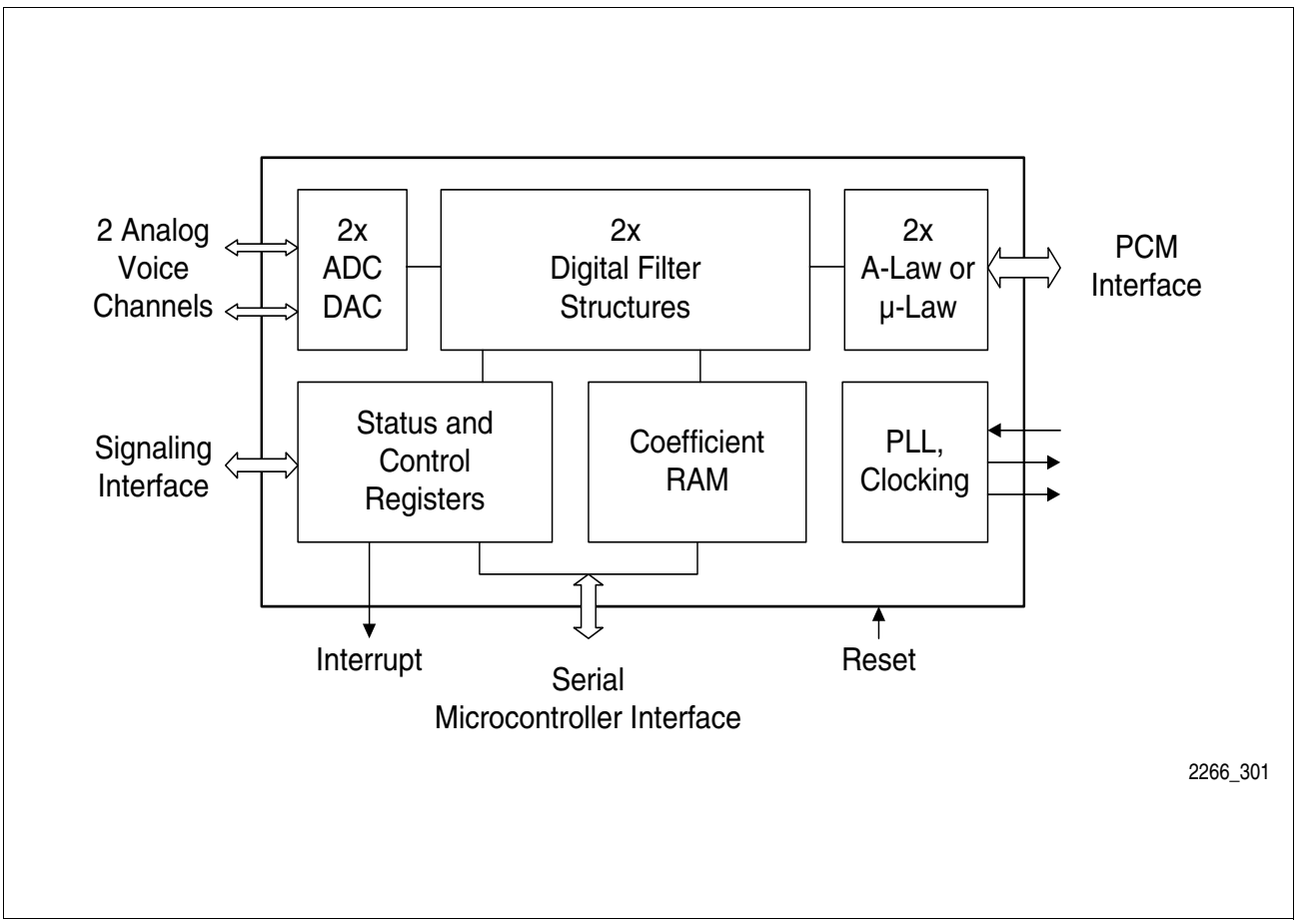


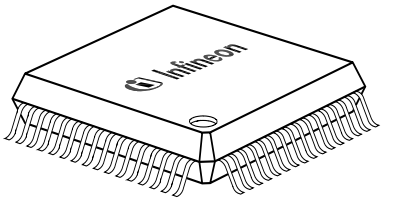
Figure 1 Programmable Two Channel Codec Filter

Two Channel Codec Filter with PCM and Microcontroller Interface SICOFI®2-µC

PEB 2266
PEF 2266

Version 2.2 **CMOS**

1.1 Features



P-MQFP-64

- Two-channel single chip codec and filter fulfills the ITU-T Q.552, G.712, and all country-specific requirements
- High analog driving capability (300 Ω, 50 pF) for direct driving of transformers
- Digital Signal Processing (DSP) technique
- Programmable digital filters to adapt transmission behavior, especially for:
  - AC impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
  - A/µ-Law compression and expansion
- High performance ADC and DAC for excellent linearity and dynamic gain
- Programmable Analog Interface to electronic SLICs or transformer solutions
- Seven SLIC-signaling I/O pins per channel with programmable debouncing
- Two PCM Highways accessible by on-chip PCM Interface
- Programmable time slot assignment and variable data rates from 128 kbit/s to 8 Mbit/s
- Easy to use 4-pin Serial Microcontroller Interface for (SPI compatible) read/write access
- Single supply voltage (5 V)
- Advanced low-power mixed-signal CMOS technology
- Two programmable tone generators per channel (DTMF possible)
- Level metering function for system tests and for analog input signal testing
- Advanced on-chip functions for device and system diagnostics and manufacturing test
  - Five digital loops
  - Four analog loops
- Support tools include:
  - Hardware development board — STUT 2466
  - QSICOS Coefficient Calculation and Register Configuration Software
- Standard P-MQFP-64 package

Type	Package
PEB 2266 Version 2.2	P-MQFP-64
PEF 2266 Version 2.2	P-MQFP-64

1.2 Logic Symbol

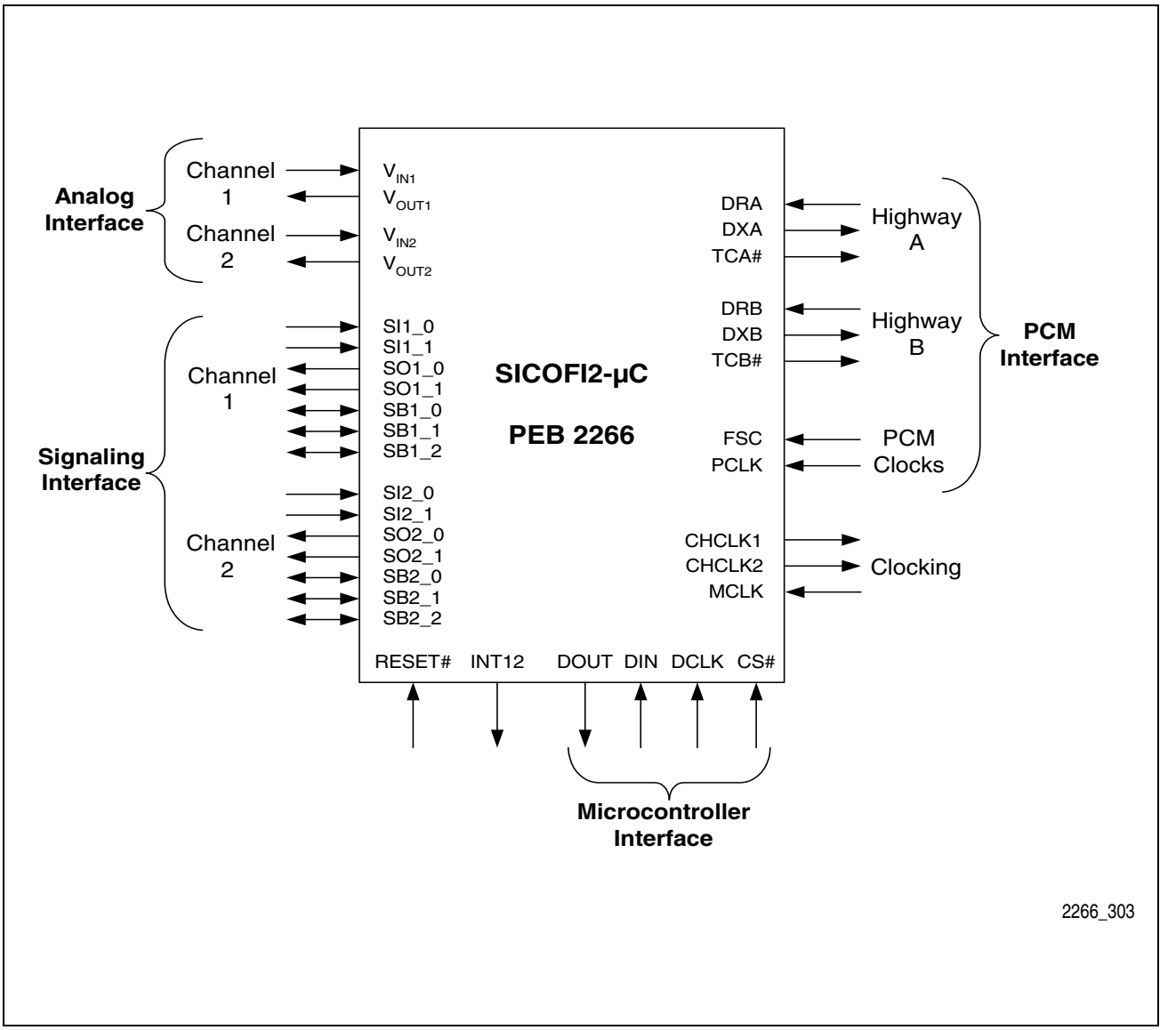


Figure 2 SICOFI®2-µC Logic Symbol

1.3 Typical Applications

Many applications will benefit from the versatility of the SICOFI®2-µC codec and filter. The inherent flexibility enables several products to be developed around one basic architecture, thus affording potentially significant savings in time to market, inventory costs, and support administration.

The following list represents some of the typical applications for which the SICOFI®2-µC codec was designed: Analog linecards for Central Offices and PBXs, Small PBX or Key Systems, Digital Loop Carrier (DLC) Systems, Digital Added Main Lines (DAML) Systems, Fiber-to-the-Curb (FTTC) Systems, Radio-in-the-Loop (RITL) Systems, and any multichannel, digital voice processing, storage, or communication applications.Refer to the ***Product Overview***, **Chapter 5 Application Hints** for more information.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

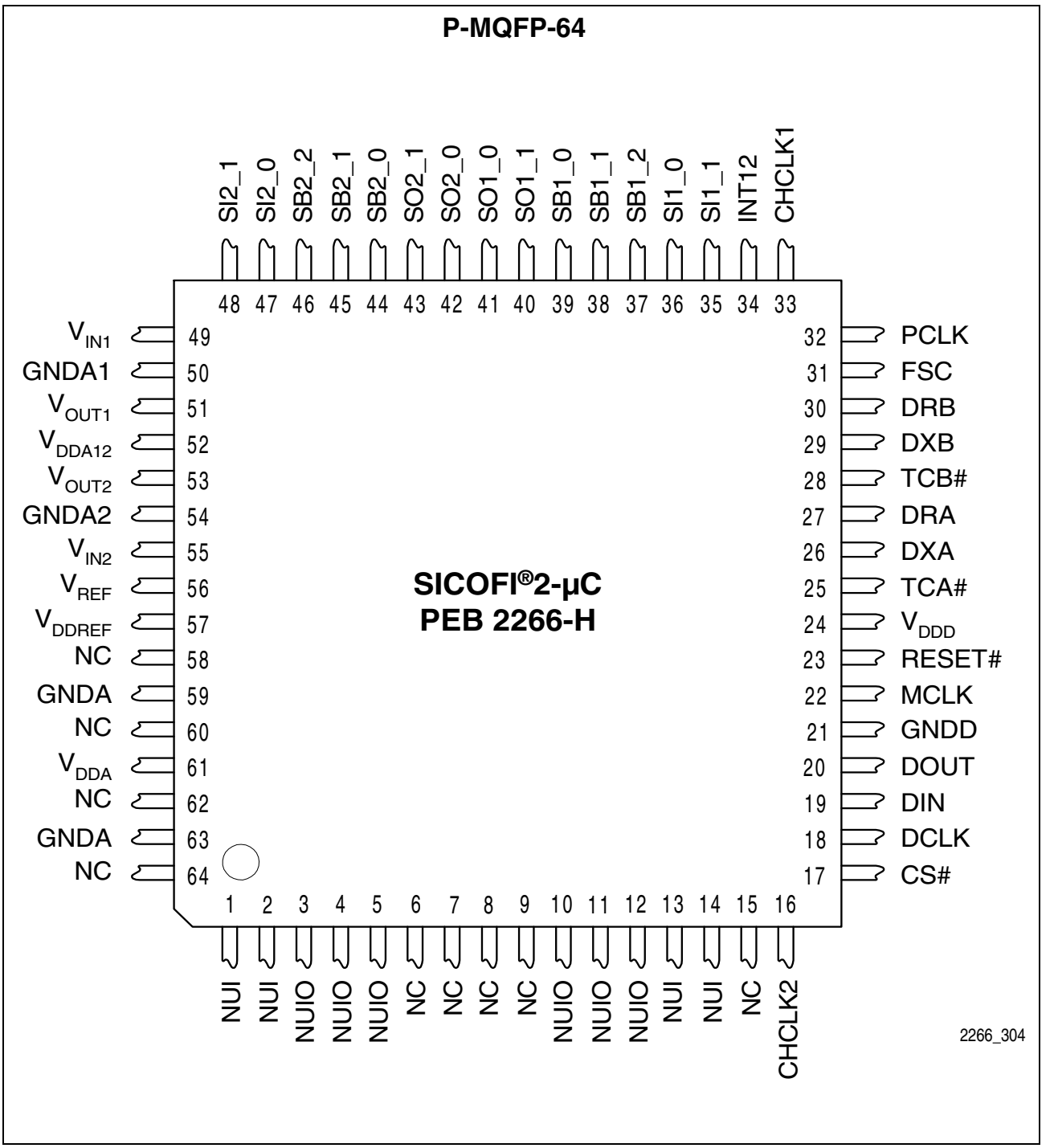


Figure 3 Pin Configuration of SICOFI®2-µC

2.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin	Symbol	Type	Function	Ch.
1, 2	NUI	I	**Non Usable Input** Pins must be tied directly to digital ground (Pin 21).	
3, 4, 5	NUIO	I/O	**Non Usable Input/Output** Pins must be tied via a pull-down resistor to digital ground (Pin 21).	
6, 7, 8, 9	NC		**Not Connected** Pins are not connected in this device.	
10, 11, 12	NUIO	I/O	**Non Usable Input/Output** Pins must be tied via a pull-down resistor to digital ground (Pin 21).	
13, 14	NUI	I	**Non Usable Input** Pins must be tied directly to digital ground (Pin 21).	
15	NC		**Not Connected** Pin is not connected in this device.	
16	CHCLK2	O	**Chopper Clock Output 2** Provides 256, 512, or 16,384 kHz signal; sync. to MCLK. Configured with Register Bits XR5.2 and XR5.3.	both
17	CS#	I	**Chip Select** Microcontroller Interface chip select, enable to read or write; active low.	both
18	DCLK	I	**Data Clock** Microcontroller Interface data clock, shifts data from or to device; maximum clock rate 8192 kHz.	both
19	DIN	I	**Data Input** Microcontroller Interface control data input pin; DCLK determines data rate.	both
20	DOUT	O	**Data Output** Microcontroller Interface control data output pin; DCLK determines data rate: DOUT is high impedance "Z" if no data is transmitted from the SICOFI®2-µC.	both
21	GNDD	I	**Digital Ground** Ground reference for all digital signals. Internally isolated from GNDA1 (Pin50), GNDA2 (Pin 54), and GNDA (Pins 59 and 63).	both

Pin	Symbol	Type	Function	Ch.
22	MCLK	I	**Master Clock Input** 1536, 2048, 4096 or 8192 kHz signal must be applied for any operation (select frequency in Register Bits XR5.6 and XR5.7). MCLK, PCLK, FSC must be synchronous.	both
23	RESET#	I	**Reset Input** Forces the device into default setting mode; active low.	both
24	V_{DDD}	I	**Digital Supply Voltage** +5 V supply for digital circuits (use 100 nF blocking cap.).	both
25	TCA#	O	**Transmit Control Output A** PCM Interface: active if data is transmitted via DXA; active low, open drain.	both
26	DXA	O	**Data Transmit to PCM-Highway A** PCM Interface: PCM data for each channel is transmitted in 8-bit bursts every 125 µs.	both
27	DRA	I	**Data Receive from PCM-Highway A** PCM Interface: PCM data for each channel is received in 8-bit bursts every 125 µs.	both
28	TCB#	O	**Transmit Control Output B** PCM Interface: active if data is transmitted via DXB; active low, open drain.	both
29	DXB	O	**Data Transmit to PCM-highway B** PCM Interface: data for each channel is transmitted in 8-bit bursts every 125 µs.	both
30	DRB	I	**Data Receive from PCM-highway B** PCM Interface: data for each channel is received in 8-bit bursts every 125 µs.	both
31	FSC	I	**Frame Synchronization Clock** 8 kHz; reference for individual time slots, indicates start of PCM frame; MCLK, PCLK, FSC must be synchronous.	both
32	PCLK	I	**PCM Data Clock** 128 to 8192 kHz; determines the rate at which PCM data is shifted into or out of the PCM-ports. MCLK, PCLK, FSC must be synchronous.	both
33	CHCLK1	O	**Chopper Clock Output 1** Configurable output clock (T = 2 … 28 ms), sync. to MCLK. Programmed in Register Bits XR4.0 to XR4.3.	both

Pin	Symbol	Type	Function	Ch.
34	INT12	O	**Interrupt Output, Channels 1 and 2** Active high.	both
35	SI1_1	I	**Signaling Input Channel 1, Pin 1** Read logic status from Register Bit XR0.1.	1
36	SI1_0	I	**Signaling Input Channel 1, Pin 0** Read logic status from Register Bit XR0.0.	1
37	SB1_2	I/O	**Bi-directional Signaling, Channel 1 Pin 2** Set direction in XR3.0, read/write value from/to Bit XR3.4.	1
38	SB1_1	I/O	**Bi-directional Signaling, Channel 1 Pin 1** Set direction in XR2.1, read/write value from/to Bit XR1.1.	1
39	SB1_0	I/O	**Bi-directional Signaling, Channel 1 Pin 0** Set direction in XR2.0, read/write value from/to Bit XR1.0.	1
40	SO1_1	O	**Signaling Output, Channel 1, Pin 1** Write output value to Register Bit XR0.1.	1
41	SO1_0	O	**Signaling Output, Channel 1, Pin 0** Write output value to Register Bit XR0.0.	1
42	SO2_0	O	**Signaling Output, Channel 2, Pin 0** Write output value to Register Bit XR0.2.	2
43	SO2_1	O	**Signaling Output, Channel 2, Pin 1** Write output value to Register Bit XR0.3.	2
44	SB2_0	I/O	**Bi-directional Signaling, Channel 2 Pin 0** Set direction in XR2.2, read/write value from/to Bit XR1.2.	2
45	SB2_1	I/O	**Bi-directional Signaling, Channel 2 Pin 1** Set direction in XR2.3, read/write value from/to Bit XR1.3.	2
46	SB2_2	I/O	**Bi-directional Signaling, Channel 2 Pin 2** Set direction in XR3.1, read/write value from/to Bit XR3.5.	2
47	SI2_0	I	**Signaling Input, Channel 2, Pin 0** Read logic status from Register Bit XR0.2.	2
48	SI2_1	I	**Signaling Input, Channel 2, Pin 1** Read logic status from Register Bit XR0.3.	2

Pin	Symbol	Type	Function	Ch.
49	V_{IN1}	I	**Analog Voice (Voltage) Input, Channel 1** Requires a coupling capacitor >39 nF to the SLIC.	1
50	GNDA1	I	**Analog Ground, Channel 1** Not internally connected to GNDD, GNDA2, or GNDA.	1
51	V_{OUT1}	O	**Analog Voice (Voltage) Output, Channel 1** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance.	1
52	V_{DDA12}	I	**Analog Supply Voltage**, **Channels 1 and 2** +5 V (100 nF blocking capacitor required).	1,2
53	V_{OUT2}	O	**Analog Voice (Voltage) Output, Channel 2** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance.	2
54	GNDA2	I	**Analog Ground, Channel 2** Not internally connected to GNDD, GNDA1,or GNDA.	2
55	V_{IN2}	I	**Analog Voice (Voltage) Input**, **Channel 2** Requires a coupling capacitor >39 nF to the SLIC.	2
56	V_{REF}	I/O	**Reference Voltage** Must connect to a 220 nF cap. to ground.	both
57	V_{DDREF}	I	**Analog Supply Reference Voltage** +5 V (100 nF blocking capacitor required).	both
58	NC		**Not Connected** Pin is not connected in this device.	
59	GNDA	I	**Analog Ground** Not internally connected to GNDD or GNDA1,2.	
60	NC		**Not Connected** Pin is not connected in this device.	
61	V_{DDA}	I	**Analog Supply Voltage** +5 V (100 nF blocking capacitor required).	
62	NC		**Not Connected** Pin is not connected in this device.	
63	GNDA	I	**Analog Ground** Internally isolated from GNDD (Pin 21), GNDA1 (Pin 50), and GNDA2 (Pin 54).	
64	NC		**Not Connected** Pin is not connected in this device.	

3 Functional Description

The general architecture of the PEB 2266 is discussed in the ***Product Overview,*** **Chapter 2**. This *Programmer's Reference Manual* describes the signal processing functions performed by the PEB 2266 and provides detailed information on those blocks and features that are programmable to meet country-specific telephone line requirements, and to adapt to the system environment:

- Analog Amplification/Attenuation,
- Impedance Matching,
- Transhybrid Balancing,
- Digital Amplification/Attenuation,
- Frequency Response Correction,
- Programmable A- or µ-Law Companding,
- Level Metering Functions,
- Two Tone Generators,
- 14 Programmable Input and Output Signals (Signaling Interface),
- Programmable Data Rate of PCM Highway,
- Programmable Time Slots for PCM Highway,
- 4 Analog and 5 Digital Configurable Test Loops, and
- Programmable Clock Outputs.

3.1 Functional Blocks

Based on an advanced digital filter concept, the PEB 2266 provides excellent transmission performance and high flexibility. The PEB 2266 includes both Fixed Blocks and Programmable Blocks. The new filter concept maximizes independence of the different filter blocks. The blocks are illustrated in **Figure 4**.

3.1.1 Fixed Blocks

The fixed blocks (IMFIX1, IMFIX2, XFIX1, XFIX2, RFIX1, RFIX2 and THFIX) describe the transfer functions of the non-programmable blocks of the SICOFI®2-µC.

The fixed blocks in the transmit path (XFIX1 and XFIX2) include the transfer functions of the anti-aliasing prefilter, digital hardware filter, and decimation units.

The fixed blocks in the receive path (RFIX1 and RFIX2) include the transfer functions of the post filter, digital hardware filters, and interpolation blocks. The digital hardware filters are fast, hardwired logic circuits which reduce the amount of data and thus the workload of the DSP. IMFIX1, IMFIX2, and THFIX include functions like fixed delays, interpolation, and decimation blocks for the IM and TH filters.

3.1.2 Programmable Blocks

The following paragraphs characterize the programmable filter blocks, including the numbers of bits used for programming each filter. These bits must be stored in the SICOFI®2-µC Coefficient RAM. A utility program (QSICOS) is available for calculation and optimization of the coefficients. QSICOS is described and discussed in **Chapter 7** "Application Hints" on page 56.

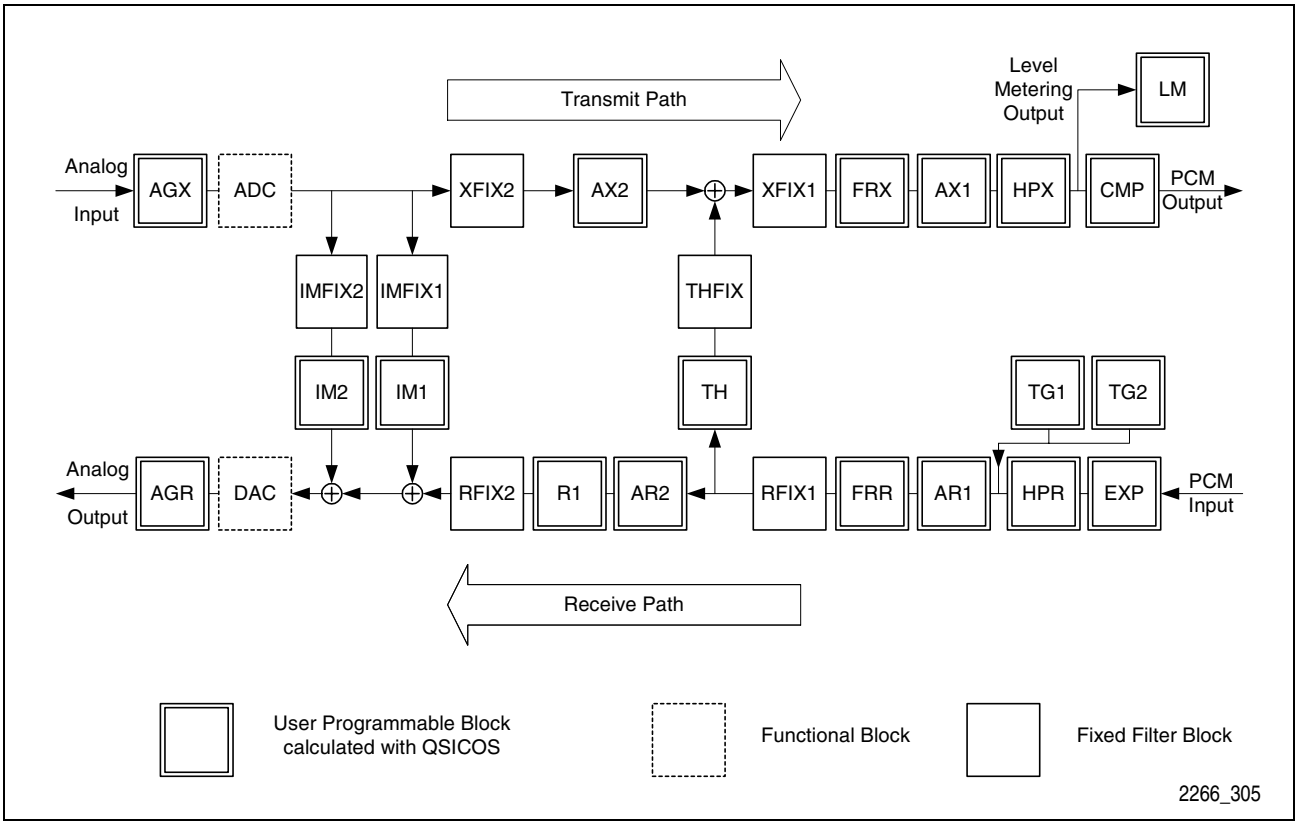


Figure 4 SICOFI®2-µC Detailed Flow Diagram

Analog Amplification/Attenuation (AGX, AGR) Block

In the transmit direction, an amplification of 6.02 dB can be enabled or disabled (CR2.2). In the receive direction, an attenuation of 6.02 dB can be enabled or disabled (CR2.3).

Impedance Matching (IM) Filter

The Impedance Matching (IM) Filters can achieve a return loss better than 30 dB. They consist of 3 different loops: IM2 and the IIR and FIR filters internal to IM1.

The IM2 block works at a sampling rate of 4 MHz and is implemented with a fixed and a programmable element. 12 bits are needed for programming IM2.

The programmable IM1 block has two filter blocks internally which work in parallel: A Wave Digital Filter at 128 kHz for improved low frequency response, and a Finite Impulse Response Filter (FIR) at 64kHz for fine tuning.

The Wave Digital Filter is programmed with 60 bits. It is an Infinite Impulse Response Filter (IIR) with guaranteed passive behavior and excellent stability. The FIR Filter is programmed with 48 bits.

The real part of the termination impedance is positive under all conditions. The filters also show an improved overflow performance for transients.

When the channel is in operating mode the IM Filters have to be enabled by setting bit CR0.6 to "1" (see **Chapter 6.3.1**). The IM filter coefficients are programmed with the COP_4 and COP_5 command (see **Chapter 6.5** for details). These command sequences also contain the coefficients for the R1 block.

Transhybrid Balancing (TH) Filter

The flexible implementation of the Transhybrid Balancing (TH) Filter allows optimization over a wide impedance range. The resulting Transhybrid Loss can achieve 30 dB (typically better than 40 dB; PEB/PEF 2266 without connecting a SLIC).

The programmable block TH is internally implemented by two filter blocks that work in parallel: A second order Wave Digital Filter (IIR) and a 7-tap FIR Filter. The Wave Digital Filter improves the low frequency response. It is programmed with 106 bits. The 7-tap FIR Filter is programmed with 7*3 nibbles (84 bits) and is used for fine tuning. Both filter blocks work at a sampling frequency of 16 kHz.

The coefficients for the TH Filters are programmed with the COP_0, COP_1 and COP_2 commands (see **Chapter 6.5** for details). For easy adaptation to different lines, two independent coefficient sets can be stored in the CRAM. The TH Filter behavior can be changed quickly by selecting either set with the bits CR0.0 and CR0.1. Bit CR0.7 enables/disables the TH path.

Frequency Response Correction (FRR and FRX) Filters

Frequency Response Correction (FRR and FRX) Filters are provided for line equalization and compensation of attenuation distortion. The use of minimum phase filters instead of linear phase filters improves the Group Delay Distortions. The Frequency Response Receive (FRR) Filter corrects distortions of the receive path, the Frequency Response Transmit (FRX) Filter performs the same function in transmit direction. Both are implemented as 5-tap programmable FIR filters operating at 8 kHz. Each of them is programmed with 5*3 nibbles (60 bits). Their frequency response is better than 0.1 dB. FRX and FRR coefficients are programmed with the COP_6 and COP_7 commands (see **Chapter 6.5**). Bit CR0.5 enables/disables FRX, Bit CR0.4 enables/disables FRR.

The R1 Filter is also used to compensate the frequency response in the receive path. The programming bits for the R1 Filter are part of the programming sequence for the Impedance Matching Filters (COP_4, COP_5).

Amplification/Attenuation Filters (AX1, AX2, AR1, AR2)

There are two separate filters in the transmit path and in the receive path, improving the level adjustment in both directions. These blocks allow optimal adjustment of the digital dynamic range. They further improve the transhybrid balancing results and allow gain adjustments independent of the TH Filters.

The Amplification/Attenuation Filters AX1 and AR1 are programmed with 5 nibbles each (20 bits each). The AX2 and AR2 Filters use 3 nibbles (12 bits) each for programming. This results in 32-bit programming information for the AX1 and AX2, and the same number of bits for the AR1 and AR2 filters. As shown below, the granularity of the gain adjustments is very fine**.**

- Amplification/Attenuation Receive (AR1, AR2) Filter

Range	Step Size
+3 dB to -14 dB	0.02 to 0.05 dB
-14 dB to -24 dB	0.05 dB

- Amplification/Attenuation Transmit (AX1, AX2) Filter

Range	Step Size
-3 dB to +14 dB	0.02 to 0.05 dB
+14 dB to +24 dB	0.05 dB

The coefficients for AX1/AX2 and AR1/AR2 are programmed with the COP_8 and COP_9 commands (see **Chapter 6.5**). Bit CR0.3 enables/disables AX1 and AX2, CR0.2 enables/disables AR1 and AR2.

Total Range for Amplification/Attenuation

The amplification/attenuation of the transmit and receive paths are determined by the accumulated effect of the following blocks:

Attenuation receive:	AR = AR1 + FRR + AR2 + R1
Amplification transmit:	AX = AX2 + FRX + AX1

The transmission characteristics of the SICOFI®2-µC (see ***Hardware Reference Manual*** **Chapter 4.2**) is guaranteed for the following range of total amplification/ attenuation:

Receive characteristics:	-9 dB < AR < 0 dB
Transmit characteristics:	0 dB < AX < 9 dB with A-Law coding 0 dB < AX < 7 dB with µ-Law coding

Attenuation below -9 dB in receive direction and amplification above +9 dB in the transmit path will decrease the signal-to-noise performance due to the quantization effects in the D/A and A/D converters.

Highpass Filters (HPX, HPR)

The Highpass Filters suppress low-frequency noise (e.g. power-line noise) and are required to fulfill the ITU-Frequency masks. For special applications (e.g. modem transmission) the highpass filters may be disabled by programming bits CR3.1 and CR3.0.

A- or µ-Law Compander (CMP, EXP)

These units convert the 16-bit linear data format of the DSP to A-Law or µ-Law PCM codes, and vice versa. A-Law or µ-Law coding can be selected for each channel independently through register bit CR1.3.

Tone Generators (TG1, TG2)

The Tone Generators can be enabled or disabled (CR1.6 TG2, CR1.7 TG1), and will work with a fixed frequency of 1 kHz or with a programmable frequency (CR1.5 TG2, CR1.4 TG1). The programmed tone frequencies are determined by coefficients stored in CRAM through commands COP_C (TG1) and COP_D (TG2). (see **Chapter 7.3** "Programming the SICOFI®2-µC Tone Generators" on page 61)

Level Metering (LM)

The Level Metering unit can be enabled with bit CR2.2. It compares the signal level in the transmit path with a programmable threshold value in register XR7. Bit CR2.1 indicates if the measured level is higher or lower than the threshold (see **Chapter 7.2**).

3.2 Other Functions

There are various functions provided by the PEB 2266 which are discussed in subsequent chapters. These include the programmable input and output signals, the programmable PCM data rates and time slots, the configurable analog and digital test loops, and the programmable clock outputs.

4 Operational Description

Upon initial application of the supply voltage V_{DDD} to the PEB 2266 (Power-On), all registers of both channels will be initialized to "0" and all pins will be in a defined state (Reset State). For proper default settings, the supply voltage must be present before any voltage is applied to the input pins.

Pulling pin RESET# to low-level (HW-Reset) or setting bit RST in the XOP command byte (SW-Reset) also forces the SICOFI®2-µC into the Reset State.

4.1 Operating States

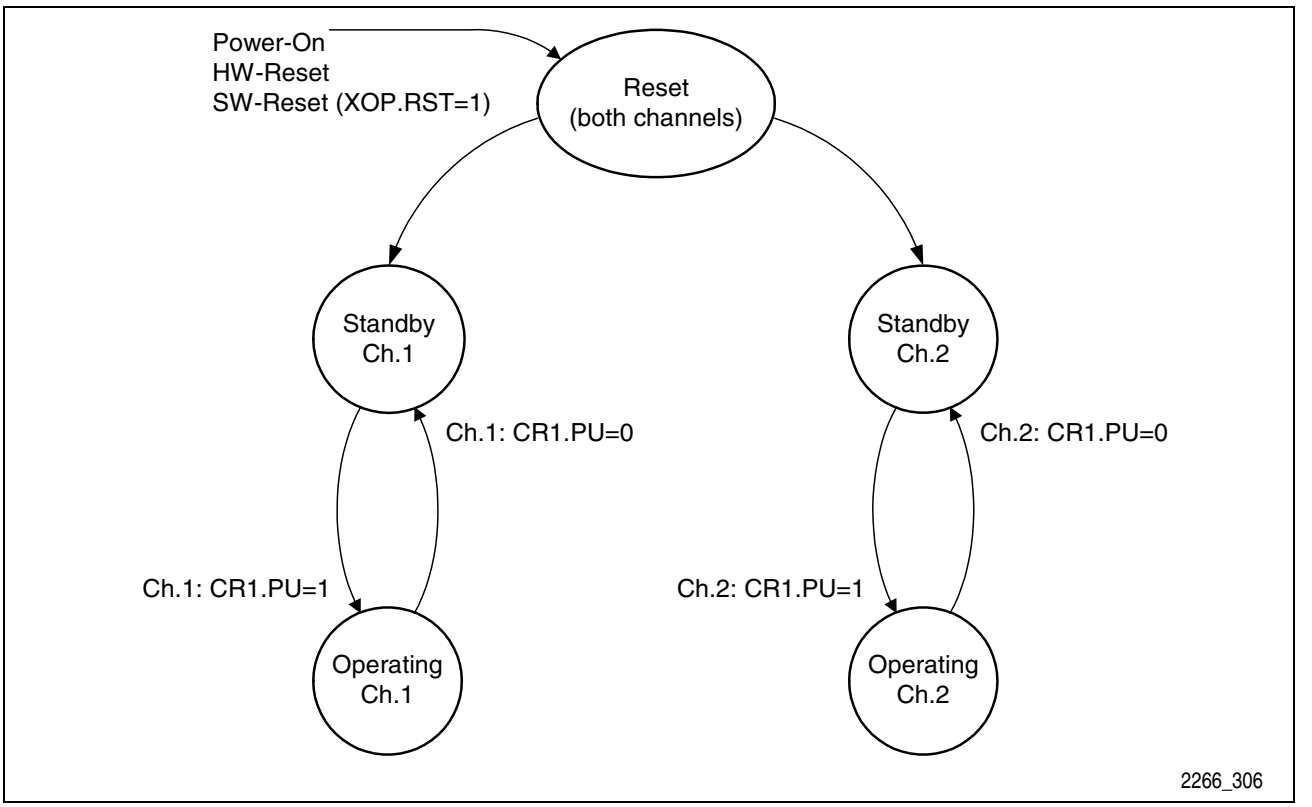


Figure 5 SICOFI®2-µC State Diagram

Reset (Default Setting)

During Reset (Default Setting), the command stack for SOP-, XOP-, and COP-command sequences is cleared. The Coefficient RAM content remains unchanged. The default register values and pin behavior are shown in **Table 2**. After pin RESET# is released, the device will leave the Reset State and enter the Standby State.

Table 2 Default Settings during Reset State

Affected Registers and Pins	State after Reset
CR0...CR4	00_H
XR0...XR7	00_H
DIN	Ignored
DOUT	High impedance
V_{OUT1}, V_{OUT2}	High impedance
SBx_y	Input
SOx_y	GNDD

Standby

Standby is a power-saving state. After Reset, both channels will be in Standby State. An individual channel can be brought to Standby State from Operating State by programming bit CR1.PU to "0". Keeping an unused channel in this mode will reduce overall system power dissipation.

In Standby State, signals on the analog inputs (V_{INx}) and PCM receive pins (DRA, DRB) are ignored. The analog outputs (V_{OUTx}) and the PCM transmit pins (DXA, DXB) are in high impedance state. The Serial Microcontroller Interface is ready to receive and transmit commands and data. Registers and the Coefficient RAM can be written and read. The Signaling Interface and the debouncing functions are working. Signaling status changes will generate interrupts (if enabled) and the signaling status can be read through the Microcontroller Interface.

Operating

In this state, the embedded DSP processes voice data according to the programmed filter characteristics in the Coefficient-RAM (CRAM) and the settings of the configuration registers. This mode can be enabled for individual channels by setting bit CR1.PU to "1". Pins V_{OUTx} and V_{INx} are transmitting and receiving analog signals. The PCM Interface is active during the time slots assigned to the channel. The tone generators, test functions, and level metering functions can also be enabled while the channel is in Operating State.

4.2 Transmission Characteristics

The specifications to which the SICOFI®2-µC are tested are tighter than the ITU-T Q.552 specification to guardband various SLIC implementations. The guaranteed transmission characteristics of the SICOFI®2-µC under test conditions ensure that the final linecard design will meet the ITU-T specification. The transmission characteristics are discussed in detail in the SICOFI®2-µC ***Hardware Reference Manual***.

5 Interface Description

The SICOFI®2-µC provides four interfaces:

- Analog Interface,
- PCM Interface,
- Signaling Interface, and
- Serial Microcontroller Interface.

A general description of these interface is given in the ***Product Overview*, Chapter 4**. Refer to the ***Hardware Reference Manual*** for a more detailed information on timings and AC and DC characteristics of these interfaces.

The subsequent chapters in this manual explain the configuration and operation of the four interfaces.

5.1 Analog Interface

The Analog Interface in combination with a Subscriber Line Interface Circuit (SLIC) forms a configurable tip & ring (t/r) telephone line. The AC transmission characteristic of the SICOFI®2-µC—SLIC combination can be controlled by programming the digital filter structures inside the SICOFI®2-µC. The correct filter coefficients are determined by the targeted AC transmission behavior (e.g. Telco specification) and by the transfer functions of the SLIC. QSICOS Coefficient Calculation and Register Configuration Software is available for the SICOFI®2-µC (see **Chapter 7.1**).

The SICOFI®2-µC can be interfaced directly to electronic SLICs or transformer solutions. The high driving capability of up to 300 Ohms eliminates the need for an external amplifier that is normally used with transformer SLICs.

5.2 PCM Interface

The SICOFI®2-µC provides an industry-standard PCM Interface with access to two PCM highways. The PCM Interface has the following features:

- Data rate from 128 kbit/s to 8 Mbit/s per highway,
- 2 to 128 time slots per frame per highway,
- PCM data format serialized 8 bits with MSB first,
- Configurable A-Law or µ-Law coding,
- Independently configurable time slot and highway for each channel and direction,
- PCM clock speeds of once or twice the bit rates,
- Programmable sampling slopes, and
- Programmable frame delay.

When the SICOFI®2-µC is transmitting data on DXA (DXB), pin TCA# (TCB#) is activated to control an external driving device.

Table 3 Configurable PCM Features and Functions

Features and Functions	Register	Bit	Label
Single or double bit clock	XR6	7	C-MODE
Transmit slope	XR6	6	X-S
Receive slope	XR6	5	R-S
Transmitter driving mode	XR6	4	DRV_0
PCM frame delay	XR6	3 to 0	Shift, PCM-OFFSET
Receive highway selection	CR4	7	R-WAY
Receive time slot assignment	CR4	6 to 0	RS
Transmit highway selection	CR5	7	X-WAY
Transmit time slot assignment	CR5	6 to 0	XS
A-Law or µ-Law coding and decoding	CR1	3	LAW

5.2.1 PCM Clock Speeds

The data rate and the number of time slots on each highway depend on the PCM Clock input (PCLK) frequency and on the setting of the C-MODE bit in register XR6:

Table 4 PCM Clocking and Data Rates

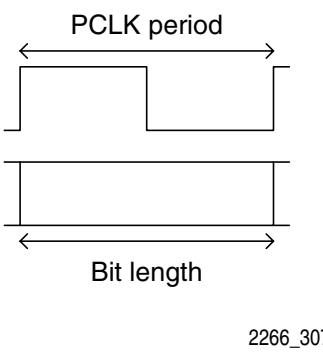
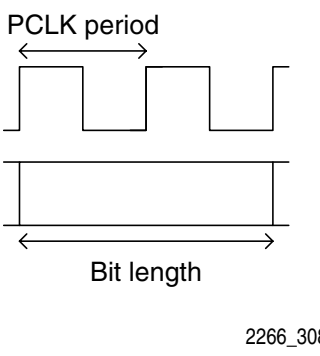
	Clock Mode	
	C-MODE (XR6.7) = 0 (Single Clock)	**C-MODE (XR6.7) = 1 (Double Clock)**
PCLK / Bit		
Data Rate	f_{PCLK}	$f_{PCLK}/2$
Number of Time Slots	$f_{PCLK}/64$	$f_{PCLK}/128$

Table 5 shows some typical PCM configurations:

Table 5 Typical PCM Data Rates, Time Slots, and Clock Modes

Data Rate (per highway)	Time Slots (per highway)	PCLK Frequency	
		C_MODE (XR6.7) = 0 (Single Clock Mode)	C_MODE (XR6.7) = 1 (Double Clock Mode)
128 kbit/s	2	128 kHz	256 kHz
256 kbit/s	4	256 kHz	512 kHz
512 kbit/s	8	512 kHz	1024 kHz
768 kbit/s	12	768 kHz	1536 kHz
1024 kbit/s	16	1024 kHz	2048 kHz
1536 kbit/s	24	1536 kHz	3072 kHz
2048 kbit/s	32	2048 kHz	4096 kHz
4096 kbit/s	64	4096 kHz	8192 kHz
8192 kbit/s	128	8192 kHz	not allowed

5.2.2 Transmit and Receive Slopes

Transmission of data bits on DXA and DXB is synchronous to the rising edge or the falling edge of PCLK. Received bits on DRA and DRB are latched with either the falling edge or the rising edge of PCLK. This feature allows easy adaptations to different PCM highway timing conditions and helps to avoid bit overlaps with other devices.

Transmit slope configured with bit **X-S** (XR6.6)

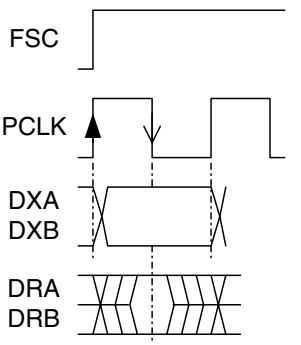
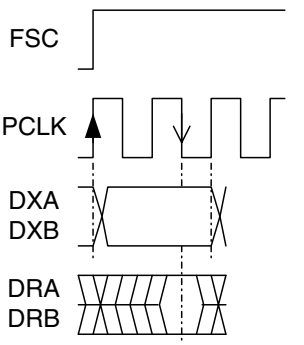
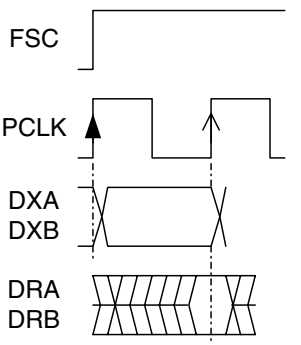
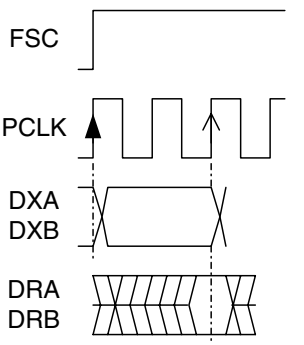
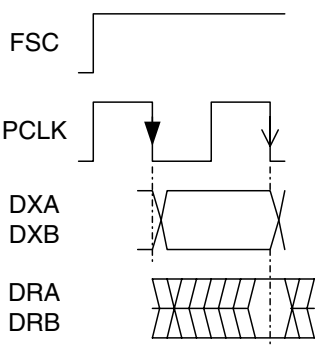
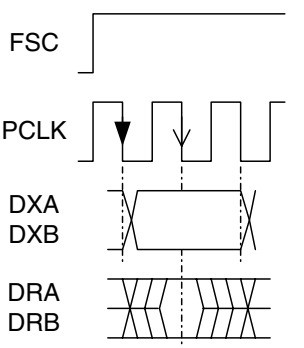
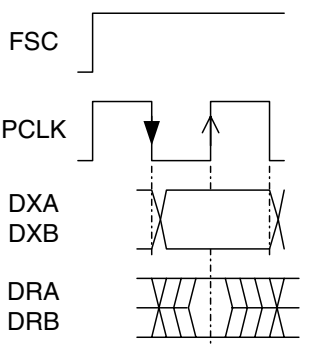
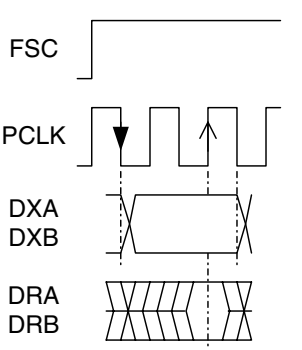
0	Rising	Edge of PCLK initiates the transmission
1	Falling	

Receive slope configured with bit **R-S** (XR6.5)

0	Falling	Edge of PCLK latches the receive level
1	Rising	

Table 6 shows the combinations of X-S, R-S and C_MODE settings, and the resulting positions of the transmit slope and the receive slope with reference to the start of a PCM frame (rising edge of FSC).

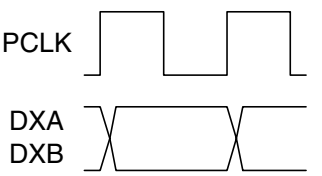
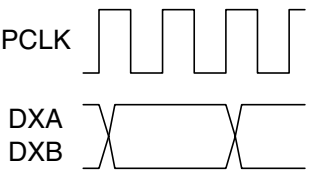
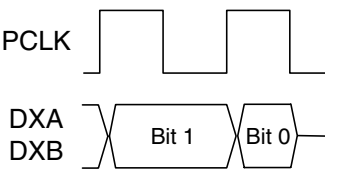
Table 6 Transmitting and Receiving Bit 7 in Time Slot 0

	Sampling Slope		Clock Mode	
(XR6.0-XR6.4)	R-S (XR6.5) Receive	X-S (XR6.6) Transmit	C-MODE (XR6.7) = 0 (Single Clock)	C-MODE (XR6.7) = 1 (Double Clock)
00000	0	0		
00000	1	0		
00000	0	1		
00000	1	1		

5.2.3 Transmitter Driving Mode

In single clock mode, the transmit outputs for bit 0 DXA and DXB can be programmed to drive the PCM highway only during the first half of a PCLK cycle. The outputs will go to high impedance state during the second half of PCLK cycle.

Table 7 Transmitter Driving Modes

Logic State	C-MODE (XR6.7) = 0 (Single Clock Mode)	C-MODE (XR6.7) = 1 (Double Clock Mode)
DRV_0 (XR6.4) = 0		
DRV_0 (XR6.4) = 1		**Not applicable**

5.2.4 PCM Frame Delay

By default, the rising edge of the FSC signal indicates the start of a PCM frame (time slot 0). An extra delay of up to 7 clock periods, valid for all channels, may be programmed in register XR6 (see **Figure 6**).

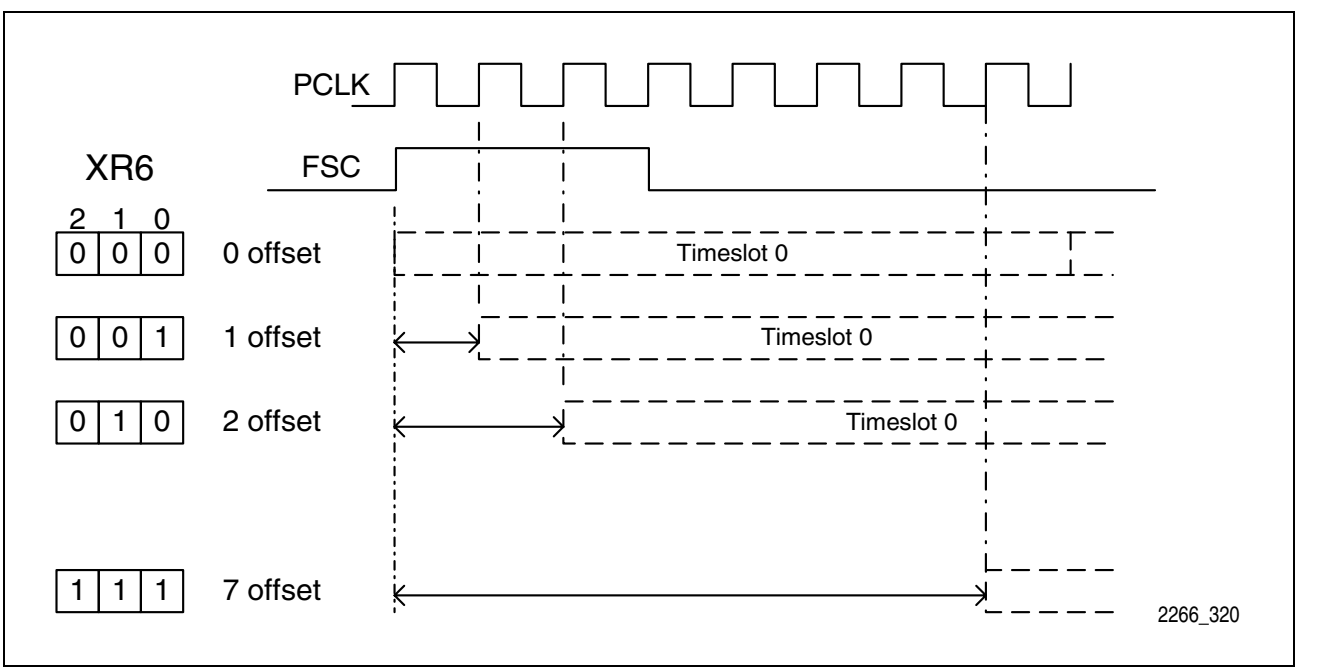


Figure 6 PCM Offset Programming with Bits in XR6.2 to XR6.0

Table 8 PCM Offset in Single Clock Mode

Shift (XR6.3)	Offset (XR6.2 ..0)	No. of PCLK Cycles	Number of Bits
0	000	0	0
	001	1	1
	010	2	2
	011	3	3
	100	4	4
	101	5	5
	110	6	6
	111	7	7
1	xxx	**not valid**	

Table 9 PCM Offset in Double Clock Mode

Shift (XR6.3)	Offset (XR6.2 ..0)	No. of PCLK Cycles	Number of Bits
0	000	0	0
	001	2	1
	010	4	2
	011	6	3
	100	8	4
	101	10	5
	110	12	6
	111	14	7
1	000	1	1/2
	001	3	1 1/2
	010	5	2 1/2
	011	7	3 1/2
	100	9	4 1/2
	101	11	5 1/2
	110	13	6 1/2
	111	15	7 1/2

5.2.5 Time Slot Assignment

Receive Direction

The receive highway and time slot for each channel are configured in the channel specific register CR4.

Register CR4	Receive Time Slot Assignment
R-WAY (CR4.7)	0: Receive PCM data on DRA 1: Receive PCM data on DRB
RS6 ... RS0 (CR4.6 ... CR4.0)	Receive time slot 0 - 127

Transmit Direction

The transmit highway and time slot for each channel are configured in the channel specific register CR5.

Register CR5	Transmit Time Slot Assignment
X-WAY (CR5.7)	0: Transmit PCM data on DXA 1: Transmit PCM data on DXB
XS6 ... XS0 (CR5.6 ... CR5.0)	Transmit time slot 0 - 127

Both channels must have different transmit time slots or highways assigned. If both channels try to drive the same time slot on the same transmit output, both channels will be disabled and a crash bit in common register XR5 will indicate the contention (CRSH_A for DXA, CRSH_B for DXB). The crash condition can be cleared by reprogramming the values in CR5 and reading XR5.

5.3 Signaling Interface

The SICOFI®2-µC can accumulate and manage the I/O status of four SLICs—one per channel— through its Signaling Interface (see **Figure 7**).

The Signaling Interface handles line and SLIC status and control, ringing relays, etc. with the following:

- 14 Signaling pins (2 input pins, 2 output pins, and 3 user-configurable bi-directional pins per channel),
- Debouncing functions,
- 2 Interrupts (one for each channel-pair), and
- 2 Clock output signals (user configurable).

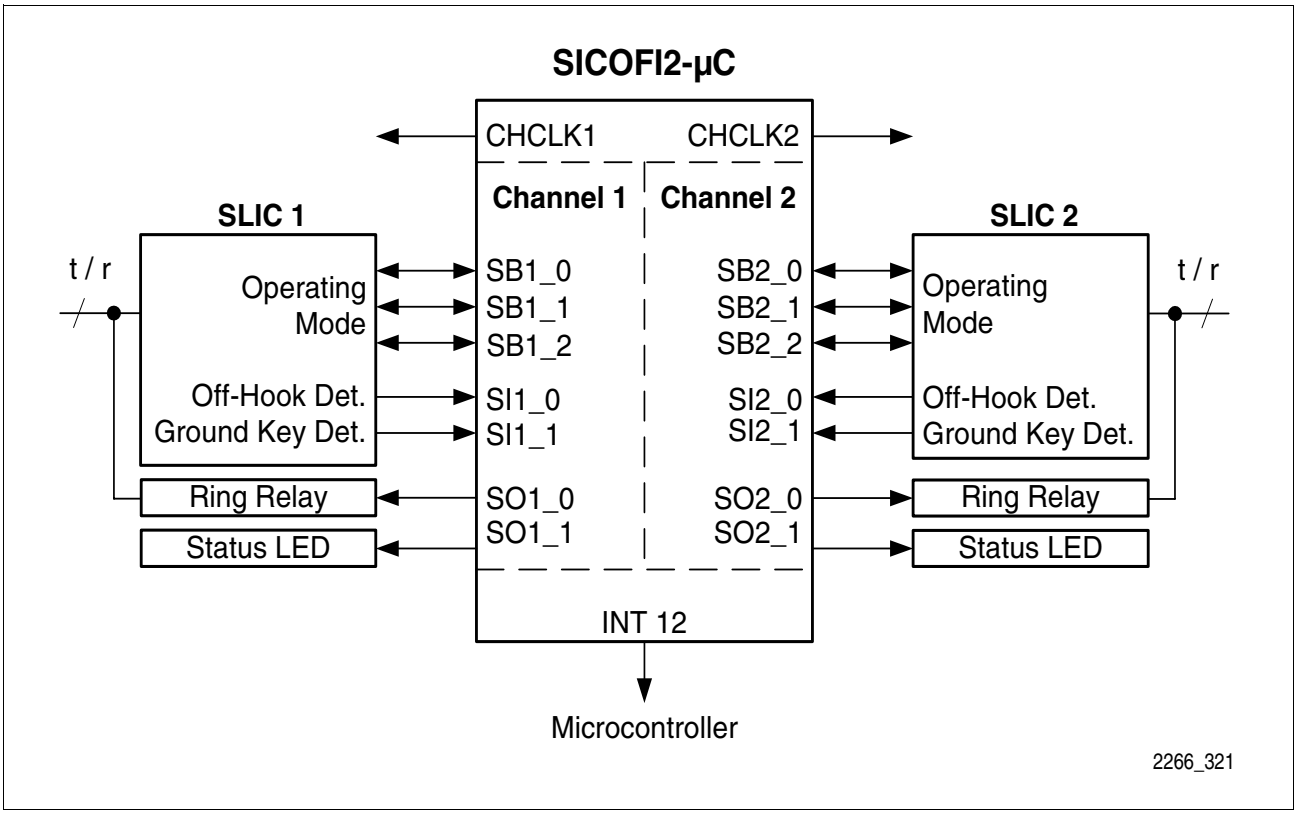


Figure 7 Signaling Example for two Subscriber Lines

5.3.1 Signaling Pins and Registers

The function of common register XR0 depends on the type of access:

Reading from XR0	Writing to XR0
Provides status information on the eight signaling input pins SIx_y (see **Figure 8**)	Determines logic level of the signaling outputs SO_x_y (see **Figure 8**)

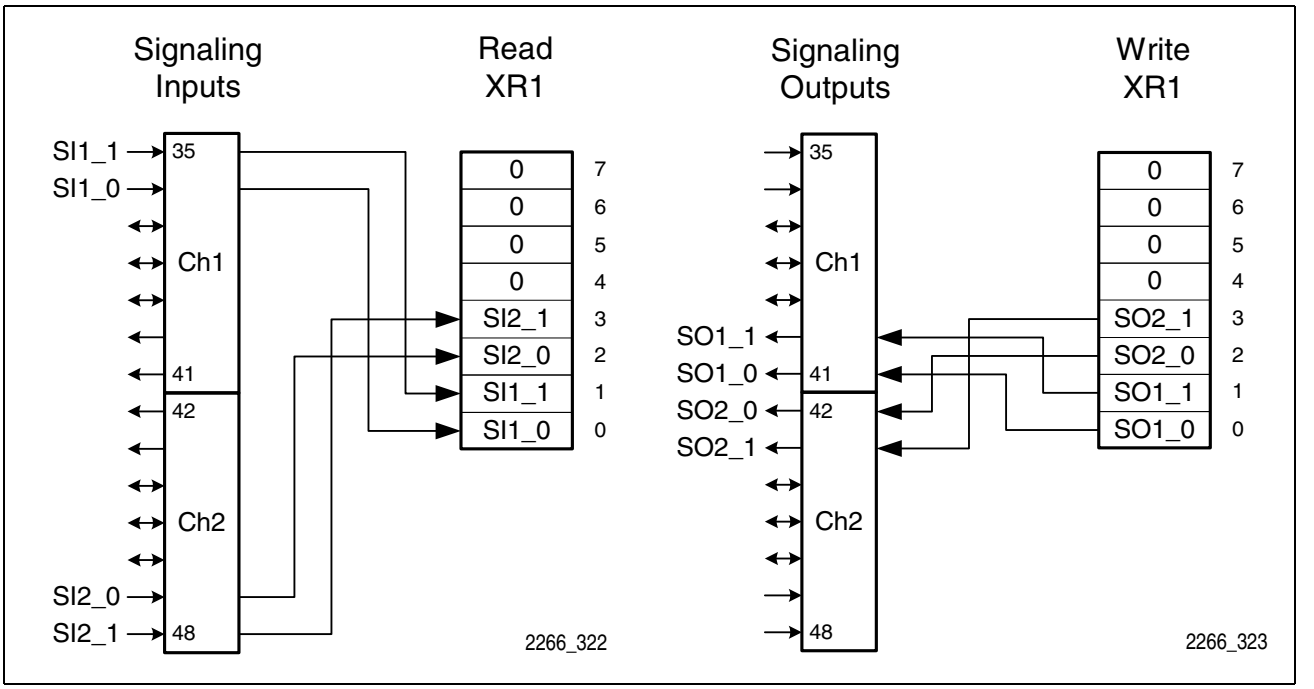


Figure 8 Access to the Signaling Inputs and Outputs Through XR0

The bi-directional signaling pins SBx_y are configured through common register XR2 and through bits 0 to 3 in XR3. Reading from registers XR1 and XR3 provides status information on those bi-directional pins that have been configured as inputs. Writing to register XR1 and XR3 sets the logic levels of those bi-directional pins operating as outputs (see **Figure 9**).

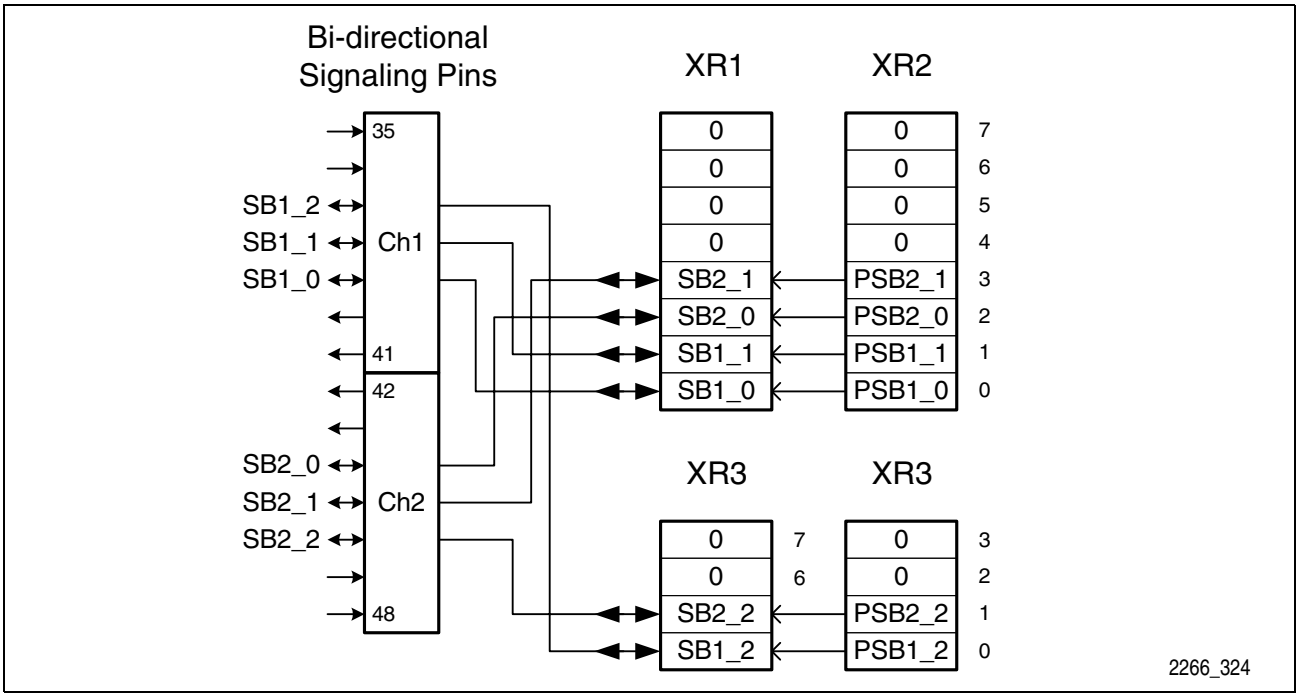


Figure 9 Bi-directional Pin Configuration and Access via XR1, XR2, XR3

5.3.2 Debouncing Functions

The SICOFI®2-µC offers programmable debouncing functions for improved immunity against spurious signals and glitches applied to the signaling inputs (SIx_y and SBx_y, if configured as inputs). If debounce is enabled, the input pins are sampled in intervals between 0.5ms and 26ms.

Field N (XR4, Bits 7 to 4)	Debounce Sampling Period
0000 (default)	Debouncing and interrupt generation disabled
1111	Sampling period = 0.5 ms
0001 to 1101	Sampling period = N * 2 ms (2 to 26 ms)
1110	Reserved

In order to detect status changes, all signaling inputs must be stable for two successive samples. Under this condition, an interrupt is generated and the signaling input values are stored in the corresponding registers.

Figure 10 shows an example for this scheme when SBx_x are programmed as outputs.

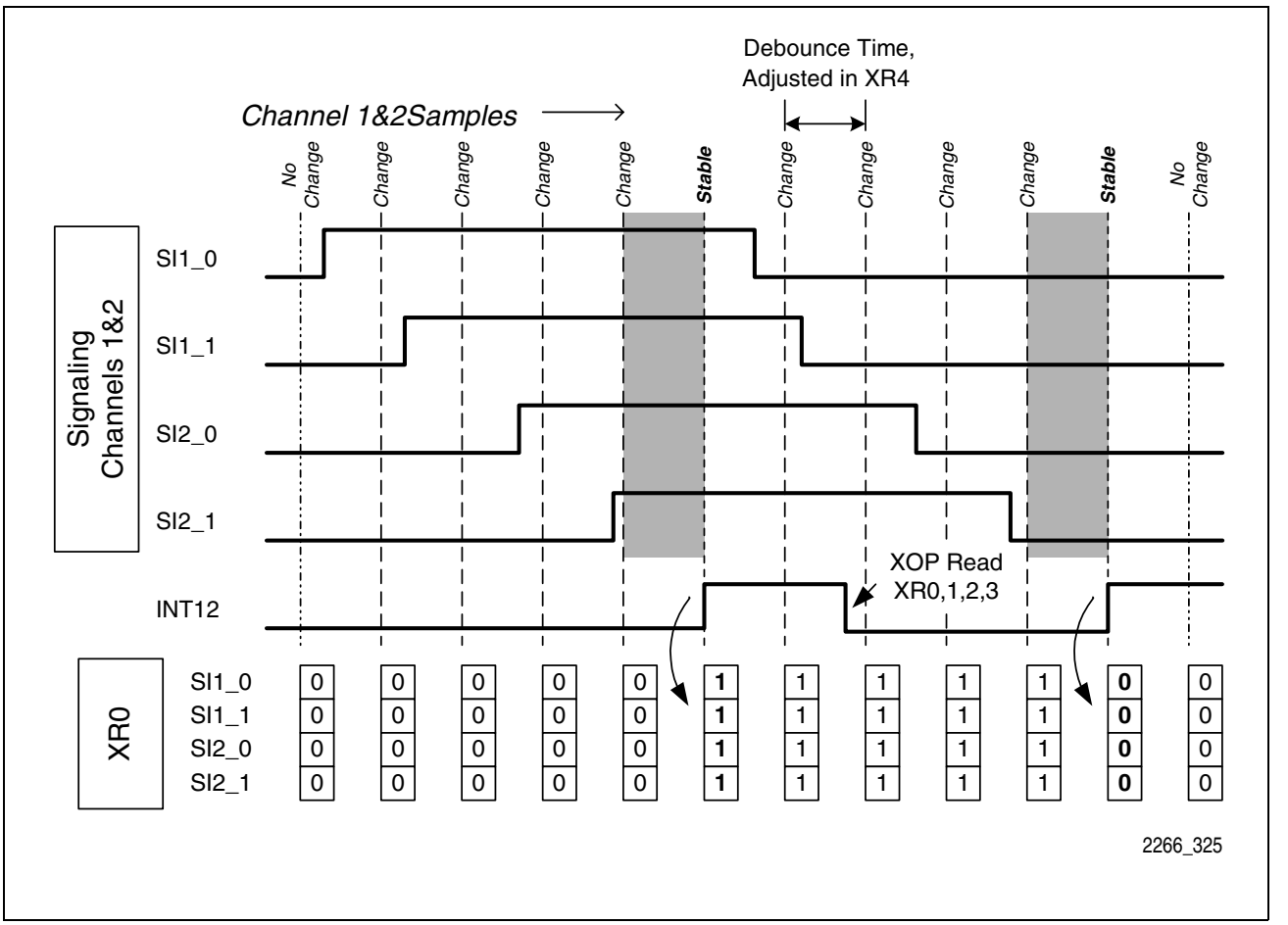


Figure 10 Signal Debouncing, Interrupt Generation and Register Updates

5.3.3 Interrupt Handling

With the debouncing functions enabled, changes on the Signaling Interface are indicated by the interrupt signal INT12 for the channel pair.

INT12 (Channels 1 and 2)

Logic State	Changes at the Signaling Interface Inputs
0	No signaling change
1	Input level changed on at least one signaling pin

The interrupt signals can be used to alert the microcontroller to signaling changes (e.g. subscriber line off-hook detection). The logic levels of the signaling inputs are reflected in the common registers XR0, XR1 and XR3. One of the XOP_3 to XOP_7 commands must be used to access all three registers inside the interrupt service routine. The read access releases the interrupt signal.

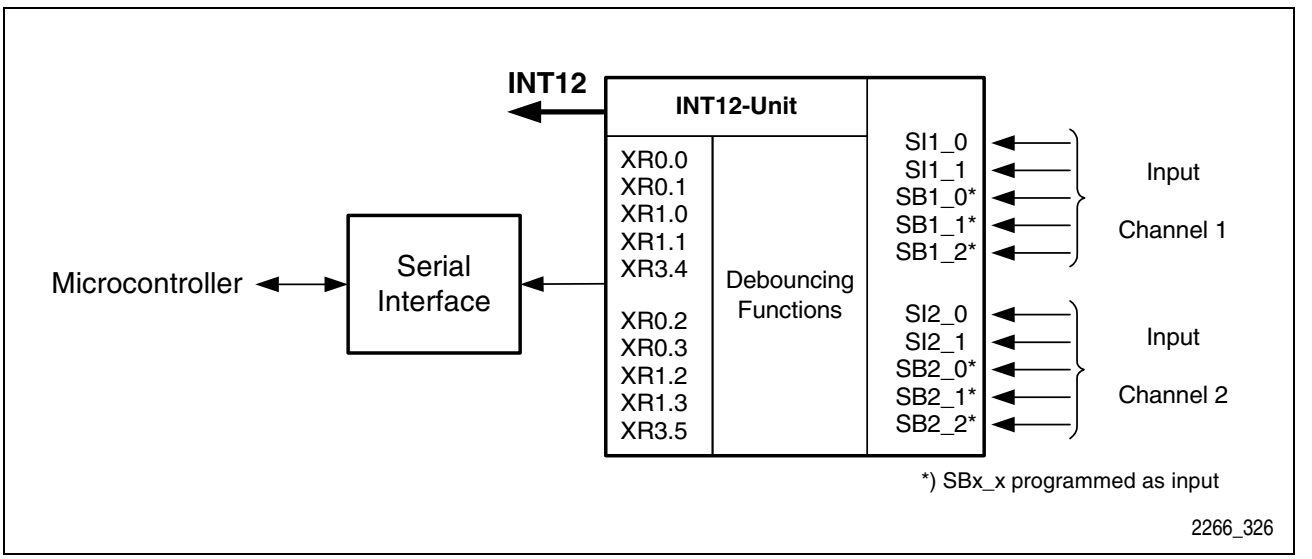


Figure 11 Interrupt Handling

Signal debouncing and interrupt generation can be disabled in register XR4. In this case, the microcontroller can check the signaling status by polling the signaling registers.

5.3.4 Clock Output Signals

For special purposes, two Chopper Clock output signals are provided by the PEB 2266:

- CHCLK1 (Pin 33) is configured in register XR4.Field T (bits XR4.3 to XR4.0)
- CHCLK2 (Pin 16) is configured in register XR5.CHCLK2 (bits XR5.3 and XR5.2)

Note: Both chopper clock output signals are available only if a valid master clock signal is applied to pin MCLK.

Table 10 CHCLK1 Programming

XR4.Field T	CHCLK1 Output)
0000	High level (+5V)
0001	Clock period = 2 ms
0010	Clock period = 4 ms
0011	Clock period = 6 ms
0100	Clock period = 8 ms
0101	Clock period = 10 ms
0110	Clock period = 12 ms
0111	Clock period = 14 ms
1000	Clock period = 16 ms
1001	Clock period = 18 ms
1010	Clock period = 20 ms
1011	Clock period = 22 ms
1100	Clock period = 24 ms
1101	Clock period = 26 ms
1110	Clock period = 28 ms
1111	Low level (0V)

Table 11 CHCLK2 Programming.

XR5.CHCLK2	CHCLK2 Output
00	High level (+5V)
01	512 kHz signal
10	256 kHz signal
11	16,384 kHz signal (at least one of the two channels must be in POWER-UP state)

5.4 Serial Microcontroller Interface

The internal configuration registers, the signaling registers, and the Coefficient RAM (CRAM) of the SICOFI®2-µC are accessible through a Serial Microcontroller Interface.

The Serial Microcontroller Interface consists of four lines (CS#, DCLK, DIN, and DOUT) as shown in **Figure 12**:

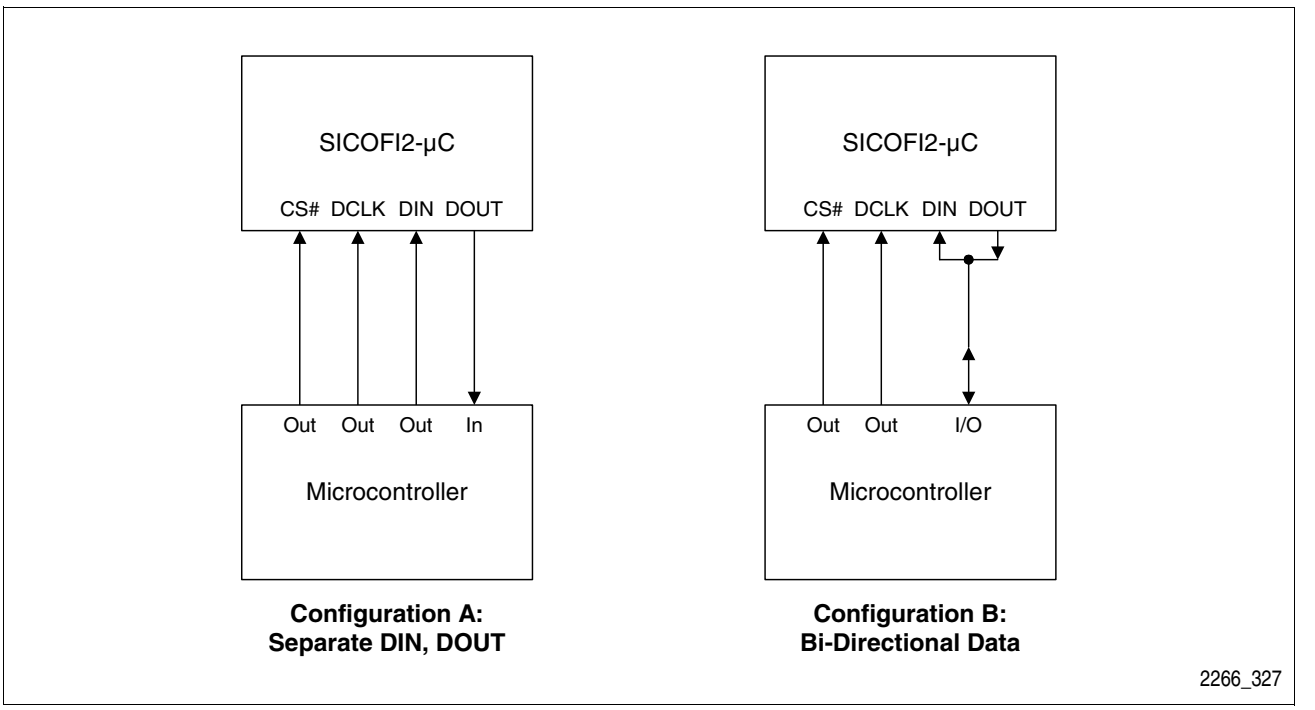


Figure 12 Serial Microcontroller Interface

Table 12 Serial Microcontroller Interface Pins and Functions

Symbol	Pin	Function
CS#	17	Chip Select, active low. The falling edge initiates the read or write access to the SICOFI®2-µC. The rising edge terminates the read or write access.
DCLK	18	Data Clock: Bit synchronous clock; maximum clock rate is 8192kHz.
DIN	19	Data Input: Serialized data bytes with MSB first. Data bits are latched with the rising edge of DCLK.
DOUT	20	Data Output: Serialized data bytes with MSB first. Data bits are driven with the falling edge of DCLK as a response to a read command. Otherwise, DOUT is in high impedance ("Z") state.

5.4.1 Write Access

Following a falling edge of CS#, the first eight bits received on DIN specify the type of command. The data bytes following a write command are stored in the selected configuration registers or the selected part of the Coefficient RAM. The number of data bytes depend on the type of command.

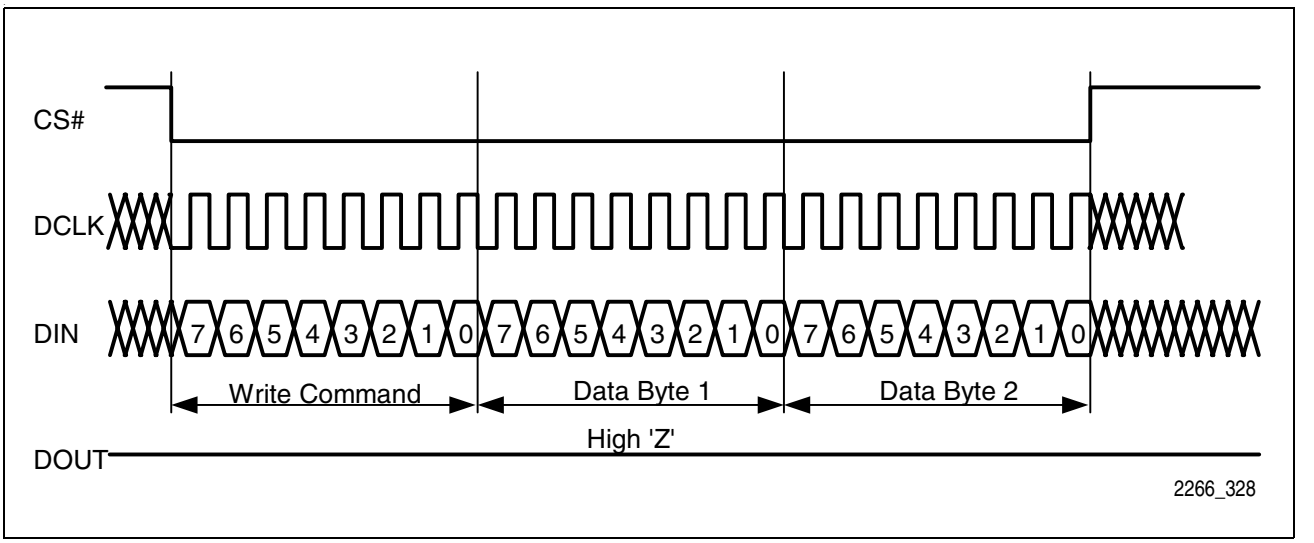


Figure 13 Example for a Two-Byte Write Access

5.4.2 Read Access

If the first eight bits received via DIN represent a read command, the SICOFI®2-µC will initiate its response via DOUT. An identification byte (81_H) is followed by the requested number of data bytes (contents of configuration registers or contents of the CRAM). During execution of a read command, the device will ignore data on DIN.

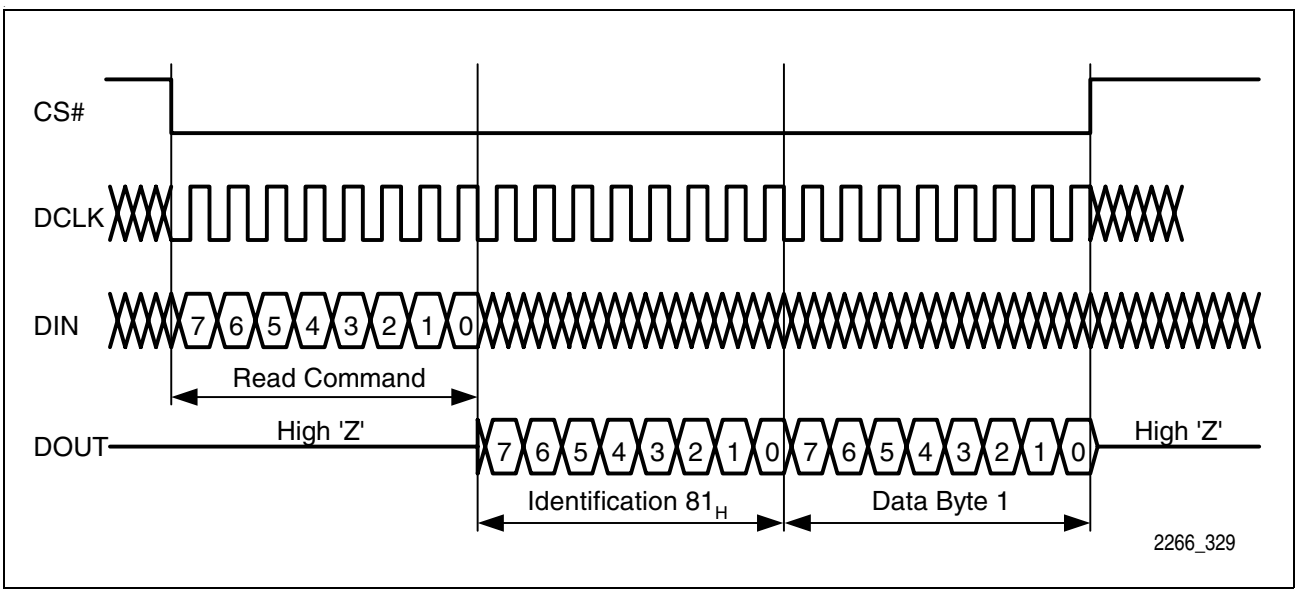


Figure 14 Example for a One-Byte Read Access

For byte-by-byte transfer, the high time of DCLK can be prolonged, resulting in a user defined ‘waiting time’ between bytes. This mechanism can be used for writing to and reading from the device.

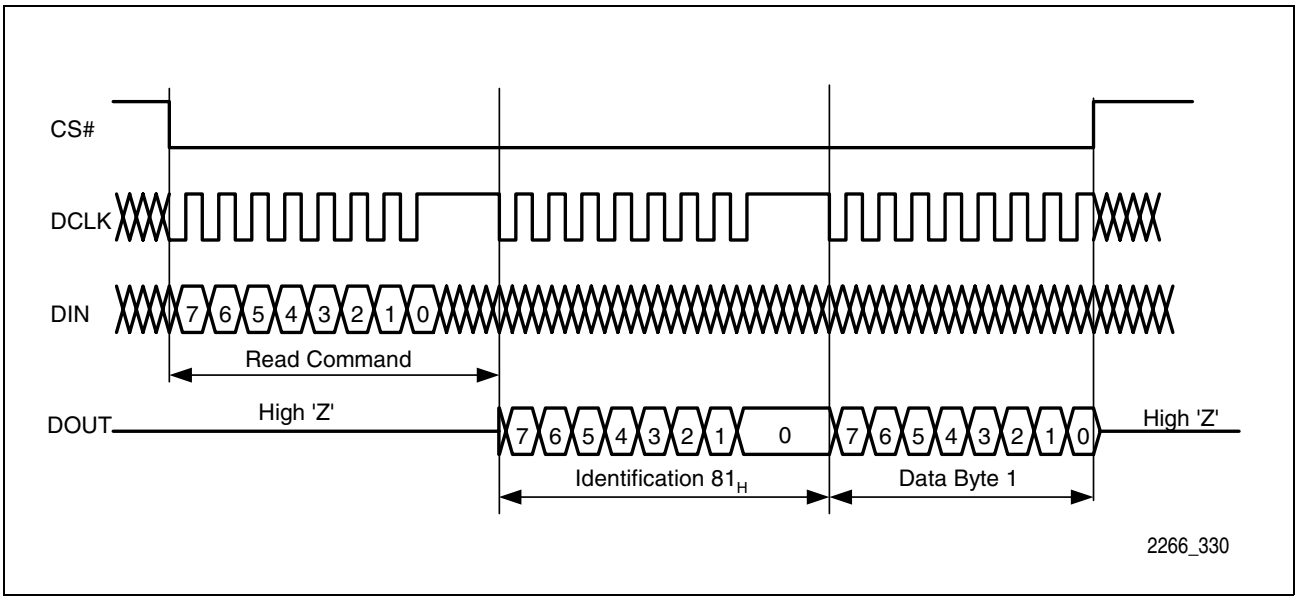


Figure 15 Example for a Read Access, with Byte-by-Byte Transfer

Read and write commands can be chained by leaving CS# low after the completion of each command sequence.

For read or write access to individual registers, the command sequence may be terminated by rising CS# after the transmission of any number of bytes.

5.4.3 Three-Wire Access

DIN and DOUT may be strapped together and connected to a single I/O pin of the microcontroller. The interface remains fully functional with only 3 wire connections.

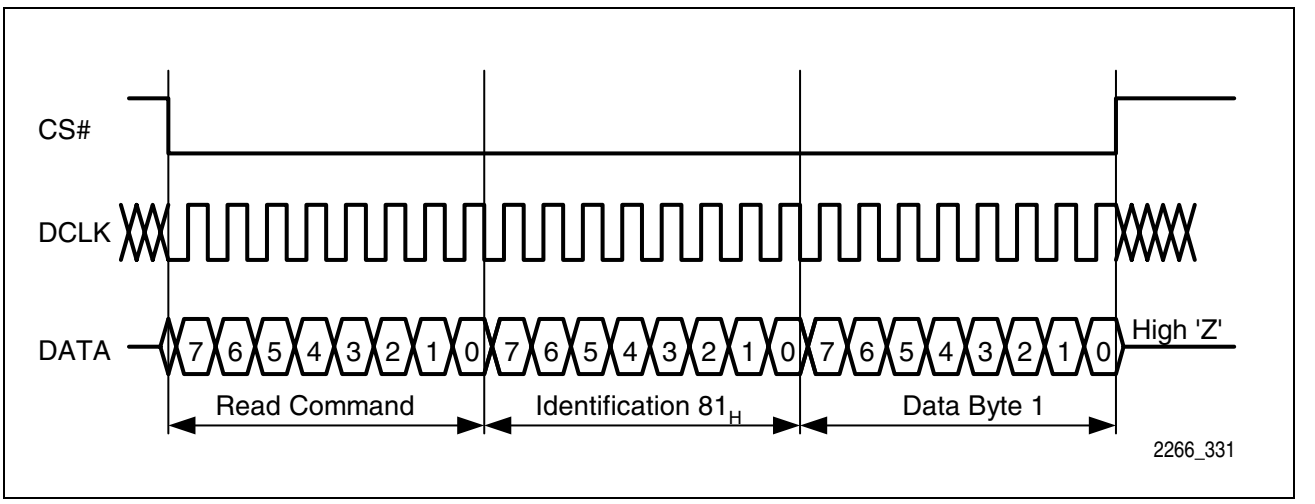


Figure 16 Bi-Directional Data Signal with DIN and DOUT Strapped Together

6 Programming the SICOFI®2-µC

The transmission characteristics and interfaces of the PEB 2266 can be adapted to various environments. Configuring the functional blocks and programming the digital filter behavior is accomplished by loading values to the Configuration Registers and the Coefficient RAM (CRAM). Software utilities are available to determine the appropriate register and CRAM values (see **Chapter 7.1** "Support Tools" on page 56).

6.1 Programming Overview

The SICOFI®2-µC has eight Common Configuration Registers (XR0 to XR7). Settings in these registers affect all two channels.

Each of the two channels has six Channel-Specific Configuration Registers (CR0 to CR5). Settings in these registers affect only the designated channel.

The filters of each channel are individually programmable through channel-specific coefficients in CRAM. There are two global sets of TH Filter coefficients that can be assigned to either channel. All of the filter blocks are described in **Chapter 3** and their locations are illustrated in **Figure 4**.

6.1.1 Register Model

Channel-specific and common configuration registers and coefficients are shown in **Table 13**.

Table 13 Register Model

Configuration Registers and CRAM	Channel Usage
XR0 to XR7 (8 bytes)	common
CR0 to CR5 (6 bytes)	channel-specific
IM/R1 Coefficients (16 bytes)	
FRR, FRX Coefficients (16 bytes)	
AR1, AR2, AX1, and AX2 Coefficients (8 bytes)	
TG1 and TG2 Coefficients (8 bytes)	
TH Coefficient Set 1 (24 bytes)	either
TH Coefficient Set 2 (24 bytes)	

6.1.2 Register Maps

Table 14 *Read* Access to Common Configuration Register (XR) Map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XR0	0	0	0	0	SI2_1	SI2_0	SI1_1	SI1_0
XR1	0	0	0	0	SB2_1	SB2_0	SB1_1	SB1_0
XR2	0	0	0	0	PSB2_1	PSB2_0	PSB1_1	PSB1_0
XR3	0	0	SB2_2	SB1_2	0	0	PSB2_2	PSB1_2
XR4	Signal Debounce				CHCLK1			
XR5	MCLK-SEL		CRSH-A	CRSH-B	CHCLK2		Version	
XR6	C-Mode	X-S	R-S	DRV_0	Shift	PCM-OFFSET		
XR7	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Table 15 *Write* Access to Common Configuration Register (XR) Map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XR0	0	0	0	0	SO2_1	SO2_0	SO1_1	SO1_0
XR1	0	0	0	0	SB2_1	SB2_0	SB1_1	SB1_0
XR2	0	0	0	0	PSB2_1	PSB2_0	PSB1_1	PSB1_0
XR3	0	0	SB2_2	SB1_2	0	0	PSB2_2	PSB1_2
XR4	Signal Debounce				CHCLK1			
XR5	MCLK-SEL		CRSH-A	CRSH-B	CHCLK2		Version	
XR6	C-Mode	X-S	R-S	DRV_0	Shift	PCM-OFFSET		
XR7	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Table 16 Channel-Specific Configuration Register (CR) Map (Read & Write)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CR0	TH	IM/R1	FRX	FRR	AX	AR	TH-SEL	
CR1	ETG2	ETG1	PTG2	PTG1	LAW	0	0	PU
CR2	COT/R			0	IDR	LM	LMR	V+T
CR3	TEST-Loops				AGX	AGR	D-HPX	D-HPR
CR4	R-way	RS6	RS5	RS4	RS3	RS2	RS1	RS0
CR5	X-way	XS6	XS5	XS4	XS3	XS2	XS1	XS0

6.1.3 CRAM Structure

Coefficient RAM (CRAM) is used to store the individual coefficients calculated for each channel. The coefficients can be written and read through the Microcontroller Interface. The IM, FRX, FRR, AX, AR, TG1, and TG2 coefficients are accessed through COP-Command Sequences which include the channel address (see **Chapter 6.5**).

Table 17 Coefficient RAM (CRAM) Structure per Channel

IM Part 1	8 Coefficient Bytes
IM Part 2	8 Coefficient Bytes
FRX	8 Coefficient Bytes
FRR	8 Coefficient Bytes
AX	4 Coefficient Bytes
AR	4 Coefficient Bytes
TG1	4 Coefficient Bytes
TG2	4 Coefficient Bytes

CRAM also contains four sets of TH coefficients. Each set can be assigned to either of the two channels.

Table 18 Coefficient RAM (CRAM) Structure per Set

TH Part 1	8 Coefficient Bytes
TH Part 2	8 Coefficient Bytes
TH Part 3	8 Coefficient Bytes

The difference between the channel-specific coefficients and the common coefficient sets is shown in **Figure 17**.

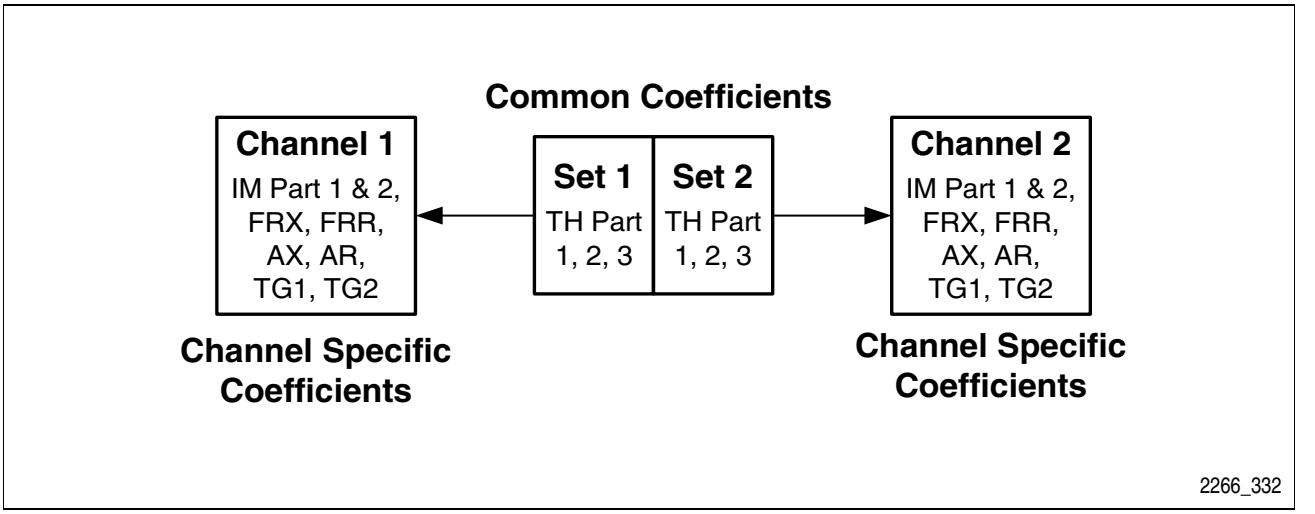


Figure 17 Channel Specific and Common Coefficients

6.2 Types of Commands and Data Bytes

Coefficients and register contents are programmed and accessed through command sequences. Using the appropriate commands, the SICOFI®2-µC can be programmed and verified very flexibly via the Microcontroller Interface. There are three types of command sequences:

- E**x**tended **Op**eration (XOP) for signaling channel configuration and evaluation (access to XR0 through XR7),
- **S**tatus **Op**eration (SOP) for device status setting and monitoring (access to CR0 to CR5), and
- **C**oefficient **Op**eration (COP) for filter coefficient setting and monitoring (CRAM).

Table 19 Types of Commands and Data Bytes.

	7	6	5	4	3	2	1	0
XOP	RST	0	RW	**1**	**1**	LSEL		
SOP	AD		RW	**1**	**0**	LSEL		
COP	AD		RW	**0**	CODE			

With the first byte received via DIN, a command type is selected through bits 3 and 4. A two-bit address field (AD) in the COP and SOP command allows access to the channel specific structures (CRAM and CR registers). Since the XR registers are common for both channels, no address field is required with the XOP command.

All three commands allow read and write access, which is indicated by bit 5 (RW). The bit fields LSEL and CODE specify the type and the length of data that follows the command.

6.3 Channel-Specific Configuration Registers (SOP Command)

Changes to these registers affect ***only*** the designated channel.

To modify or evaluate the SICOFI®2-µC status, the contents of up to 6 configuration registers CR0...CR5 may be transferred to or from the SICOFI®2-µC. This is started by a SOP-Command (**S**tatus **Op**eration Command).

SOP Command

Bit	7	6	5	4	3	2	1	0
	AD		**RW**	**1**	**0**	**LSEL**		

AD Address Information

00 Channel 1 CR registers are addressed with this command

01 Channel 2 CR registers are addressed with this command

RW Read/Write Information
Selects between read or write access to the SICOFI®2-µC

0 Write to CR registers

1 Read from CR registers

LSEL Length select information (see also programming procedure)
This field identifies the number of subsequent data bytes

000 SOP_0 command followed by 1 data byte (CR0)

001 SOP_1 command followed by 2 data bytes (CR1, CR0)

010 SOP_2 command followed by 3 data bytes (CR2, CR1, CR0)

011 SOP_3 command followed by 4 data bytes (CR3, CR2, CR1, CR0)

100 SOP_4 command followed by 5 data bytes (CR4, CR3, CR2, CR1, CR0)

101 SOP_5 command followed by 6 data bytes (CR5, CR4, CR3, CR2, CR1, CR0)

All other codes are reserved for future use!

Note: To access individual configuration registers CR0 to CR5, simply abort the SOP command sequence SOP_0 to SOP_5 after the transmission of the first data byte by setting CS# to high.

6.3.1 CR0 Configuration Register 0

Configuration register CR0 defines the basic SICOFI®2-µC settings per channel. Setting each of the 8 bits enables/disables the programmable digital filters.

Bit	7	6	5	4	3	2	1	0
	TH	**IM/R1**	**FRX**	**FRR**	**AX**	**AR**	**TH-SEL**	

TH Enable TH- (Transhybrid Balancing) Filter

0 TH-filter disabled
1 TH-filter enabled

IM/R1 Enable IM-(Impedance Matching) Filter and R1-Filter

0 IM-filter and R1-filter disabled, not recommended
1 IM-filter and R1-filter enabled

In applications where the IM/R1-Filter is not needed, it must still be switched on with following coefficients to realize the transfer function H(z)=0:
IM/R1-part1: 00 90 09 00 90 09 00 00 (Coeff. 7,6,...1,0)
IM/R1-part2: 7F FF 00 00 90 14 40 08 (Coeff. 7,6,...1,0)

FRX Enable FRX (Frequency Response Transmit)-Filter

0 FRX-filter disabled
1 FRX-filter enabled

FRR Enable FRR (Frequency Response Receive)-Filter

0 FRR-filter disabled
1 FRR-filter enabled

AX Enable AX-(Amplification/Attenuation Transmit) Filter

0 AX-Filter disabled (AX1 and AX2)
1 AX-Filter enabled (AX1 and AX2)

AR Enable AR-(Amplification/Attenuation Receive) Filter

0 AR-Filter disabled (AR1 and AR2)
1 AR-Filter enabled (AR1 and AR2)

TH-SEL 2-bit field to select one of four programmed TH-filter coefficient sets

00 TH-filter coefficient set 1 is selected
01 TH-filter coefficient set 2 is selected

6.3.2 CR1 Configuration Register 1

Configuration register CR1 selects tone generator modes and other operation modes per channel.

Bit	7	6	5	4	3	2	1	0
	ETG2	**ETG1**	**PTG2**	**PTG1**	**LAW**	**0**	**0**	**PU**

ETG2 Enable programmable tone generator 2.
Tone Generator 2 is not available if Level Metering Function is enabled!

0 Programmable Tone Generator 2 is disabled

1 Programmable Tone Generator 2 is enabled

ETG1 Enable programmable Tone Generator 1

0 Programmable Tone Generator 1 is disabled

1 Programmable Tone Generator1 is enabled

PTG2 User programmed frequency or fixed frequency is selected

0 Fixed frequency for Tone Generator 2 is selected (1 kHz)

1 Programmed frequency for Tone Generator 2 is selected

PTG1 User programmed frequency or fixed frequency is selected

0 Fixed frequency for Tone Generator1 is selected (1 kHz)

1 Programmed frequency for Tone Generator 1 is selected (Frequency is programmed with a COP Command)

LAW PCM - Law selection

0 A-Law is selected

1 µ-Law (µ255 PCM) is selected

PU Power Up, sets the addressed channel to Power Up / Down

0 The addressed channel is set to Power Down (standby)

1 The addressed channel is set to Power Up (operating)

6.3.3 CR2 Configuration Register 2

Bit	7	6	5	4	3	2	1	0
	COT/R			0	IDR	LM	LMR	V+T

COT/R Selection of Cut-off Transmit/Receive Paths (see **Chapter 8.3**)

000	Normal Operation	
001	COT16	Cut Off Transmit Path at 16 kHz (input of TH-Filter)
010	COT8	Cut Off Transmit Path at 8 kHz (shortens the input of the compressor unit to ground, resulting in PCM idle codes in the transmit time slot)
101	COR4M	Cut Off Receive Path at 4 MHz (POFI-output)
110	COR64	Cut Off Receive Path at 64 kHz (IM-filter input)

IDR Initialize Data RAM

0 Normal operation is selected

1 Contents of Data RAM is set to 0 (can be used for test purposes)

LM Level Metering function.
A signal fed to A-/µ-Law compression via AX- and HPX-filters (from a digital loop or externally via VIN, is rectified and the power is measured. If the power exceeds a certain value, loaded to XR7, bit LMR is set to "1". The power of the incoming signal can be adjusted by AX-filters.

0 Level Metering function is disabled

1 Level Metering function is enabled

LMR Result of Level Metering function (this bit ***cannot*** be written)

0 Level detected was lower than the reference (see XR7)

1 Level detected was higher than the reference (see XR7)

V+T Add Voice signal and Tone Generator signal

0 Voice or Tone Generator is fed to the Digital-to-Analog Converter (DAC) (Activating the tone generators will cut off the voice signal)

1 Voice and Tone Generator Signals are added, and fed to the DAC

6.3.4 CR3 Configuration Register 3

Bit	7	6	5	4	3	2	1	0
	Test-Loops				**AGX**	**AGR**	**D-HPX**	**D-HPR**

Test-Loops 4 bit field for selection of Analog and Digital Loop Backs (see **Chapter 8**)

0000	No loop back is selected (normal operation)	
0001	ALB-PFI	Analog Loop Back via PREFI-POFI is selected
0011	ALB-4M	Analog Loop Back via 4 MHz is selected
0100	ALB-PCM	Analog Loop Back via 8 kHz (PCM) is selected and **in all channels active**. *(required slope setting in XR6.6, XR6.5 = 00 or 11).*
0101	ALB-8K	Analog Loop Back via 8 kHz (linear) is selected
1000	DLB-ANA	Digital Loop Back via analog port is selected
1001	DLB-4M	Digital Loop Back via 4 MHz is selected
1100	DLB-128K	Digital Loop Back via 128 kHz is selected
1101	DLB-64K	Digital Loop Back via 64 kHz is selected
1111	DLB-PCM	Digital Loop Back via PCM-registers is selected

AGX Analog gain in transmit direction

0 Analog gain is disabled

1 +6.02 dB analog gain is enabled (amplification)

AGR Analog gain in receive direction

0 Analog gain is disabled

1 -6.02 dB analog gain is enabled (attenuation)

D-HPX Disable high pass in transmit direction see also **Chapter 3.1.2**.

0 Transmit high pass is enabled

1 Transmit high pass is disabled
In this case the transmit-path signal is attenuated 0.06 dB

D-HPR Disable highpass in receive direction see also **Chapter 3.1.2**.

0 Receive high pass is enabled

1 Receive high pass is disabled
In this case the receive-path signal is attenuated 0.12 dB

6.3.5 CR4 Configuration Register 4

Configuration register CR4, sets the receiving time slot and the receiving PCM-highway.

Bit	7	6	5	4	3	2	1	0
	R-WAY	**RS6**	**RS5**	**RS4**	**RS3**	**RS2**	**RS1**	**RS0**

R-WAY Selects the PCM highway for the receiving of PCM-data

0 PCM-Highway A is selected

1 PCM-Highway B is selected

RS[6:0] Selects the time slot (0 to 127) used for receiving the PCM-data

The time slot number is binary coded

0 0 0 0 0 0 0 Time slot 0 is selected

0 0 0 0 0 0 1 Time slot 1 is selected

... ...

1 1 1 1 1 1 0 Time slot 126 is selected

1 1 1 1 1 1 1 Time slot 127 is selected

6.3.6 CR5 Configuration Register 5

Configuration register CR5, sets the transmit time slot and the transmit PCM-highway.

Bit	7	6	5	4	3	2	1	0
	X-WAY	**XS6**	**XS5**	**XS4**	**XS3**	**XS2**	**XS1**	**XS0**

X-WAY Selects the PCM highway for transmitting PCM-data

0 PCM-Highway A is selected

1 PCM-Highway B is selected

XS[6:0] Selects the time slot (0 to 127) used for transmitting the PCM-data

The time slot number is binary coded

0 0 0 0 0 0 0 Time slot 0 is selected

0 0 0 0 0 0 1 Time slot 1 is selected

... ...

1 1 1 1 1 1 0 Time slot 126 is selected

1 1 1 1 1 1 1 Time slot 127 is selected

6.4 Common Configuration Registers (XOP Command)

The Common Configuration Registers XR0 through XR7 determine global, channel-independent settings. They are accessed through **XOP Command Sequences**, and provide control of the following blocks and functions:

- Signaling Interface (Logic Levels and Debouncing),
- Master-, PCM-, and Chopper Clock Settings,
- PCM Frame Alignment, Detection of Time Slot Contentions,
- Level Metering Threshold Setting, and
- Version ID.

XOP Command

Bit	7	6	5	4	3	2	1	0
	RST	**0**	**RW**	**1**	**1**	**LSEL**		

RST Software Reset (same as RESET#-pin, valid for both channels)

1 Reset

0 Normal operation

RW Read / Write Information
Enables reading from SICOFI®2-µC or writing information to SICOFI®2-µC

0 Write to the SICOFI®2-µC

1 Read from the SICOFI®2-µC

LSEL Length select information, for setting the number of subsequent data bytes

000 XOP_0 command followed by 1 data byte (XR0)

001 XOP_1 command followed by 2 data bytes (XR1, XR0)

010 XOP_2 command followed by 3 data bytes (XR2, XR1, XR0)

... ...

111 XOP_7 command followed by 8 data bytes (XR7, XR6, XR5, XR4, XR3, XR2, XR1, XR0)

Note: To access individual configuration registers XR0 to XR7, simply abort the XOP command sequence XOP_0 to XOP_7 after the transmission of the first data byte by setting CS# to high.

6.4.1 XR0 Extended Register 0

This register transfers information from or to the signaling pins.

The signaling connection between SICOFI®2-µC and a SLIC is performed by the SICOFI®2-µC signaling input and output pins. The Configuration Registers XR0 ... XR3 are used to select the pins and to define the direction of the bidirectional pins. The information of the input pins may be selected to be sent upstream. Data at the signaling input pins are read by the microcontroller. The microcontroller can also write information to the output pins.

Note: XR0 values depend on the type of access:

Bit	7	6	5	4	3	2	1	0
XOP-Read:	**0**	**0**	**0**	**0**	**SI2_1**	**SI2_0**	**SI1_1**	**SI1_0**
XOP-Write:	**0**	**0**	**0**	**0**	**SO2_1**	**SO2_0**	**SO1_1**	**SO1_0**

If accessed through an **XOP-Read** Command:	The logic input level of pin ‘SIx_y’ is indicated in bit ‘**SIx_y**’.
If accessed through an **XOP-Write** Command:	The logic output level of pin ‘SOx_y’ is set with bit ‘**SOx_y**’

6.4.2 XR1 Extended Register 1

This register transfers information to or from the programmable signaling pins.

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**SB2_1**	**SB2_0**	**SB1_1**	**SB1_0**

Bits SBx_y	**Pin ‘SBx_y’ is input** (configured in XR2)	**Pin ‘SBx_y’ is output** (configured in XR2)
Access through **XOP-Read:**	The logic level of pin ‘SBx_y’ is indicated in bit ‘**SBx_y**’.	Read-back Zero
Access through **XOP-Write:**	Ignored	The logic output value of pin ‘SBx_y’ is set with bit ‘**SBx_y**’

Note: After a ‘Reset’ of the device, all programmable pins are input pins!

6.4.3 XR2 Extended Register 2

This register controls the direction of the programmable signaling pins.

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**PSB2_1**	**PSB2_0**	**PSB1_1**	**PSB1_0**

Bits PSBx_y	**Bi-directional signaling pin SBx_y is configured as**:
0	Pin SBx_y is indication input
1	Pin SBx_y is command output

Note: After a 'Reset' of the device, all programmable pins are input pins!

6.4.4 XR3 Extended Register 3

This register transfers information to or from the programmable signaling pins and configures these pins.

Bit	7	6	5	4	3	2	1	0
	0	**0**	**SB2_2**	**SB1_2**	**0**	**0**	**PSB2_2**	**PSB1_2**

Bits SBx_y	**Pin 'SBx_y' is input** (configured in XR2)	**Pin ''SBx_y' is output** (configured in XR2)
Access through **XOP-Read:**	The logic level of pin 'SBx_y' is indicated in bit '**SBx_y**'.	Read-back Zero
Access through **XOP-Write:**	Ignored	The logic output value of pin 'SBx_y' is set with bit '**SBx_y**'

Bits PSBx_y	**Bi-directional signaling pin SBx_y is configured as**:
0	Pin SBx_y is indication input
1	Pin SBx_y is command output

Note: After a 'Reset' of the device, all programmable pins are input pins!

6.4.5 XR4 Extended Register 4

Register XR4 provides two optional functions: debouncing of signaling input changes, and the configuration of the programmable output pin CHCLK1.

Bit	7	6	5	4	3	2	1	0
	N				T			

Table 20 Signal Debouncing

Field N				Signaling Debounce Period
0	0	0	0	Debounce and interrupt generation is disabled
0	0	0	1	Debounce period 2 ms
0	0	1	0	Debounce period 4 ms
...	...	...	...	...
1	1	0	1	Debounce period 26 ms
1	1	1	0	Reserved
1	1	1	1	Debounce period 0.5 ms

The logic levels on all signaling input pins have to be stable for the time period shown in **Table 20** before changes will be detected. This feature ensures that only valid signaling information will be passed on to the microcontroller via registers XR0, XR1, and XR3. Glitches can be filtered out by programming N to an appropriate value between 0.5 ms and 26 ms. Examples for this mechanism are shown in **Figure 10**.

With N = 0, the debouncing and the interrupt generation are disabled, and the current signaling status can be read via the Microcontroller Interface (XOP-read command).

Table 21 Configuration of CHCLK1

Field T				**Output Frequency on Pin CHCLK1** (Requires a valid MCLK input signal.)
0	0	0	0	CHCLK1 is set to 1 (high) permanently
0	0	0	1	T is 2ms
0	0	1	0	T is 4ms
...	...	...	...	...
1	1	0	1	T is 26 ms
1	1	1	0	T is 28 ms
1	1	1	1	is set to 0 (low) permanently

6.4.6 XR5 Extended Register 5

Bit	7	6	5	4	3	2	1	0
	MCLK-SEL		CRSH_A	CRSH_B	CHCLK2		Version	

MCLK-SEL Selects Master Clock frequency to be applied to pin MCLK

The MCLK signal must be synchronous to the 8-kHz FSC signal.

00 1536 kHz selected

01 2048 kHz selected

10 4096 kHz selected

11 8192 kHz selected

Note: A crash occurs if both channels are programmed to transmit (talk) in the same time slot on the same highway. In this event, a crash-bit will be set and transmission will be disabled for both channels. After correct time slot programming (CR5), the crash-bit will be cleared after XR5 has been read

CRSH_A Crash on PCM-Highway A (line DXA).

0 No crash detected

1 Crash detected (bad programming in CR5-registers)

CRSH_B Crash on PCM-Highway B (line DXB).

0 No crash detected

1 Crash detected (bad programming in CR5-registers)

CHCLK2 Selects chopper clock frequency on pin CHCLK2.

00 Pin CHCLK2 is set to 1 (high)

01 512 kHz (requires a valid MCLK input signal.)

10 256 kHz (requires a valid MCLK input signal.)

11 16,384 kHz (internal master clock frequency, requires a valid MCLK input signal, and at least one of the four channels in ‘POWER UP’ state)

VERSION This two bit field identifies the specific chip version

00 Identifies Version 1.1 to 1.3 devices

01 Identifies Version 1.4 devices

10 Identifies Version 2.2 devices

6.4.7 XR6 Extended Register 6

This register configures the operation of the PCM Interface see also **Chapter 5.2**.

Bit	7	6	5	4	3	2	1	0
	C-MODE	**X-S**	**R-S**	**DRV_0**	**Shift**	**PCM-OFFSET**		

C-MODE	Defines the CLK-Mode for the PCM Interface
0	Single clocking is used. Bit length is one PCLK period.
1	Double clocking is used. Bit length is two PCLK periods.
X-S	Transmit Slope
0	Transmission starts with rising edge (see **Chapter 5.2.2**)
1	Transmission starts with falling edge (see **Chapter 5.2.2**)
R-S	Receive Slope
0	Data is sampled with falling edge of PCLK (see **Chapter 5.2.2**)
1	Data is sampled with rising edge of PCLK (see **Chapter 5.2.2**)
DRV_0	Driving Mode for Bit 0 (only available with Single Clock Mode)
0	Bit 0 is driven the whole PCLK-period
1	Bit 0 is driven during the first half of the PCLK- period only
Shift	Shifts the access to DXA/B and DRA/B by one PCLK-period (only available with Double Clock Mode)
0	No shift takes place
1	Access to DXA/B and DRA/B is shifted by one PCLK-period
PCM-OFFSET	Offset in number of bit periods added to time slot
000	No offset is added
001	One bit period is added
...	...
111	Seven bit periods are added

6.4.8 XR7 Extended Register 7

This register contains the 8-bit offset value for the level metering function.

Bit	7	6	5	4	3	2	1	0
	OF7	**OF6**	**OF5**	**OF4**	**OF3**	**OF2**	**OF1**	**OF0**

The value of the signal level measured by the level meter block is compared against the programmed value of the XR7. If the measured value is lower than the offset, bit CR2.1 (LMR) will be set to "0", if the measured level is higher the bit will be set to "1".

See ***Application Note 03.97 "Level Metering Functions of the SICOFI®4-µC"***.

6.5 Coefficients for the Programmable Filters (COP Commands)

With a COP command, coefficients for the programmable filters can be written to the SICOFI®2-µC Coefficient RAM or read from the Coefficient RAM via the Serial Microcontroller Interface for verification.

QSICOS software is used to generate the complete sequences of coefficients including the appropriate COP commands.

COP Command

Bit	7	6	5	4	3	2	1	0
	AD		**RW**	**0**	**CODE**			

AD Address information

00 Channel 1 of CRAM is addressed with this command

01 Channel 2 of CRAM is addressed with this command

RW Read/Write Information:
Selects between read or write access to the SICOFI®2-µC

0 Subsequent data is written to the SICOFI®2-µC

1 Read data from the SICOFI®2-µC

CODE Includes number of following bytes and filter-address

0000	TH-Filter coefficients (part 1)	(followed by 8 bytes of data)
0001	TH-Filter coefficients (part 2)	(followed by 8 bytes of data)
0010	TH-Filter coefficients (part 3)	(followed by 8 bytes of data)
0100	IM/R1-Filter coefficients (part 1)	(followed by 8 bytes of data)
0101	IM/R1-Filter coefficients (part 2)	(followed by 8 bytes of data)

0110	FRX-Filter coefficients	(followed by 8 bytes of data)
0111	FRR-Filter coefficients	(followed by 8 bytes of data)
1000	AX-Filter coefficients	(followed by 4 bytes of data)
1001	AR-Filter coefficients	(followed by 4 bytes of data)
1100	TG 1 - coefficients	(followed by 4 bytes of data)
1101	TG 2 - coefficients	(followed by 4 bytes of data)

6.5.1 Programming the General Filter Coefficients

Four sets of TH-filter coefficients can be loaded to the SICOFI®2-µC. Each of the two sets can be assigned to either of the SICOFI®2-µC channels, by setting the value of TH-SEL in configuration register CR0. Coefficient set 1 is loaded to the CRAM via channel 1, set 2 is loaded via Channel 2 and so on.

6.5.2 Programming the Channel-Specific Filter Coefficients

Individual coefficient sets are available for each of the two channels. They are stored in channel-specific CRAM locations.

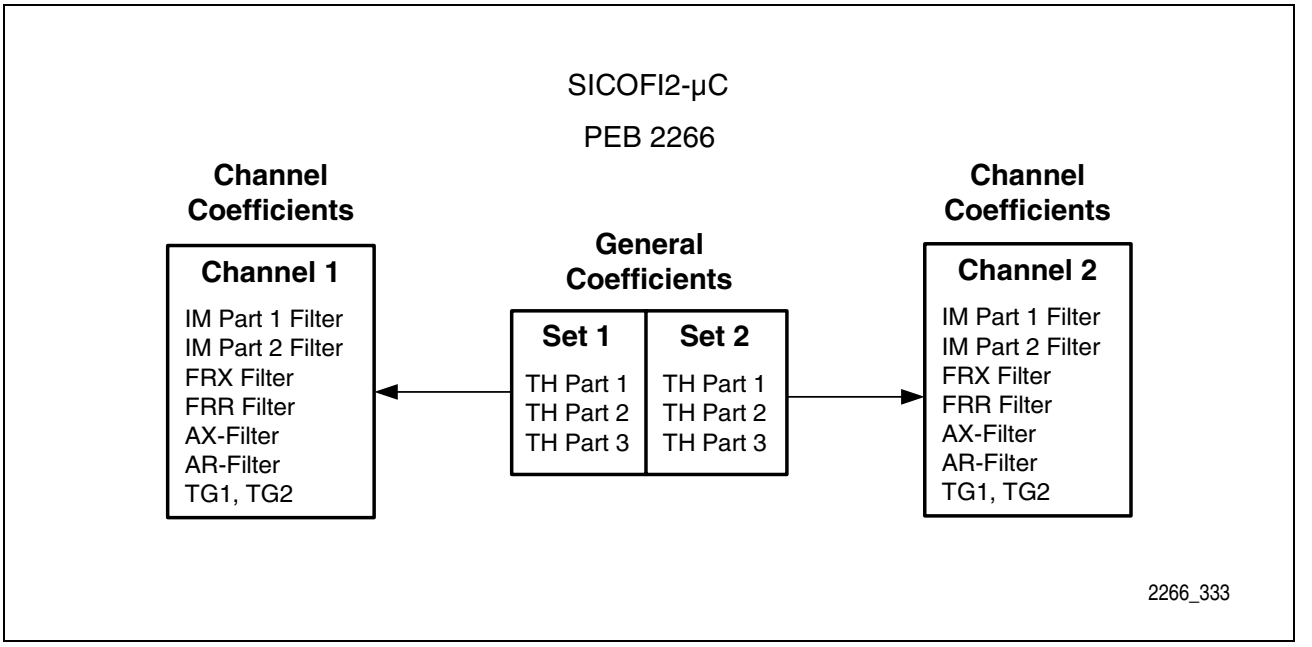


Figure 18 Storage of Coefficients in CRAM

6.6 Command Summary

Table 22 All Possible Command Sequences

Command Type	Write	Read	Data
XOP SW Reset	1001 1000	---	---
XOP_0	0001 1000	0011 1000	XR0
XOP_1	0001 1001	0011 1001	XR1, XR0
XOP_2	0001 1010	0011 1010	XR2, XR1, XR0
XOP_3	0001 1011	0011 1011	XR3, XR2, XR1, XR0
XOP_4	0001 1100	0011 1100	XR4, XR3, XR2, XR1, XR0
XOP_5	0001 1101	0011 1101	XR5, XR4, XR3, XR2, XR1, XR0
XOP_6	0001 1110	0011 1110	XR6, XR5, XR4, XR3, XR2, XR1, XR0
XOP_7	0001 1111	0011 1111	XR7, XR6, XR5, XR4, XR3, XR2, XR1, XR0
SOP_0	xy01 0000	xy11 0000	CR0
SOP_1	xy01 0001	xy11 0001	CR1, CR0
SOP_2	xy01 0010	xy11 0010	CR2, CR1, CR0
SOP_3	xy01 0011	xy11 0011	CR3, CR2, CR1, CR0
SOP_4	xy01 0100	xy11 0100	CR4, CR3, CR2, CR1, CR0
SOP_5	xy01 0101	xy11 0101	CR5, CR4, CR3, CR2, CR1, CR0
COP_0	xy00 0000	xy10 0000	TH-Filter Coefficients Part 1 (8 Bytes)
COP_1	xy00 0001	xy10 0000	TH-Filter Coefficients Part 2 (8 Bytes)
COP_2	xy00 0010	xy10 0000	TH-Filter Coefficients Part 3 (8 Bytes)
COP_4	xy00 0100	xy10 0100	IM/R1-Filter Coefficients Part 1 (8 Bytes)
COP_5	xy00 0101	xy10 0101	IM/R1-Filter Coefficients Part 2 (8 Bytes)
COP_6	xy00 0110	xy10 0110	FRX-Filter Coefficients (8 Bytes)
COP_7	xy00 0111	xy10 0111	FRR-Filter Coefficients (8 Bytes)
COP_8	xy00 1000	xy10 1000	AX-Filter Coefficients (4 Bytes)
COP_9	xy00 1001	xy10 1001	AR-Filter Coefficients (4 Bytes)
COP_C	xy00 1010	xy10 1010	TG1 Coefficients (4 Bytes)
COP_D	xy00 1011	xy10 1011	TG2 Coefficients (4 Bytes)

Note: “xy” is the specific channel address: Channel 1 = 00, Channel 2 = 01.

Table 22 summarizes all possible command sequences. Transmission is MSB first.

The next chapter includes some detailed examples of the data flow for read or write access. The command byte for read and write is only different in bit 5 RW. If the value of only one or a few of the registers is needed, the read time can be shortened by setting CS# to high, after receipt of the wanted byte.

6.7 Command Examples

The following examples show the order of the data flow on the DIN and DOUT pin. The Identification byte is always 1000 0001 and appears only on read commands to indicate the beginning of the data transfer. ‘Idle’ condition on DOUT results in a high-impedance state of the output. ‘Idle’ on DIN means that all input signals will be ignored.

XOP_0

Write Example: (RW=0)

DIN	XOP_0(w)	XR0
DOUT	idle	idle

Read Example: (RW=1)

DIN	XOP_0(r)	idle	idle
DOUT	idle	Ident.	XR0

XOP_5

Write Example: (RW=0)

DIN	XOP_5 (w)	XR5	XR4	XR3	XR2	XR1	XR0
DOUT	idle	idle	idle	idle	idle	idle	idle

Read Example: (RW=1)

DIN	XOP_5 (r)	idle	idle	idle	idle	idle	idle	idle
DOUT	idle	Ident	XR5	XR4	XR3	XR2	XR1	XR0

XOP_7

Write Example: (RW=0**)**

DIN	XOP_7 (w)	XR7	XR6	XR5	XR4	XR3	XR2	XR1	XR0

DOUT	idle	idle	idle	idle	idle	idle	idle	idle	idle

Read Example: (RW=1)

DIN	XOP_7 (r)	idle	idle	idle	idle	idle	idle	idle	idle	idle
DOUT	idle	Ident	XR7	XR6	XR5	XR4	XR3	XR2	XR1	XR0

SOP_0

Write Example: (RW=0**)**

DIN	SOP_0 (w)	CR0
DOUT	idle	idle

Read Example: (RW=1)

DIN	SOP_0 (r)	idle	idle
DOUT	idle	Ident.	CR0

SOP_5

Write Example: (RW=0**)**

DIN	SOP_5 (w)	CR5	CR4	CR3	CR2	CR1	CR0
DOUT	idle	idle	idle	idle	idle	idle	idle

Read Example: (RW=1)

DIN	SOP_5 (r)	idle	idle	idle	idle	idle	idle	idle
DOUT	idle	Ident	CR5	CR4	CR3	CR2	CR1	CR0

COP_0

Write Example: (RW=0**)**

DIN	COP_0 (w)	Coeff.8	Coeff.7	Coeff.6	Coeff.5	Coeff.4	Coeff.3	Coeff.2	Coeff.1
DOUT	idle	idle	idle	idle	idle	idle	idle	idle	idle

Read Example: (RW=1)

DIN	COP_0 (r)	idle	idle	idle	idle	idle	idle	idle	idle	idle
DOUT	idle	Ident	Coeff.8	Coeff.7	Coeff.6	Coeff.5	Coeff.4	Coeff.3	Coeff.2	Coeff.1

COP_8

Write Example: (RW=1)

DIN	COP_8 (w)	Coeff.4	Coeff.3	Coeff.2	Coeff.1
DOUT	idle	idle	idle	idle	idle

Read Example: (RW=1)

DIN	COP_8 (r)	idle	idle	idle	idle	idle
DOUT	idle	Ident	Coeff.4	Coeff.3	Coeff.2	Coeff.1

Example for Concatenated Command Sequences

DIN	**SOP_3(w)**	CR3	CR2	CR1	CR0	**XOP_1(w)**	XR1	XR0	**COP_3(w)**	Coeff3
DOUT	idle	idle	idle	idle	idle	idle	idle	idle	idle	idle

Coeff2	Coeff1	Coeff0	**SOP_2(r)**	idle	idle	idle	idle	**COP_C(r)**	idle	idle
idle	idle	idle	idle	ident	CR2	CR1	CR0	idle	ident	Coeff3

idle	idle	idle	**XOP_0(r)**	idle	idle
Coeff2	Coeff1	Coeff0	idle	ident	XR0

```
; SICOFI2-TE Configuration and Coefficients Programming Example
; (Modified File output format of QSUCCONV.EXE)

W 0 1D 80                          ; XR5: Master Clock 4096 kHz

W 0 15 01 01 00 00 00 00           ; Programming of channel 1
W 0 04 0B AC 53 33 3A 2A 30 00
W 0 05 78 BD 00 02 B3 32 50 08
W 0 07 02 8F C8 FF 07 AA A0 08
W 0 06 07 42 5A 34 25 1A 40 08
W 0 09 4B 59 BB 33
W 0 08 DD B2 32 4C
W 0 00 08 00 80 00 81 08 88 80
W 0 01 02 FB 17 A0 D8 DA 00 81
W 0 02 00 08 CD 23 EA BA 2A A2
W 0 15 01 01 00 00 01 FC

W 0 55 02 02 00 00 00 00           ; Programming of channel 2
W 0 44 0B AC 53 33 3A 2A 30 00
W 0 45 78 BD 00 02 B3 32 50 08
W 0 47 02 8F C8 FF 07 AA A0 08
W 0 46 07 42 5A 34 25 1A 40 08
W 0 49 4B 59 BB 33
W 0 48 DD B2 32 4C
W 0 40 08 00 80 00 81 08 88 80
W 0 41 02 FB 17 A0 D8 DA 00 81
W 0 42 00 08 CD 23 EA BA 2A A2
W 0 55 02 02 00 00 01 FC
```

Figure 19 QSICOS Output Example (TEST.SUC)

7 Application Hints

7.1 Support Tools

7.1.1 QSICOS Software

The programmable filters of the SICOFI®2-µC enable adaptation of the AC system behavior to the linecard circuit, especially to the SLIC and the given country-specific line characteristics.

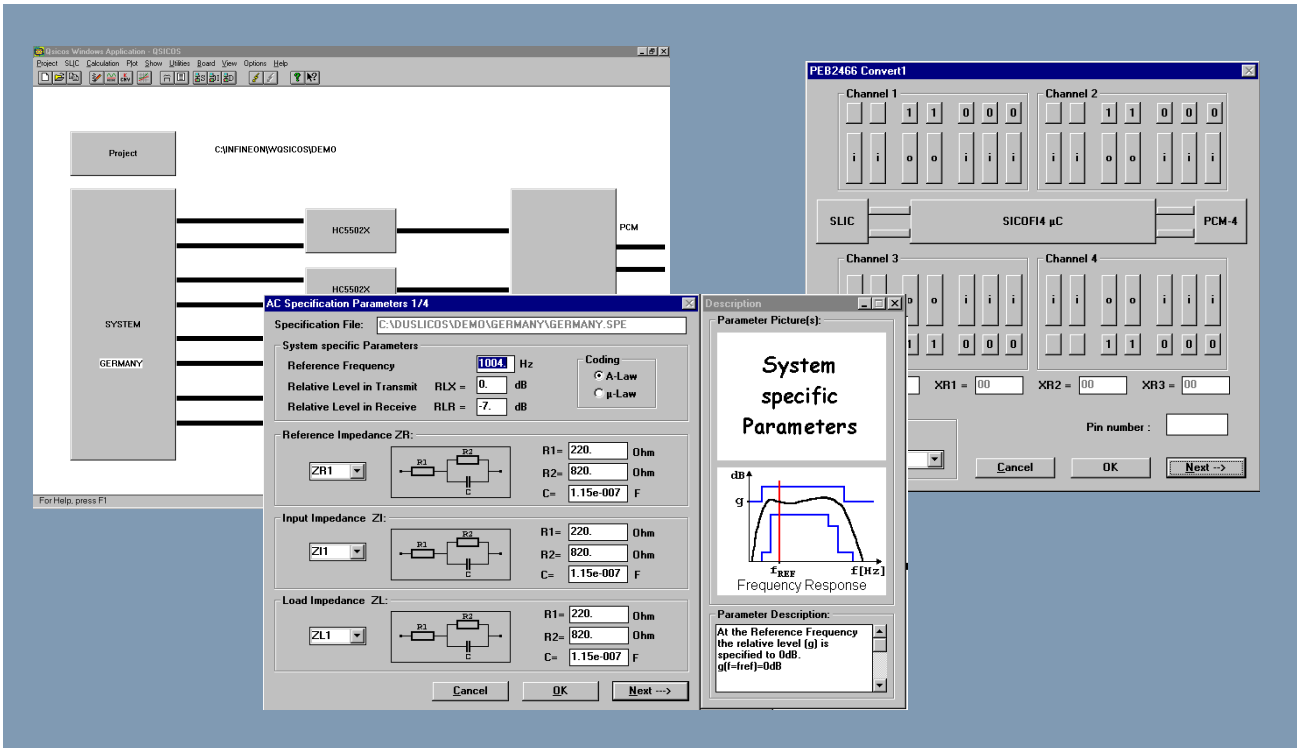


Figure 20 Dialogs of the QSICOS Coefficients Software

The Windows based **Q**uad **SI**COFI **Co**efficient **S**oftware (QSICOS) **Figure 20** allows the calculation of optimized sets of coefficients for programming the SICOFI®2-µC.

As shown in **Figure 21**, the QSICOS software needs the following input files for coefficient optimization:

1. External Circuit Description (K-Parameter Interface File):
   K-parameters are used to describe the electrical properties of the external circuit.

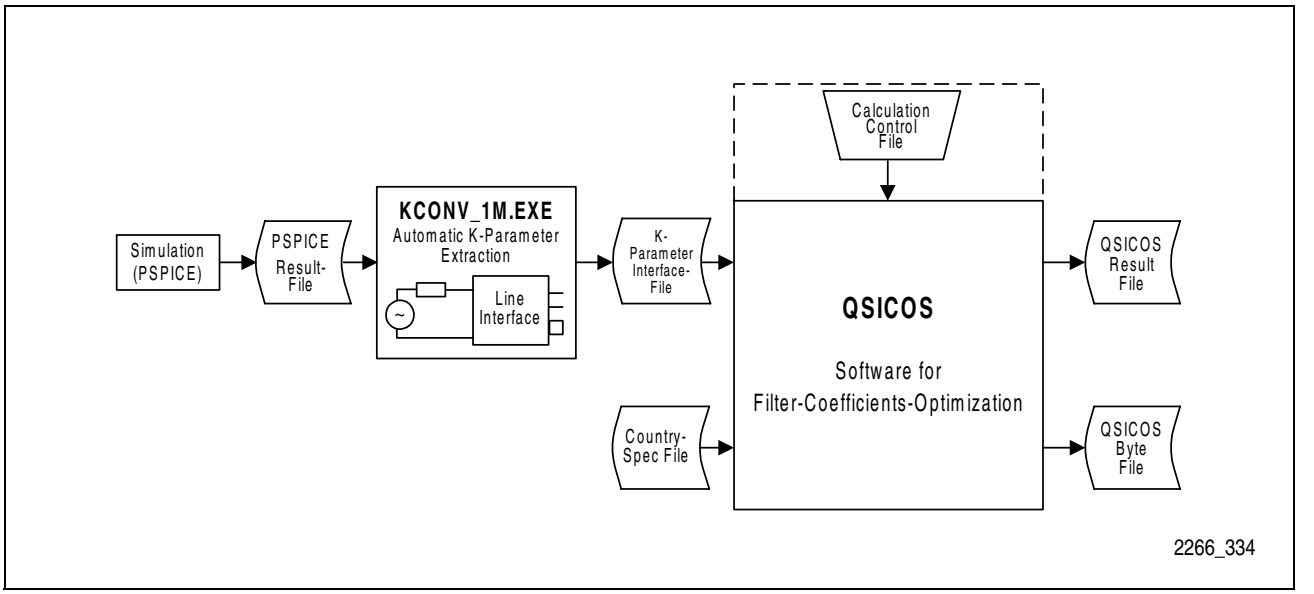


Figure 21 Input Files of QSICOS

To obtain the K-parameters, the results of a Windows based PSPICE® simulation of the external circuit are converted using the conversion program “KCONV_1M.EXE”.

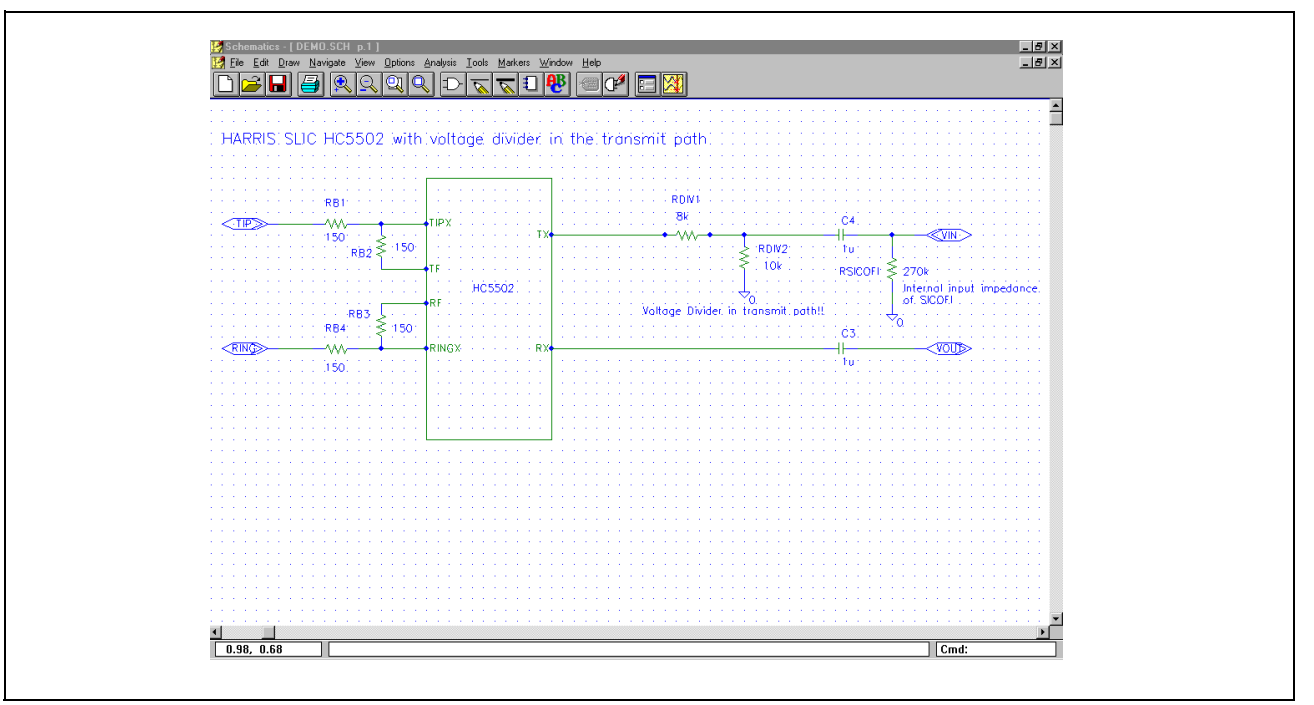


Figure 22 PSpice Schematic Editor

The conversion calculations are made in accordance with the three-port theory. Both the PSPICE Electrical Circuit Simulation Program **Figure 22** (Evaluation Version, V6.2) and the “KCONV_1M.EXE” conversion program are provided with the QSICOS Coefficient Calculation and Register Configuration Software.

2. PTT Specifications (Country-Spec File):
   The particular PTT specifications and the targeted AC behavior are described in the Country-Spec File.

The QSICOS software uses the input from the K-Parameter Interface File and the Country-Spec File to calculate filter coefficients which fulfill the PTT-defined/required AC behavior (**Figure 23**) for the whole system. A Calculation Control File provides additional input information on the optimization process.

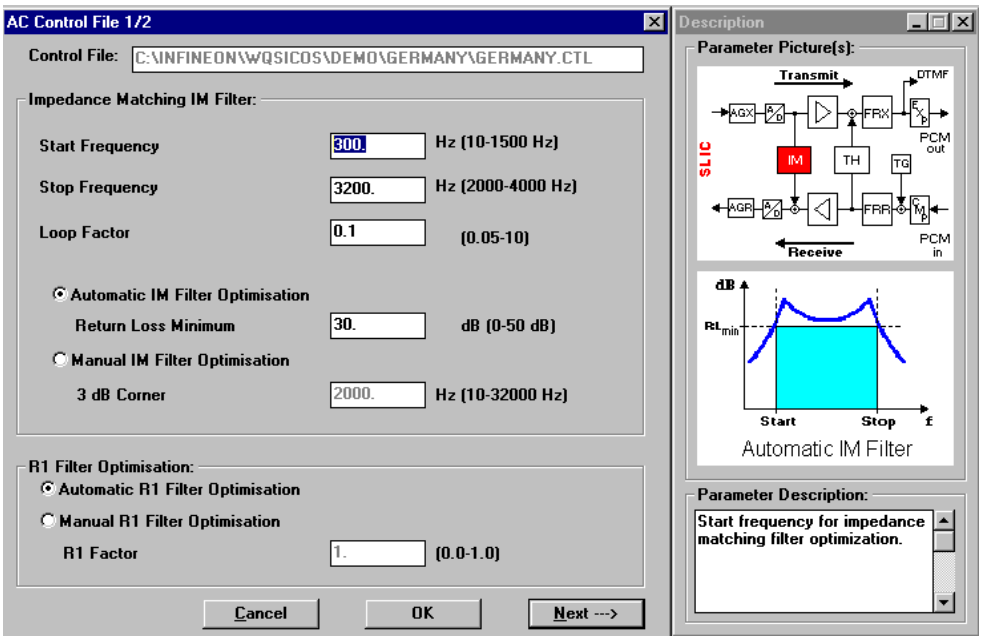


Figure 23 Parameter Settings of the Control File

QSICOS calculates coefficients for the following filters:

- Impedance Matching to adapt the system to the required line-impedance of the local loop (return loss calculation),
- Frequency Response Correction for both the receive and transmit paths,
- Level Adjustment for both the receive and transmit paths,
- Transhybrid Balancing, and
- Two programmable Tone Generators.

During the optimization process, the system behavior is calculated for the desired SLIC and the SICOFI2-µC. Some calculated functions can be displayed graphically to enable the product designer to quickly verify the required behavior and to easily make any additional optimizations manually. The following calculations are displayed graphically:

- Return loss,
- Frequency response in the receive and transmit paths, and
- Transhybrid loss.

An important feature of the QSICOS software is the ability to verify the calculated coefficients against criteria necessary to maintain overall system stability. The QSICOS software produces both a Byte File and a Result File. The Result File contains all of the numerical simulation results data as well as the programming bytes. After the calculation process the evaluation board can be directly programmed via the QSICOS user control.

7.1.2 EASY 2466 Tool Package

The EASY 2466 tool package includes an evaluation board which allows simple programming of the SICOFI®2-µC using a personal computer (PC). Conversion utilities are also provided in the tool package which convert the Byte File from the QSICOS software into a downloadable file usable by the evaluation board. This enables the product designer to compare the actual behavior of the hardware against the calculated results from the QSICOS software.

The EASY 2466 evaluation system has connectors for a test instrument to measure the transfer characteristics (e.g., the PCM-4 Channel Measuring Set by Wandel & Goltermann). This feature provides the option of system verification and fine-tuning. When the product designer has produced a set of coefficients which fulfill all required criteria, the values stored in the Byte File can be downloaded to the target hardware via the QSICOS user control, see at **Figure 24**.

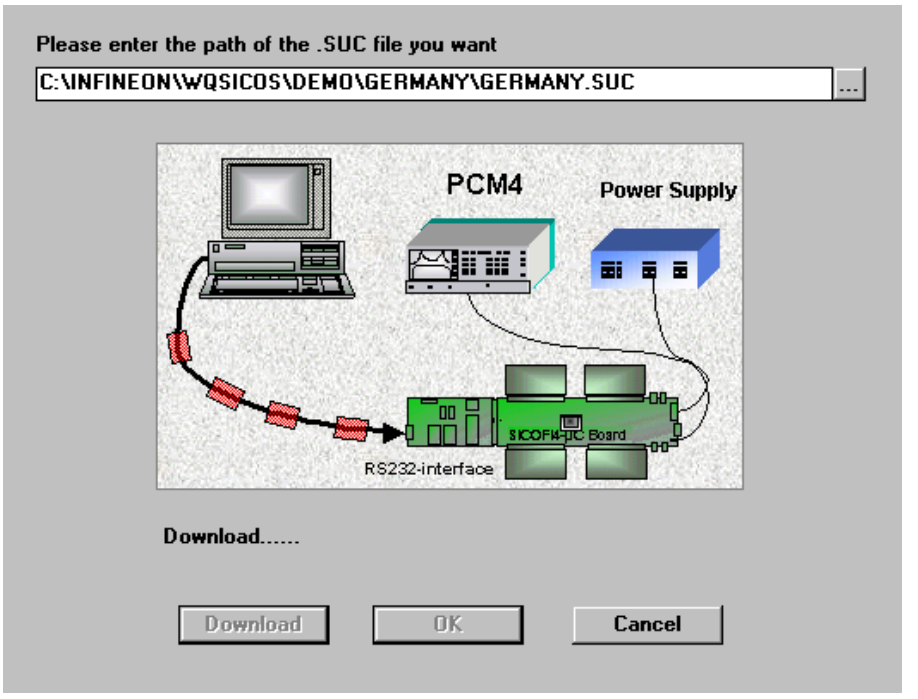


Figure 24 Dialog for Programming the Evaluation Board

7.2 Level Metering Function

The Level Metering Function allows measurement of a bandpass-filtered signal component in the transmit path. A test signal can be injected by an external source or by the on-chip tone generator. Level metering is used for line characterization, diagnostics of the SLIC and other external components, as well as device and system self-tests. This function does not require any extra components.

Figure 25 shows how the Level Metering works. Level metering is activated by setting bit LM (CR2.2). A programmable bandpass filter (not shown) screens out a narrow frequency range that is programmable with TG2 coefficients. This signal is rectified and compared to a threshold value that is programmed in the XR7 register. Bit LMR (CR2.1) indicates whether the measured value is lower or higher than the programmed value. For a detailed description, see ***Application Note 03.97 "Level Metering Functions of the SICOFI®4-µC."***

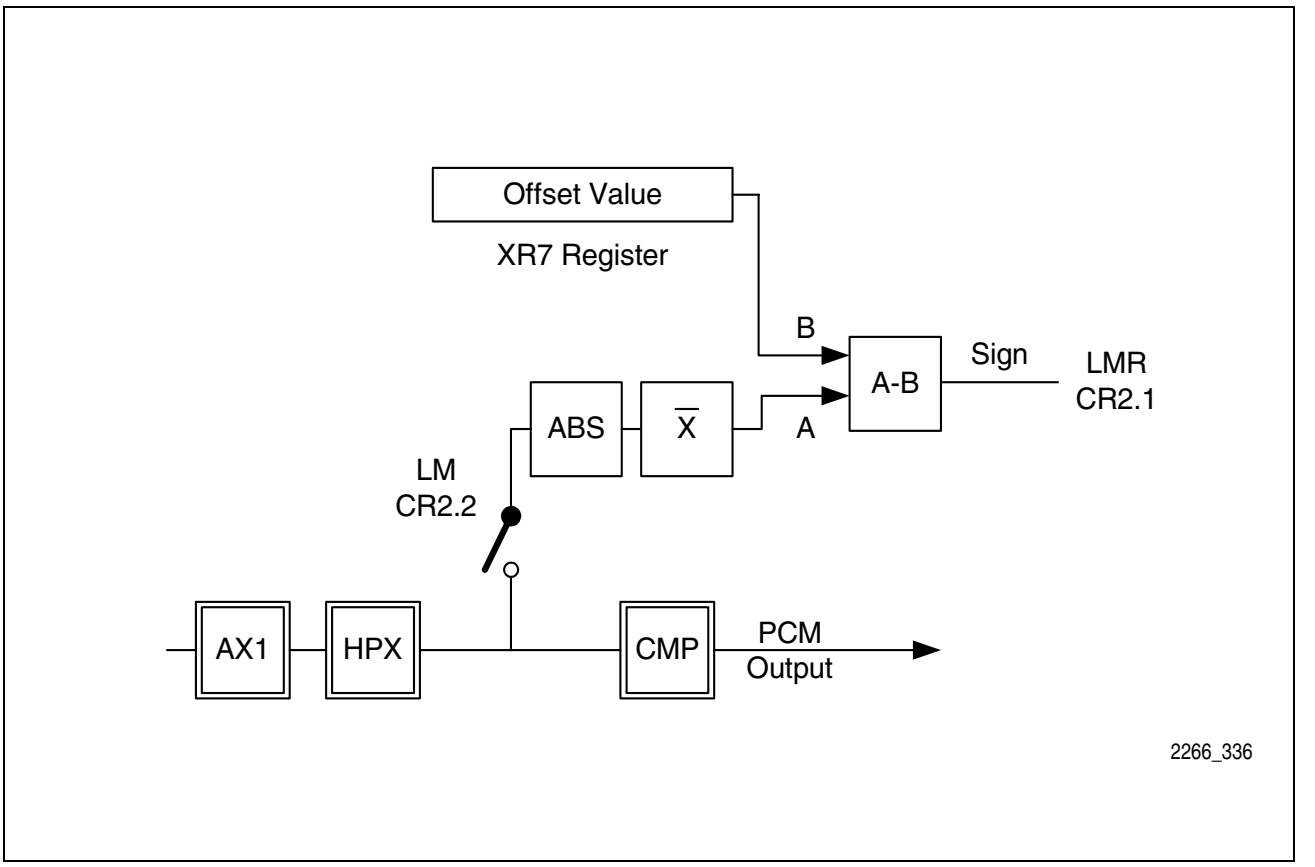


Figure 25 Level Metering

As shown in **Figure 26**, there are three different ways to inject a test signal for Level Metering:

- Built-in tone generators,
- Test equipment PCM4 by Wandel & Goltermann, or
- An external analog test source.

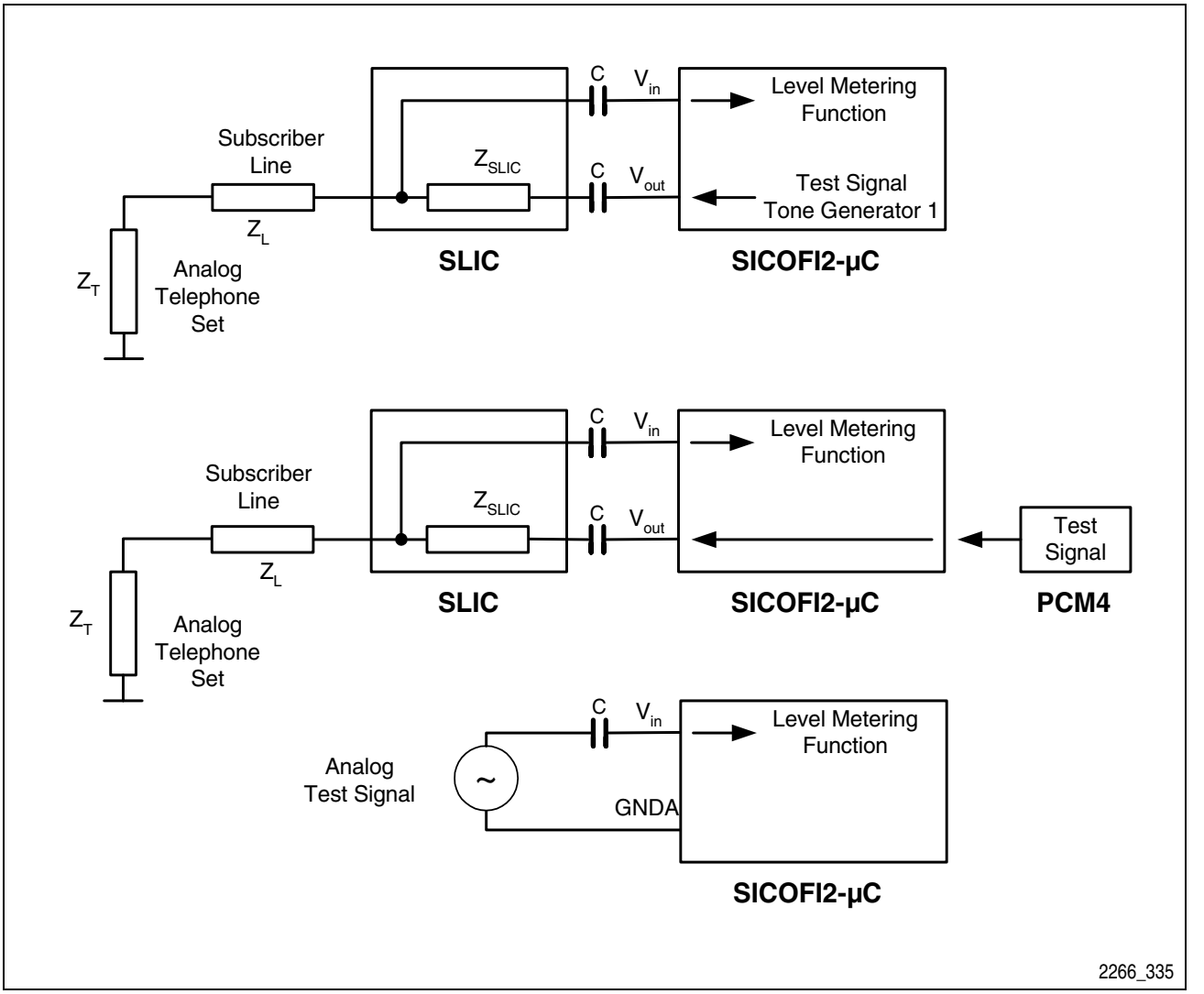


Figure 26 Level Metering with different Test Signal Sources

7.3 Programming the SICOFI®2-µC Tone Generators

Two independent tone generators are available to each channel. The tone generators are controlled through bits 7 to 4 in register CR1, and can be used with a fixed 1-kHz frequency or variable frequencies. Variable frequencies are programmed with COP-C and COP-D commands, followed by the appropriate 4-byte sequence. Enabling the tone generators will switch off the voice path in the receive direction by default. Bit 0 in CR 2 (V+T) can be set to mix the voice and tone signals.

The signals from the tone generators are bandpass-filtered to fulfill DTMF requirements.

QSICOS Coefficient Calculation and Register Configuration Software can be used to calculate the coefficients for specific tone generator frequencies.

Table 23 shows the programming sequences (command and coefficients) for some selected frequencies.

Table 23 Sample Tone Generators and Bandpass Filters Byte Sequences

Frequency	Programming Sequence	
	Tone Generator 1	**Tone Generator 2**
697 Hz	COP_C, 0A, 33, 5A, 2C	COP_D, 0A, 33, 5A, 2C
800 Hz	COP_C, 12, D6, 5A, C0	COP_D, 12, D6, 5A, C0
950 Hz	COP_C, 1C, F0, 5C, C0	COP_D, 1C, F0, 5C, C0
1008 Hz	COP_C, 1A, AE, 57, 70	COP_D, 1A, AE, 57, 70
2000 Hz	COP_C, 00, 80, 50, 09	COP_D, 00, 80, 50, 09

The signal levels produced by the tone generator are TG1= -4.58dB and TG2= -2.58dB. Signal amplitude can be adjusted with the digital gain stages AR1 and AR2. The signal can be routed to the transmit path by closing one of the ‘digital loops’ (see **Figure 28** in the following chapter).

Note: Tone Generator 1 may also be used as a signal source for Level Metering.

8 Test Modes

The SICOFI®2-µC features four test loops from the analog input back to the analog output (analog loops) and five test loops from the PCM input back to the PCM output (digital loops). The receive path and the transmit path can be interrupted at two different locations each.

8.1 Analog Loops

The four analog loops feed signals from the transmit path back into the receive path. **Figure 27** shows the locations of the analog loops. The analog loops are enabled through bits 7 to 4 in register CR3.

ALB-PFI connects the prefilter output to the postfilter input (no A/D and D/A conversion is performed).

ALB-4M connects the output of the ADC to the input of the DAC.

ALB-8k connects the output of the HPX Filter to the input of the HPR Filter,

ALB-PCM connects the output of the compressor unit to the input of the expander. Signals that are looped through ‘ALB-PCM’ have passed through all signal processing stages. It is in all channels active.

Note: For loop ‘ALB-PCM’, the PCM receive and transmit slopes must be set to oppositional clock edges (see Chapter 5.2.2). For example XR6.5=0 and XR6.6=0 or XR6.5=1 and XR6.6=1.
Channels 1 and 2 must be set to CR4.7=0 and CR5.7=0.

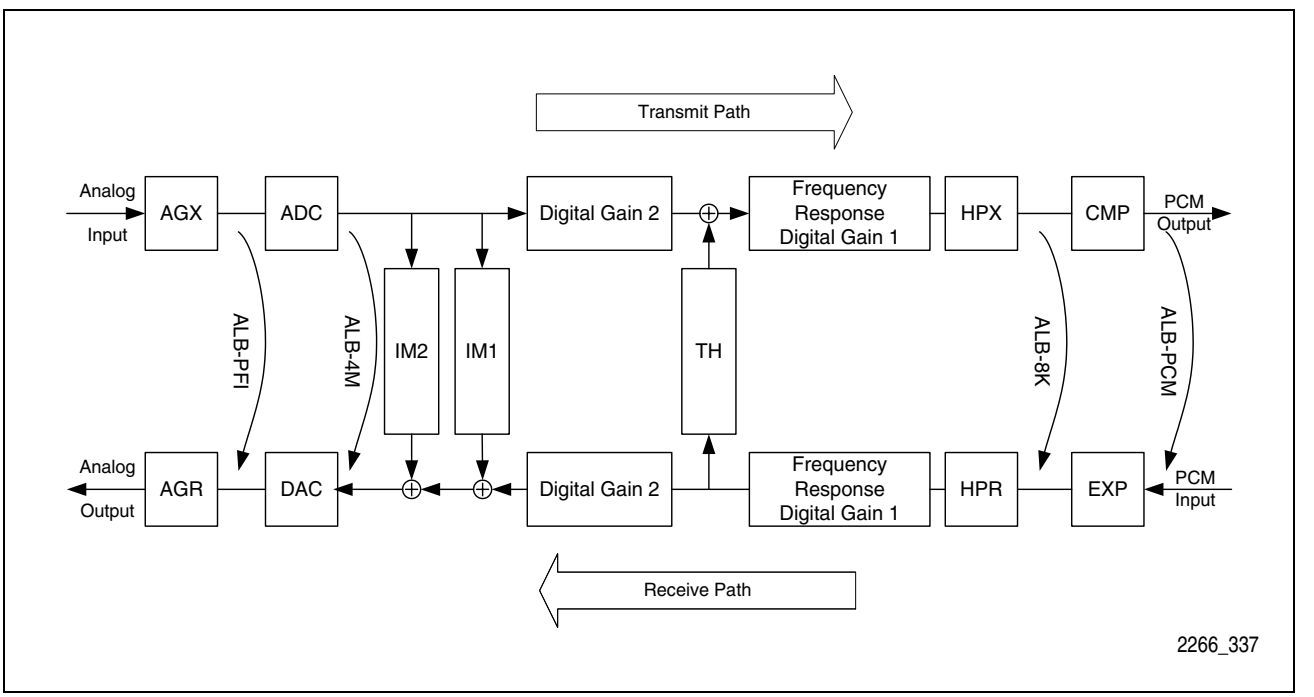


Figure 27 Analog Loops

8.2 Digital Loops

Digital Loops feed signals from the receive path back to the transmit path. There are five digital loops, which are shown in **Figure 28**.

The digital loops are enabled through bits 7 to 4 in register CR3.

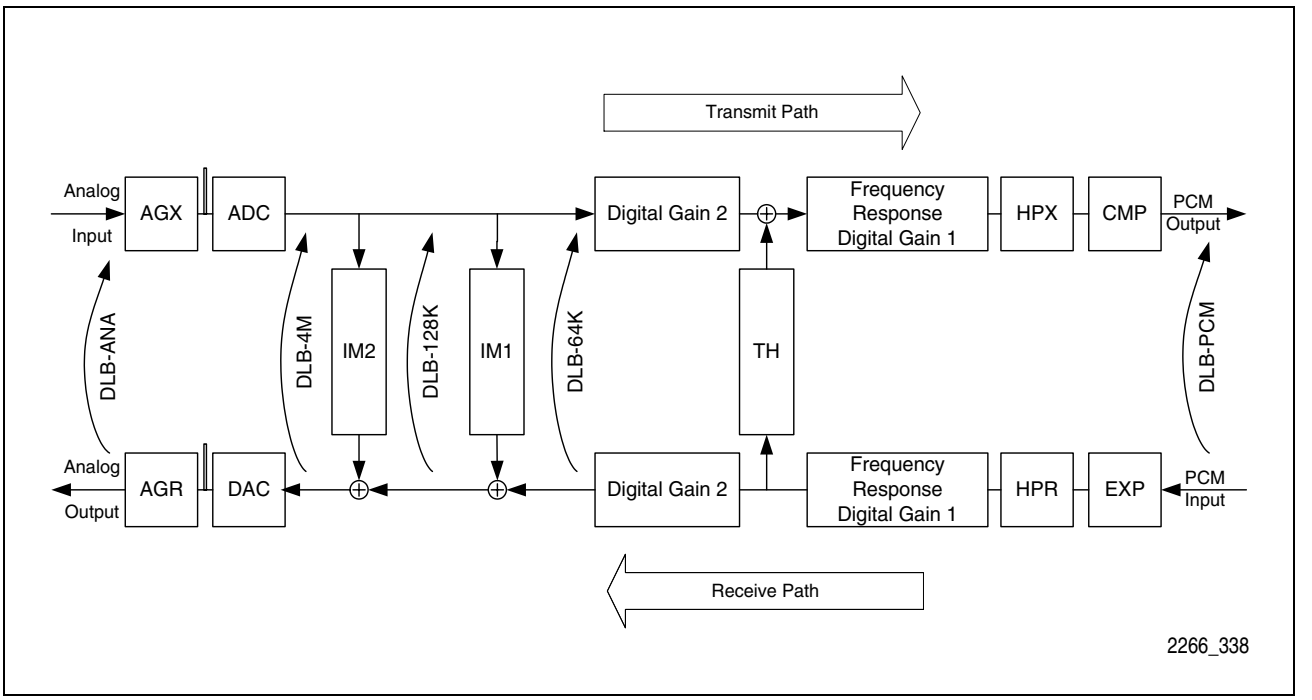


Figure 28 Digital loops

DLB-PCM returns PCM codes from the selected receive time slot on DRA or DRB to the selected transmit time slot on DXA or DXB. No bit manipulation is performed.

DLB-64K connects the output of Digital Receive Gain 2 with the input of Digital Transmit Gain 2.

DLB-128K loops the receive signal behind the IM1 Filter.

DLB-4M loops the receive signal behind the IM2 Filter.

DLB-ANA connects the output of the analog receive gain with the input of the analog transmit gain, thus providing a loop through the complete device.

8.3 Cut-Off's

The transmit path and the receive path can be cut off at two locations each. The Cut-Offs are programmed with bits 7 to 5 in register CR2. **Figure 29** shows the locations in the signal paths.

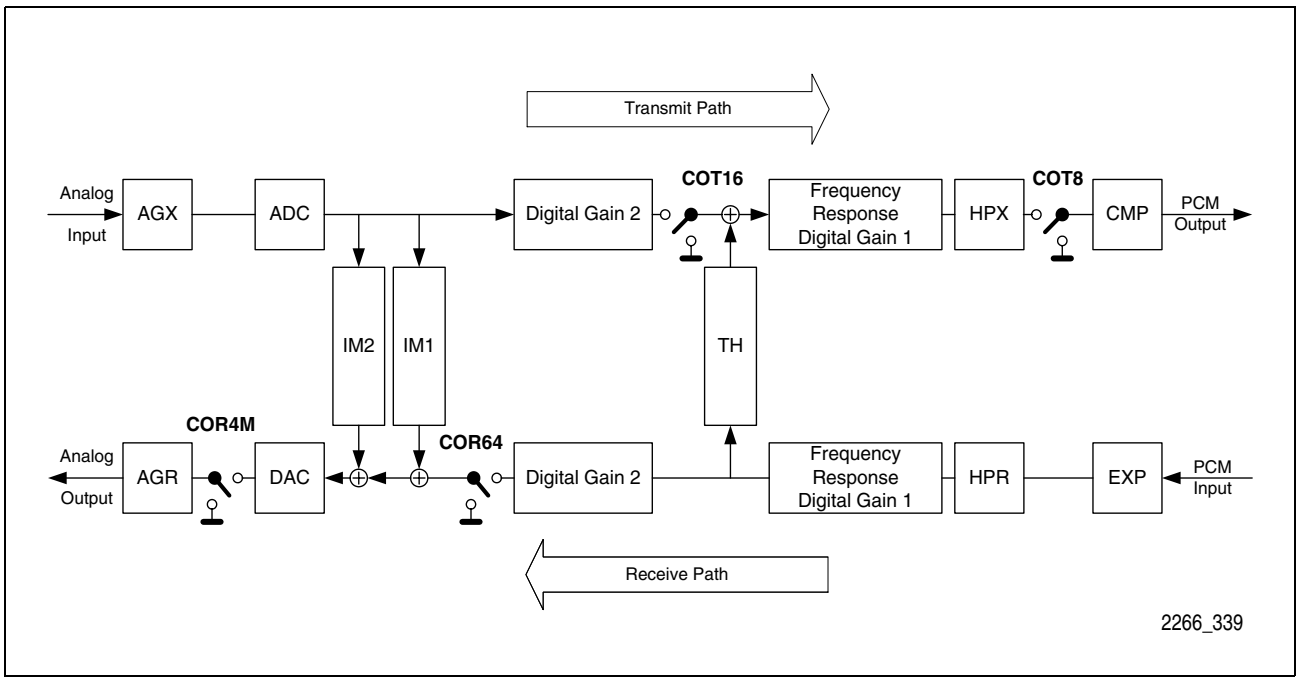


Figure 29 Cut Off's

Receive path

COR4M shortens the input of the Postfilter to ground. No AC signal on the analog output.

COR64 cuts off all receive signals, except for the signals coming through the Impedance Matching Filters.

Transmit path

COT16 cuts off all transmit signals, except for the signals coming through the Transhybrid Filter Function.

COT8 shortens the input of the compressor unit to ground, resulting in PCM idle codes in the transmit time slot.

9 Glossary

AC	**A**lternating **C**urrent
ADC	**A**nalog-to-**D**igital **C**onverter
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CRAM	**C**oefficient-**RAM**
DAC	**D**igital-to-**A**nalog **C**onverter
DC	**D**irect **C**urrent
DLC	**D**igital **L**oop **C**arrier
DSP	**D**igital **S**ignal **P**rocessor
DTMF	**D**ual **T**one **M**ulti **F**requency
FIR	**F**inite **I**mpulse **R**esponse
FTTC	**F**iber-**T**o-**T**he-**C**urb
IIR	**I**nfinite **I**mpulse **R**esponse
IOM-2	**I**SDN-**O**riented **M**odular **2**nd Generation
ITU	**I**nternational **T**elecommunication **U**nion
ITU-T	**I**nternational **T**elecommunication **U**nion-**T**elecommunication Standardization Sector (formerly CCITT)
PBX	**P**rivate **B**ranch E**x**change
PCM	**P**ulse **C**ode **M**odulation
PSTN	**P**ublic **S**witched **T**elephone **N**etwork
PTT	**P**ost **T**elephone **T**elegraph
QSICOS	**Q**uad **SI**COFI **Co**efficient **S**oftware
RITL	**R**adio-**I**n-**T**he-**L**oop
RT	**R**emote **T**erminal
SICOFI	**Si**gnal Processor **Co**dec **Fi**lter
SLIC	**S**ubscriber **L**ine **I**nterface **C**ircuit
t/r	**t**ip/**r**ing

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