AT&T Microelectronics

41LG and 41LP
Quad Differential Line Drivers

Features

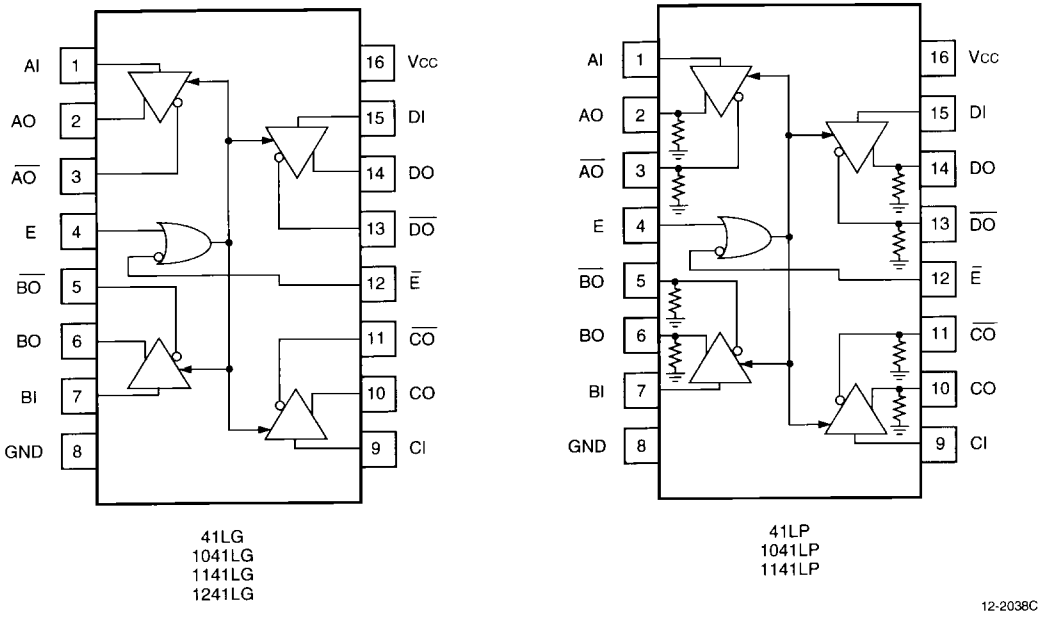
- Pin equivalent to the general-trade 26LS31 device, with improved speed, reduced power consumption, and significantly lower levels of EMI
- Four line drivers per package
- Logic which converts TTL input logic levels to differential, pseudo-ECL output logic levels
- 200 Mbits/s maximum data rates when used with the 41L*x* or 41M*x* receivers
- Meets ESDI standards
- No line loading when V_{CC} = 0 V
- High output drive for 50 Ω lines
- 200 mA short-circuit current (typical)
- 4.5 ns maximum propagation delay
- <0.2 ns output skew (typical)
- 0 °C to 85 °C ambient operating temperature range (See Section 9.)
- Single 5 V supply

Description

The 41LG and 41LP Quad Differential Line Driver integrated circuits transmit digital data over balanced transmission lines. They translate input TTL levels to differential, pseudo-emitter-coupled logic (pseudo-ECL) output levels. All devices in this family have four drivers with a common enable control. The 41LG and 41LP line drivers are compatible with many receivers, including the AT&T 41 Series receivers and transceivers and the general-trade 26LS32 device. The 41LG devices require the customer to supply external termination resistors on the circuit board. The 41LP devices have internal 220 Ω termination resistors to ground on each driver output. The 41LG/41LP line drivers are pin equivalent to the general-trade 26LS31 devices, but offer increased speed, decreased power consumption, and significantly lower levels of electromagnetic interference (EMI).

The packaging options that are available for the quad differential line drivers include a 16-pin DIP (41LG, 41LP), a 16-pin J-lead SOJ (1041LG, 1041LP), a 16-pin gull-wing SOIC (1141LG, 1141LP), and a 16-pin narrow-body gull-wing SOIC (1241LG).

Pin Information



Note: The device is disabled when E = 0 and $\overline{E}$ = 1.

Figure 3-1. 41LG and 41LP Logic Diagrams

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	7.0	V
Ambient Operating Temperature	T_A	0	85	°C
Storage Temperature	T_{stg}	–40	125	°C

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation.

ESD voltage thresholds are dependent on the critical parameters used to define the model. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltage presented here was obtained using this circuit.

Device	Rating
41LG/41LP Drivers	>1000 V

Electrical Characteristics

Table 3-1. 41LG and 41LP Power Supply Current Characteristics

T_A = 0 °C to 85 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current:					
41LG*					
All Outputs Disabled	I_{CC}	—	50	85	mA
All Outputs Enabled	I_{CC}	—	35	50	mA
41LP†					
All Outputs Disabled	I_{CC}	—	130	180	mA
All Outputs Enabled	I_{CC}	—	160	220	mA

* Measured with no load.

† The additional power dissipation is the result of integrating the termination resistors into the device. I_{CC} is measured with a 100 Ω resistor across the driver outputs.

Table 3-2. 41LG and 41LP Voltage and Current Characteristics

T_A = 0 °C to 85 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, V_{CC} = 4.5 V:					
Low, I_{OL} = –8.0 mA*	V_{OL}	—	3.0	V_{OH} – 0.8†	V
High, I_{OH} = –40.0 mA*	V_{OH}	3.0	4.0	—	V
High Z, I_{OH} = –1.0 mA, V_{CC} = 4.75 V	V_{OZ}	—	2.0	V_{OL} – 0.02	V
Input Voltages:					
Low, V_{CC} = 5.5 V	V_{IL}‡	—	—	0.7	V
High, V_{CC} = 4.5 V	V_{IH}‡	2.0	—	—	V
Clamp, V_{CC} = 4.5 V, I_{IN} = –5.0 mA	V_{IK}	—	—	–1.5	V
Short-circuit Output Current, V_{CC} = 5.5 V	I_{OS}§	–100	–200	–300	mA
Input Currents, V_{CC} = 5.5 V:					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	µA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	µA
Output Resistors (41LP)	R_O	—	220	—	Ω

* Typical value of the output current for the 41LG and the 41LP when terminated per Figure 6-5.

† V_{OL} must be a minimum of 0.8 V less than its complementary output.

‡ The input levels provide zero noise immunity and should be tested only in a static, noise-free environment.

§ Test must be performed one lead at a time to prevent damage to the device.

Timing Characteristics

Table 3-3. 41LG and 41LP Timing Characteristics (See Figures 6-1 and 6-2.)

Propagation-delay test circuit connected to output (see Figure 6-6).

T_A = 25 °C, V_{CC} = 5 V.

Symbol	Parameter	Typ	Max	Unit
	Propagation Delay:			
t_{P1}	Input High to Output	3.0	4.5	ns
t_{P2}	Input Low to Output	3.0	4.5	ns
	Disable Time:			
t_{PHZ}	High to High Impedance	10	15	ns
t_{PLZ}	Low to High Impedance	10	15	ns
	Enable Time:			
t_{PZH}	High Impedance to High	10	15	ns
t_{PZL}	High Impedance to Low	10	15	ns
t_{skew}	Output Skew, $\lvert t_{P1} - t_{P2} \rvert$	0.2	0.5	ns
Δt_{skew}	Difference Between Drivers	0.3	—	ns