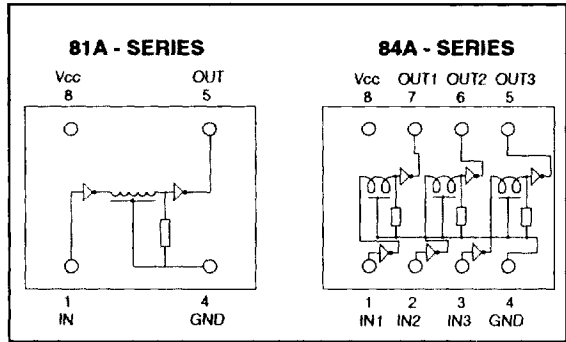


DUAL-IN-LINE PACKAGE (TOP VIEW)

- Schottky TTL buffered
- 8 pin package
- Low profile
- TTL compatible



description

The 81A and 84A series of Digital Delay Modules are Schottky TTL buffered delay lines providing precise delay times and direct compatibility with TTL. A single output fixed delay and triple independent equal delays are packaged in low profile 8 pin dual-in-line configurations. Internal termination of the delay lines and compensation for propagation delays are incorporated in the design so that no additional external components are required. These modules are very compact and are particularly suitable for high density board designs.

absolute maximum ratings over operating free-air temperature range

| | |
|---|----------------------|
| Supply voltage V_{cc} | 7V |
| Input voltage | 5.5V |
| Min pulse width as % of total delay | 80% |
| Input pulse repetition rate PRR | 3 x pulse width min. |
| Operating free-air temperature range | 0C to 70C |
| Storage temperature range | -55C to 125C |
| Temperature coefficient of delay | ± 300 ppm/C |
| Lead temperature 1.5mm from case for 10 seconds | 300C |

drive capabilities

Logic 0 & 1 output 10 TTL loads max.

81A, 84A Series

Single Output and Triple Independent 8 Pin DIP

**electrical specifications over operating free-air temperature range,
 $V_{CC} = 5 \pm 0.25V$**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|--|-----|-----|-----|---------|
| V_{IH} High-level input voltage | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.8 | V |
| V_{OH} High-level output voltage | $V_{IH} = 2V, I_{OH} = -1mA$ $V_{CC} = 4.75V$ | 2.7 | 3.4 | | V |
| V_{OL} Low-level output voltage | $V_{CC} = 4.75V$ $I_{OL} = 20mA, V_{IL} = 0.8V$ | | | 0.5 | V |
| I_{IH} High-level input current | $V_{CC} = 5.25V, V_{IH} = 2.7V$ | | | 50 | μA |
| I_{IL} Low-level input current | $V_{CC} = 5.25V, V_{IL} = 0.5V$ | | | -2 | mA |
| I_{CC} Supply current outputs high | $V_{CC} = 5.25V$ | | | 24 | mA |
| I_{CC} Supply current outputs low | $V_{CC} = 5.25V$ | | | 54 | mA |

81A, 84A Series
Single Output and Triple Independent 8 Pin DIP

delay characteristics Vcc = 5V, Ta = 25C, no load at output; input test pulse width 100% of total delay, rise time 3.0ns.

delay tolerance from input to tap $\pm 2\text{ns}$ or $\pm 5\%$ whichever is greater

81A SERIES Single Output 8 Pin DIP
Package style A with pins 2, 3, 6 and 7 missing

| PART No. | TOTAL DELAY (ns) $\pm 5\%$ (1) | RISE TIME (ns) max. | PART No. | TOTAL DELAY (ns) $\pm 5\%$ (1) | RISE TIME (ns) max. |
|-----------------|--|--------------------------------|-----------------|--|--------------------------------|
| 81A - 010 | 10 | 4 | 81A - 090 | 90 | 4 |
| 81A - 020 | 20 | 4 | 81A - 100 | 100 | 4 |
| 81A - 030 | 30 | 4 | 81A - 125 | 125 | 4 |
| 81A - 040 | 40 | 4 | 81A - 150 | 150 | 4 |
| 81A - 050 | 50 | 4 | 81A - 200 | 200 | 4 |
| 81A - 060 | 60 | 4 | 81A - 250 | 250 | 4 |
| 81A - 070 | 70 | 4 | 81A - 300 | 300 | 4 |
| 81A - 080 | 80 | 4 | 81A - 400 | 400 | 4 |

84A Triple independent 8 Pin DIP. Package style A

| PART No. | TOTAL DELAY (ns) $\pm 5\%$ (1) | RISE TIME (ns) max. | PART No. | TOTAL DELAY (ns) $\pm 5\%$ (1) | RISE TIME (ns) max. |
|-----------------|--|--------------------------------|-----------------|--|--------------------------------|
| 84A - 010 | 10 | 4 | 84A - 060 | 60 | 4 |
| 84A - 020 | 20 | 4 | 84A - 070 | 70 | 4 |
| 84A - 030 | 30 | 4 | 84A - 080 | 80 | 4 |
| 84A - 040 | 40 | 4 | 84A - 090 | 90 | 4 |
| 84A - 050 | 50 | 4 | 84A - 100 | 100 | 4 |

Note: Delays measured at 1.5V on leading edge, Rise Time measured from 0.75V to 2.4V (1) or $\pm 2\text{ns}$ whichever is greater.

